The Essence of Reliability Estimation during Operational Life for Achieving High System Dependability

Muhammad Aamir Khan, Hans G. Kerkhoff
Testable Design and Test of Integrated Systems (TDT) Group,
University of Twente, Centre of Telematics and Information Technology (CTIT),
Enschede, the Netherlands
{m.a.khan / h.g.kerkhoff}@utwente.nl

***Abstract*—System dependability has become important for critical applications in recent years as technology is moving towards smaller dimensions. Achieving high system dependability can be supported by reliability estimations during the *operational life*. In addition, this requires a workflow for regularly monitoring reliability and taking necessary repair actions. This has been proposed as a possible solution where degradation in system-level performance parameters, being directly influenced by variations and degradation in device-level parameters, has been considered a potential possibility for estimating reliability during the *operational life* of a system. Furthermore, the degradation rate of these system-level performance parameters depends on the initial values dispersion as a result of fabrication-related process variations. This requires a database of initial and runtime system-level performance parameters at the very start and at every potentially anticipated critical time-point of the system. Therefore, initial system specifications at the design-time and runtime performance parameter measurements stored in the database are used to estimate reliability and taking necessary actions for enhancing system dependability via repair. Simulation results for an example target system in a LabVIEW environment fully support the proposed idea.**

Keywords- reliability; lifetime prediction; dependable system

I. INTRODUCTION

System dependability has become important for critical applications in recent years as technology is moving towards smaller dimensions. In general, dependability of a system is defined as its trustworthiness that in a given environment the system will operate as expected and will not fail during its normal operation [1]. More precisely, it is a collection of system attributes like availability, reliability, maintainability, safety, security and survivability [2].

Among these attributes reliability can be considered as the most important attribute because reliability estimations at the design stage are essential to safely guardband the system performance for a certain life time. However, reliability estimations during the *operational life* of a system are crucial for a dependable system design. In this case, reliability can be better estimated in advance and proper actions can be anticipated in order to achieve a higher availability, proper maintainability and hence better dependability of the system. Therefore, it is important to know how reliability of a system is influenced by different physical mechanisms and how it can be monitored or estimated especially during its *operational life* for enhancing its dependability.

Fabrication-related process variations, due to difficulties in precise fabrication of small featured sized transistors, and different physical mechanisms like negative-bias temperature instability (NBTI), hot carrier injection (HCI), time-dependent dielectric breakdown (TDDB), and electromigration (EM), are the major causes affecting the circuit reliability. These fabrication-related process variations [3, 4] and different degradation mechanisms [5, 6] have been discussed separately and together in literature [7, 8] to address their impact on the reliability of ICs. Among these mechanisms, NBTI is considered to be the major contributor in CMOS aging [9, 10]. On the other hand, NBTI itself depends on the initial threshold voltage ($V_{th}(t_0)$) [11].

Therefore, fabrication-related process variations will introduce variations in the initial threshold voltage and they will further affect the NBTI behavior or the reliability of every device and hence the whole system. This means the NBTI behavior or the reliability of each device and the whole system will be different and initial-value dependent. *This highlights the importance of monitoring reliability during the operational life of a system despite the usual concept of reliability estimations at the design time.*

In this paper it is investigated how to estimate the reliability of systems during their operational life with the goal of enhancing system's dependability. Therefore, this paper will provide answers to the following questions:

1- How to estimate system reliability during its operational life (section II)?
2- How will initial values due to fabrication-related process variations affect these reliability estimations (section II)?
3- How will these estimations play an important role in improving the dependability (only reliability, maintainability, and availability are considered in this paper) of these systems (sections III and IV)?

The outline of the paper is as follows. Conventional reliability estimation methods based on the design-stage simulations and the proposed method to estimate the reliability during the operational life is discussed in the next section.

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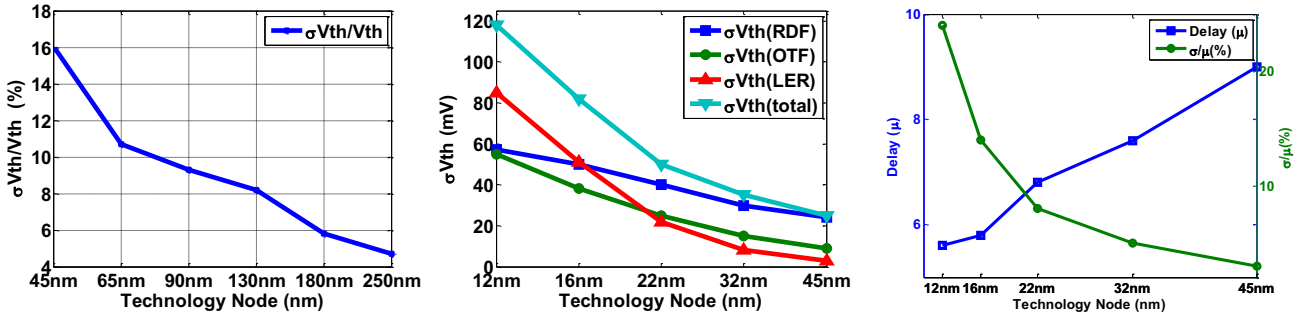
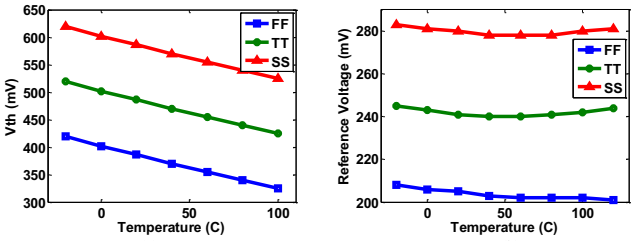


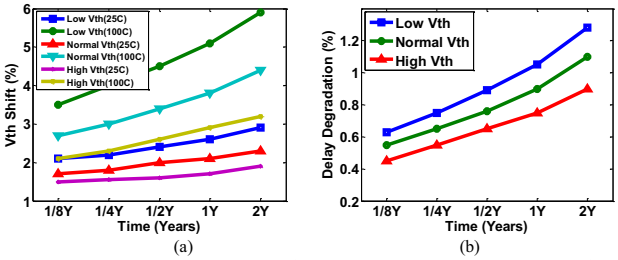
(a) (b) (c)

Figure 1: **a)** Typical transistor threshold voltage standard deviation (σV_{th}) normalized to the threshold voltage (V_{th}) for several technologies (extracted from [18]) **b)** Trend of σV_{th} in a typical transistor for different technologies as a result of different process-induced intrinsic variations like random dopant fluctuation (RDF), line-edge roughness (LER), and oxide thickness fluctuation (OTF) (extracted from [19]) **c)** Mean (μ) and normalized standard deviation (σ/μ) of inverter delay under random process variations for different technologies (extracted from [19]).



(a) (b)

Figure 2: **a)** V_{th} variation as a function of temperature for a typical transistor in fast (FF), typical (TT) and slow (SS) process technology corners (extracted from [20]) **b)** Reference voltage in different process corners using circuit proposed in [20].



(a) (b)

Figure 3: **a)** Percentage of V_{th} shift in a typical PMOS transistor for three technology corners: low, nominal, and high V_{th} at 25°C and 100°C **b)** Percentage of delay degradation of a five-stage ring oscillator for three different V_{th} corners. Low V_{th} circuit shows more degradation compared to high V_{th} circuit (extracted from [11])

Furthermore, how variations and degradation at the device-level parameters can affect system-level parameters and how they can affect reliability estimations during the operational life are also discussed in section II. The proposed workflow of reliability estimation during the operational life for achieving high system dependability and the corresponding simulation results are presented in sections III and IV respectively. Conclusions are given in section V.

II. Reliability Estimations during Operational Life

For a long time, different analytical approaches have been thoroughly investigated in literature to examine the circuit-level aging effects based on device-level (transistor) models [5, 12, 13]. These analytical approaches also include some indirect ways to estimate circuit-level reliabilities at the *design time*. For example, the maximum digital circuit delay degradation in [14], the maximum frequency (F_{max}) degradation of ring oscillators in [15], and total quiescent supply current (I_{DDQ}) in [16] have been used to indicate the reliability hazards of digital circuits. Similarly, a reliability-analysis technique has been proposed in [17] by lifetime yield prediction of analog circuits.

In order to estimate the system reliability during its *operational life* it is required to investigate *runtime* reliability estimation techniques. Figures 1(a), 1(b), and 1(c) show respectively variations in the threshold voltage being a device-level parameter due to technology-node shrinkage [18], intrinsic process variations, and the corresponding variations in an inverter delay [19] being a system-level parameter. Similarly, variations in the threshold voltage due to different process corners, and the corresponding variations in the output voltage, a system-level performance parameter, of a reference voltage generator are shown in Figures 2(a) and 2(b) [20] respectively.

Bias temperature instability (BTI) is another cause of introducing variations in the threshold voltage (V_{th}). It is noted that these BTI degradations further depend on the initial threshold voltage ($V_{th}(t_0)$) [11]. Figures 3(a) and 3(b) show respectively the variations in the NBTI induced threshold voltage of a PMOS transistor at three different technology corners and the corresponding variations in the delay, a system-level parameter, of a five-stage ring oscillator as a function of stress time [11].

These facts show that the system-level parameters are indeed linked to the device-level parameters. Therefore, process variations as well as aging effects will have effect on the device-level parameters (e.g. V_{th}), and similar variations could be expected in the system-level parameters (e.g. delay Fig. 1(c) and 3(b), reference voltage Fig. 2(b)) being connected to device-level parameters. Furthermore, reliability of a system can be defined ***quantitatively*** as the total time for which its performance parameters remain within the designed specifications. This provides a solid foundation that any anticipated change from the designed specifications of its system-level performance parameters will provide an estimate of its reliability. These changes could be a result of a mix of process variations and/or aging effects. Therefore, monitoring

variations in system-level performance parameters at the very start and during the operational life will provide the basis for an estimate of the process variations and the aging effects respectively and hence a technique to estimate the reliability of the system.

The selection of system-level performance parameters will be application dependent and can be divided into different categories based on their sensitivity to aging effects and process variations. The most sensitive system-level performance parameter(s) acquired via aging simulations at the design time can be selected as the best indicator(s) for reliability estimations. Furthermore, these reliability estimations can be used for the system dependability enhancements via repair as discussed in the next section. Let a system-level performance parameter 'P' be the most sensitive to aging effects and process variations. And let P_{min} and P_{max} represent the designed functional specification boundaries for performance parameter P $(i.e.\ P_{min} \leq P \leq P_{max})$. Then at any point in time 't' the time it will take to move 'P' beyond specifications or the time before failure (TBF), defined as the functional failure, can be regarded as a ***quantitative*** mean of estimating the reliability at that particular time. The larger the remaining time before it fails, the higher will its reliability be and vice versa. Therefore, the TBF has been used as a reliability estimator in this research. Suppose at time 't', the performance parameter 'P' has been degraded from $P(t_0)$ to $P(t)$. Assuming a linear degradation, the time it will take to move 'P' beyond its specifications is called its reliability $R(t) = TBF(t)$ at time 't'. It will be given by:

$$TBF(t) = R(t) = \left[\frac{P_{max} - P(t)}{P(t) - P(t_0)}\right] * t \quad (1)$$

in case 'P' has increased during the time interval '$t - t_0$', and will be given by:

$$TBF(t) = R(t) = \left[\frac{P(t) - P_{min}}{P(t) - P(t_0)}\right] * t \quad (2)$$

in case 'P' has decreased during the time interval '$t - t_0$' respectively.

Furthermore, from Figures 1(a), 1(b), 2(a), and 3(a) it can be concluded that the initial value and time dependent behavior of V_{th} is [9]:

$$V_{th}(t) = V_{th}(t_0) + At^n \quad (3)$$

and $$A = f(V_{DS}, V_{GS}, V_{th}(t_0), T, W, L, RDF, OTF, LER, FF, TT, SS) \quad (4)$$

Here, $V_{th}(t_0)$ is the initial threshold voltage (for an unstressed device), 't' is the time and 'n' is a degradation parameter (about 0.18 for NBTI [9]). 'A' is a function of geometrical (e.g. length L and width W), environmental (e.g. temperature T), and process-related (e.g. random dopant fluctuation RDF) transistor parameters.

These facts show that the system-level parameters (e.g. delay in Fig. 1(c) and 3(b), reference voltage in Fig. 2(b)) are not only connected to device-level parameters (e.g. V_{th}) but also *their degradation rate is dependent on the initial threshold voltage ($V_{th}(t_0)$) values (Fig. 3b).* It means that the system-level parameters of the similar systems will degrade differently. They show different degradation rates and behaviors as they have different $V_{th}(t_0)$ values at the very start as a result of fabrication-related process variations. Therefore in general, the reliability $R(t)$ of the system defined in (1) and (2) will become:

$$TBF(t, V_{th}(t)) = R(t, V_{th}(t)) = \left[\frac{P_{max} - P(t, V_{th}(t))}{P(t, V_{th}(t)) - P(t_0, V_{th}(t_0))}\right] * t \quad (5)$$

in case 'P' has increased during the time interval '$t - t_0$', and will be given by:

$$TBF(t, V_{th}(t)) = R(t, V_{th}(t)) = \left[\frac{P(t, V_{th}(t)) - P_{min}}{P(t, V_{th}(t)) - P(t_0, V_{th}(t_0))}\right] * t \quad (6)$$

in case 'P' has decreased during the time interval '$t - t_0$' respectively. The above equations assume that there is a linear degradation during time interval '$t - t_0$'. In case there are *non-linear degradations*, one can divide the time into 'n' time points ($t_0,\ t_1,\ t_2,\ \ldots\ldots\ t_{n-1},\ t_n$). During each time interval $(t_1 - t_0, t_2 - t_1, \ldots\ldots, t_n - t_{n-1})$ the degradation remains nearly linear. Therefore, (5) and (6) can be rewritten as:

$$TBF(t_n, V_{th}(t_n)) = R(t_n, V_{th}(t_n)) = \left[\frac{P_{max} - P(t_n, V_{th}(t_n))}{P(t_n, V_{th}(t_n)) - P(t_{n-1}, V_{th}(t_{n-1}))}\right] * t_n \quad (7)$$

in case 'P' has increased during the time interval '$t_n - t_{n-1}$', and will be given by:

$$TBF(t_n, V_{th}(t_n)) = R(t_n, V_{th}(t_n)) = \left[\frac{P(t_n, V_{th}(t_n)) - P_{min}}{P(t_n, V_{th}(t_n)) - P(t_{n-1}, V_{th}(t_{n-1}))}\right] * t_n \quad (8)$$

in case 'P' has decreased during the time interval '$t_n - t_{n-1}$' .

III. Proposed Dependability Workflow

The above discussion provides the important information that for estimating the correct reliability of a system based on the degradation of its system-level parameters it will be necessary to regularly monitor and store design as well as initial values of specifications in a database. The initial values at the start will provide information about the process variations whereas the gradual degradation with time will provide information about the aging effects. Keeping this in mind, the suggested workflow shown in Fig. 4 for estimating the reliability during operational life and enhancing system dependability consists of a database of design-stage specifications (e.g. P_{min}, P_{max}, C, TBF_{min} and $MTBF$) for a particular application and a system memory for runtime logged values. The database will also be further stored in the system memory. Further included are the performance monitoring circuit(s) for the potential critical performance parameter(s) (e.g. 'P'). The database of system specifications (parameters) along with measurements of system-level parameters during its operational life will be further used to estimate the reliability $R(t) = TBF(t)$ using (7) and (8).

At the very start of the system, the system will be first put into a test mode to acquire its initial values of performance parameter(s) (e.g. $P(t_0, V_{th}(t_0))$), as a result of process variations, using performance monitoring circuit(s). The next time point 't_1'will be estimated based on the distance it has from the specification boundaries (i.e. P_{min} and P_{max}) and stored values (i.e. C and $MTBF$). This can be expressed as:

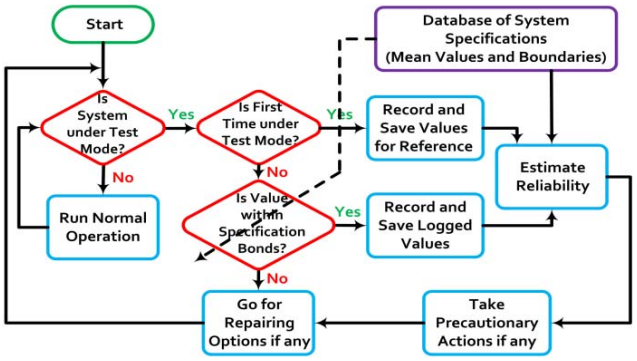


Figure 4: Workflow of the proposed approach for estimating the reliability of a system and taking proper actions for enhancing dependability

$$t_1 = \left[\frac{P_{max} - P_{min}}{C * P(t_0, V_{th}(t_0))}\right] * MTBF \quad (9)$$

Where 'C' is a constant determined from the design-stage reliability simulations for performance parameter 'P' and can be selected in such a way that the degradation in 'P' remains nearly linear during each time interval '$t_n - t_{n-1}$'. At point in time 't_1' the system will be put again in test mode to acquire new values of the performance parameter, as a result of the aging effects, and after that the normal operation will be resumed. These values are then stored in the database along with a time stamp. Reliability ($TBF(t_1, V_{th}(t_1)) = R(t_1, V_{th}(t_1))$) will be estimated using (7) and (8) at this calculated point in time 't_1' by having newly acquired values ($P(t_1, V_{th}(t_1))$) of the performance parameter 'P' and already saved values ($P(t_0, V_{th}(t_0))$) in the database. In the case TBF_{min} represents the minimum value to be monitored for taking repair actions, a decision about digital tuning or replacement can be taken if the estimated reliability ($TBF(t_1, V_{th}(t_1)) = R(t_1, V_{th}(t_1))$) is less than or equal to TBF_{min} (i.e. $TBF(t_1, V_{th}(t_1)) \leq TBF_{min}$). The next point in time for the next acquisition will be calculated based on this new reliability information. That is:

$$t_2 = \left[\frac{P_{max} - P_{min}}{C * P(t_1, V_{th}(t_1))}\right] * TBF(t_1, V_{th}(t_1)) \quad (10)$$

At this new point in time the reliability ($TBF(t_2, V_{th}(t_2)) = R(t_2, V_{th}(t_2))$) and the next point in time 't_3' will be calculated. In this way, this process will continue during its operational life.

Estimating reliability is an important part of this approach. Having this value, proper precautionary actions, like estimating possible actions to prevent failure or minimizing dangers to environment can be taken. Under critical situations, e.g. if the estimated TBF is less than or equal to TBF_{min} (i.e. $TBF(t_n, V_{th}(t_n)) \leq TBF_{min}$), digital tuning or replacement actions of its subsystems could be taken to remain within specification limits of the performance parameters (e.g. P_{min}, P_{max}). In practice, the actual replacement of one sub-block with another redundant sub-block can be achieved by using electronic switches. Anticipating digital tuning and replacement actions in advance based on the regular reliability estimations will reduce the repair time or time-to-repair (TTR).

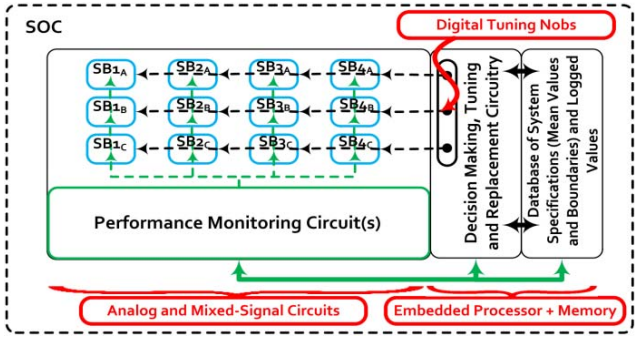


Figure 5: An exemplary system consisting of digitally tunable redundant sub-blocks for running simulations on the proposed workflow in Fig 4.

TABLE 1: Necessary details of $SB1_{(A,B,C)}$ used in the LabVIEW simulations.

Mean value of the designed parameter 'P'	100 a.u.
Allowed boundaries of the parameter 'P'	[90 110] a.u.
Number of redundant blocks available	3
Digital tuning options for the parameter 'P'	8 (3 digital bits)
Digitally tuning range for each digital option	2% of initial value of P
Maximum MTBF for each $SB1_{(A,B,C)}$	3000 hr (for example)
Constant 'C' value	667

In other words the ***maintainability*** of the system can be increased. This means the system will know in advance at what point in time it has to take digital repair actions. Theoretically, by anticipating repair actions in advance, the repair time can be reduced to near zero. Furthermore, ***availability*** of the system at any time t_n will be given by:

$$A(t_n, V_{th}(t_n)) = \frac{TBF(t_n, V_{th}(t_n))}{TBF(t_n, V_{th}(t_n)) + TTR(t_n)} \quad (11)$$

The above equation shows that by reducing TTR near to zero the availability $A(t_n, V_{th}(t_n))$ of the system can be increased to 100% [21]. Therefore, by estimating the reliability of the system during its operational life to remain within its specification boundaries will ultimately increase its ***reliability***, ***maintainability, availability*** and hence the ***dependability*** of the whole system.

IV. Simulations and Results

In order to investigate the proposed idea, a target system consisting of redundant sub-blocks (e.g. $SB1_A$, $SB1_B$, and $SB1_C$ for SB1) each having eight possible digitally tunable options have been considered as shown in Fig. 5. The performance monitoring circuit(s) can monitor the most sensitive performance parameter(s) for estimating reliability of each individual sub-block or of the whole system as shown by vertical dotted lines (green dotted lines in Fig. 5). This further communicates with the decision making, tuning and replacement circuitry for taking necessary digital tuning or replacement actions and with the database for storing performance parameter values. Fig. 6 shows the simulation results of a redundant sub-block ($SB1_{(A,B,C)}$) where a single performance parameter 'P' has been considered most sensitive to aging mechanisms and process variations with different degradation behaviors. Table 1 shows the necessary details of this sub-block (SB1).

In order to simulate a variety of different aging degradation

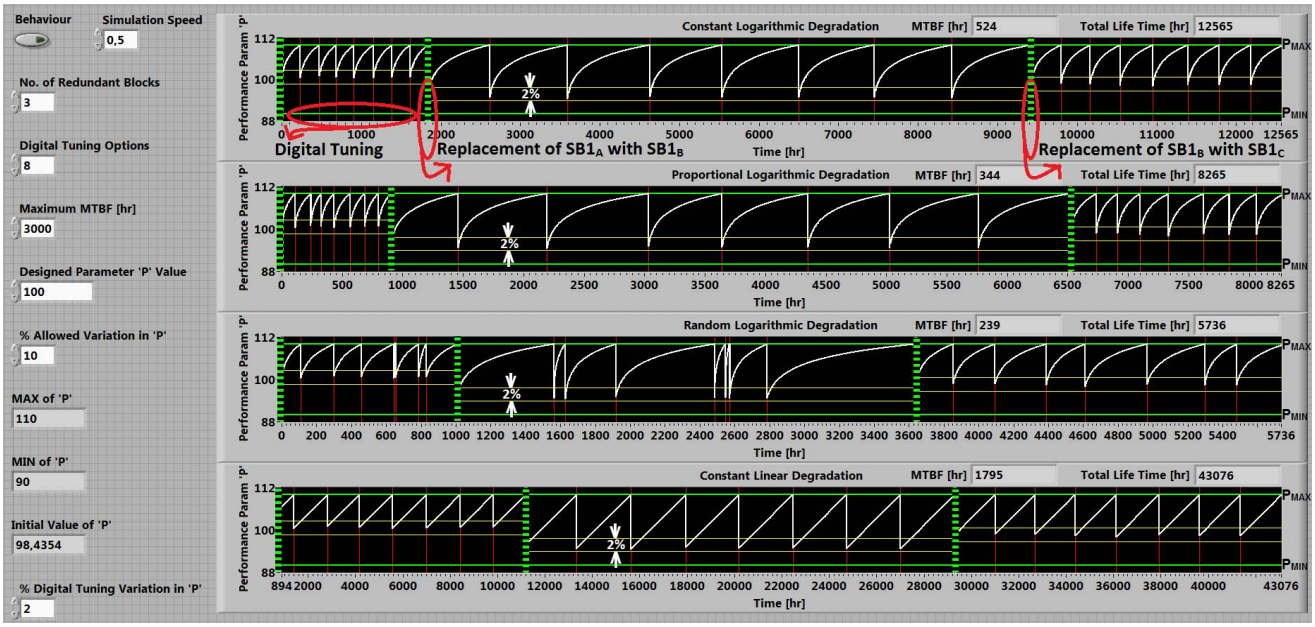


Figure 6: Simulation results of a system consisting of three redundant sub-blocks ($SB1_{(A, B, C)}$). Each sub-block $SB1_{(A, B, C)}$ has eight digital tunable options for performance parameter 'P'. Four different aging degradation possibilities for parameter 'P' has been considered and simulated for same the system with same initial/start values of 'P'. A failure is defined in the case the parameter 'P' goes beyond its defined boundaries (green horizontal lines for P_{min} and P_{max}).

TABLE 2: Numerical results of simulations conducted in Fig. 6. The start value of 'P' for every digital tuning option (i.e. 001-111) lies within 2% of its initial value ($P_{(000)}$). Similarly, the initial value of '$P_{(000)}$' for each redundant sub-block ($SB1_{(A, B, C)}$) lies within the designed specification bounds (i.e. [90 110]). All of these values are randomly selected to show the possible initial value variations due to fabrication-related process variations. Decision times are measured from the beginning of the simulation.

	$SB1_A$ Digital Tuning Values								$SB1_B$ Digital Tuning Values								$SB1_C$ Digital Tuning Values							
	000	001	010	011	100	101	110	111	000	001	010	011	100	101	110	111	000	001	010	011	100	101	110	111
Constant Logarithmic Degradation																								
Start Value of 'P'	100,631	100,474	101,054	100,746	100,435	100,593	100,692	100,770	95,736	94,774	94,540	95,090	94,828	94,922	94,774	94,715	98,693	98,798	98,735	98,379	98,076	98,545	98,469	98,435
Start Time [hr]	0	232	473	680	904	1147	1380	1607	1830	2607	3584	4617	5524	6489	7433	8410	9401	9779	10147	10521	10930	11371	11763	12163
Decision Time [hr]	231	472	679	903	1146	1379	1606	1829	2606	3583	4616	5523	6488	7432	8409	9400	9778	10146	10520	10929	11370	11762	12162	12565
TBF [hr]	231	240	206	223	242	232	226	222	776	976	1032	906	964	943	976	990	377	367	373	408	440	391	399	402
Proportional Logarithmic Degradation																								
Start Value of 'P'	100,631	100,474	101,054	100,746	100,435	100,593	100,692	100,770	95,736	94,774	94,540	95,090	94,828	94,922	94,774	94,715	98,693	98,798	98,735	98,379	98,076	98,545	98,469	98,435
Start Time [hr]	0	110	240	322	428	562	681	792	896	1450	2184	3023	3629	4340	5012	5746	6506	6720	6895	7078	7315	7604	7815	8038
Decision Time [hr]	109	239	321	427	561	680	791	895	1449	2183	3022	3628	4339	5011	5745	6505	6719	6894	7077	7314	7603	7814	8037	8265
TBF [hr]	109	129	81	105	133	118	110	103	553	733	838	605	710	671	733	759	213	174	182	236	288	210	222	227
Random Logarithmic Degradation																								
Start Value of 'P'	100,631	100,474	101,054	100,746	100,435	100,593	100,692	100,770	95,736	94,774	94,540	95,090	94,828	94,922	94,774	94,715	98,693	98,798	98,735	98,379	98,076	98,545	98,469	98,435
Start Time [hr]	0	110	298	455	641	650	782	823	1000	1554	1619	1907	2473	2535	2558	2772	3623	3837	4077	4370	4593	4946	5277	5459
Decision Time [hr]	109	297	454	640	649	781	822	999	1553	1618	1906	2472	2534	2557	2771	3622	3836	4076	4369	4592	4945	5276	5458	5736
TBF [hr]	109	187	156	185	8	131	40	176	553	64	287	565	61	22	213	850	213	239	292	222	352	330	181	277
Constant Linear Degradation																								
Start Value of 'P'	100,631	100,474	101,054	100,746	100,435	100,593	100,692	100,770	95,736	94,774	94,540	95,090	94,828	94,922	94,774	94,715	98,693	98,798	98,735	98,379	98,076	98,545	98,469	98,435
Start Time [hr]	0	1407	2836	4178	5567	7002	8414	9811	11196	13336	15620	17940	20177	22453	24715	26999	29292	30989	32670	34360	36104	37893	39612	41342
Decision Time [hr]	1406	2835	4177	5566	7001	8413	9810	11195	13335	15619	17939	20176	22452	24714	26998	29291	30988	32669	34359	36103	37892	39611	41341	43076
TBF [hr]	1406	1428	1341	1388	1434	1411	1396	1384	2139	2283	2319	2236	2275	2261	2283	2292	1696	1680	1689	1743	1788	1718	1729	1734

behaviors (linear and non-linear) for performance parameter 'P', which may or may not be a function of initial values due to fabrication-related process variations, four different degradation behaviors have been considered. The *Logarithmic Degradation* represents a degradation rate which has a purely constant logarithmic behavior independent of initial value of 'P'. The *Proportional Logarithmic Degradation* represents a degradation rate which has a logarithmic behavior which depends on the initial value of 'P'. Initial value of 'P' close to 'P_{min}' will result in a slow logarithmic degradation rate and vice versa. Similarly, the *Random Logarithmic Degradation* represents the degradation rate which has a random (slow or fast) logarithmic behavior and is independent of the initial value of 'P'. Furthermore, the *Constant Linear Degradation* represents the degradation rate which has a constant linear behavior independent of initial value of 'P'.

The outer horizontal lines (green) in Fig. 6 show the allowed boundaries of parameter 'P' (i.e. P_{min} and P_{max}) whereas the inner horizontal lines (yellow) show the range of possible initial values of digital tuning options (i.e. 2% of initial value of P). The vertical lines (red) show the time points where the digital tuning options have been used for tuning parameter 'P' back to its allowed boundaries. Similarly, the dotted vertical lines (green) show the time points where $SB1_A$ has been replaced with a redundant sub-block (i.e. by $SB1_B$ or $SB1_C$). The initial/start value of each redundant sub-block and each digitally tuned value of sub-block has been randomly selected from the allowed parameter 'P' range (green or outer horizontal lines for P_{max} and P_{min}) and possible digitally tunable range of each selected sub-block (yellow or inner horizontal lines for start values within 2% of initial value of 'P') respectively. *Randomly selected values are used to show*

the possible initial value variations due to fabrication-related process variations.

Fig. 6 and Table 2 provides an important information that by considering different degradation behaviors (linear and non-linear) of the performance parameter 'P', with the same initial value (i.e. the starting value of 'P' is same for each degradation behavior as shown in Table 2), the total life time of each system is different. The system with constant linear degradation behavior for 'P' has the maximum lifetime (i.e. 43076 hours) whereas the system with the random degradation behavior for 'P' has the minimum lifetime (i.e. 5736 hours).

It is also obvious from Table 2 that different initial values of parameter 'P', with different degradation behaviors, will give completely different behaviors of the same system. It becomes quite complicated to decide at which time one has to start digital tuning or replacing the sub-block for enhancing its reliability or availability. For example the sub-block $SB1_A$, with a *constant logarithmic degradation* behavior for parameter 'P', that was expected to be digitally tuned after every 231 hours (blue box in Table 2) is no longer valid for other digital tunings. It is further digitally tuned after 240, 206, 223, 242, 232, 226, and 222 hours respectively. Similarly, the first complete replacement of sub-block (i.e $SB1_A$ with $SB1_B$) has been done after 1829 hours (green box in Table 2) while the second complete replacement of sub-block (i.e $SB1_B$ with $SB1_C$) has been done after 7571 (9400-1829=7571) hours. This is quite large value as compared to the first replacement time. Especially, it becomes extremely complex to decide about the right time of repair or replacement based on the initial reliability calculations at the design time if the performance parameter 'P' has a random degradation rate. Some of these exceptions are also highlighted by dotted boxes (red) in Table 2. *This necessitates the use of the proposed workflow of Fig. 4 for regularly estimating reliability during operational life and enhancing system dependability by taking proper actions at the proper time.*

This is what has been done in the current simulation shown in Fig. 6. The simulation starts with the redundant sub-block $SB1_A$.The performance monitoring circuit regularly monitors the performance parameter 'P' during the regular test mode operation and communicates with the database for storing performance parameter 'P' values. These values are then used to estimate its reliability using (7) and (8). This is further used for taking necessary digital tuning or replacement actions by the decision making, tuning and replacement circuitry at the right time (i.e. if $R(t) = TBF(t) \leq TBF_{min}$) before the performance parameter 'P' moves beyond its defined specifications (i.e. beyond P_{min} and P_{max}). Initially, a sub-block (e.g. $SB1_A$) will be digitally tuned via digital knobs to remain within defined specification boundaries (i.e. P_{min} and P_{max}) and in case the digital tuning options are no more available for this sub-block ($SB1_A$), it will be replaced with a redundant sub-block (e.g. $SB1_A$ with $SB1_B$).

It is also clear from these simulations that by incorporating the proposed strategy the system can be better managed in real time. That is at what time the decision making, tuning and replacement circuitry has to digitally tune or replace the sub-blocks for increasing its reliability and availability respectively. Therefore, by having proper maintainability with reduced repair time and increased reliability and availability the dependability of the system will increase.

In practice, the resolution or monitoring accuracy of the performance monitoring circuits and the corresponding digital tuning accuracy will play an important role in the overall effectiveness of the presented technique. Furthermore, the performance monitoring circuits, the switches, and the redundant sub-blocks will impose serious area overheads on one side while on the other side they are essential for better dependable design. Similarly, the reliability of the digital circuit, for decision making and digital repair, may introduce some delay or cause slower processing during repair. However, the overall impact can be ignored by taking repair actions well in advance before the system goes beyond its design specifications.

V. CONCLUSIONS

In this paper, we investigated how regularly estimating reliability during operational life of a system can be used to enhance system dependability. Variations and degradations in the system-level parameters having a direct influence from the device-level parameters have been used to estimate the reliability during the operational life of a system. These degradations further depend on the initial values of parameters due to fabrication-related process variations and the architecture of the system. This makes the reliability estimation a complicated process during operational life. By using the conventional techniques of estimating the reliability of a system at the design stage, one cannot handle these real-time variations that are a function of initial values. Therefore, a workflow based upon regular monitoring and storage of the system-level parameters is proposed for estimating reliability of these systems during operational life. These reliability estimations are further used for intelligently making decisions on digital tuning and replacement mechanism. An example target system has been simulated in a LabVIEW environment. These simulations validate the proposed idea that by regularly monitoring the most sensitive performance parameter(s) with any degradation behavior (linear or non-linear) to aging effects and intelligently taking the right decisions at the right time the system dependability during its operational life can be better managed and enhanced. The price paid is in terms of higher area overheads. However, it is essential for a better dependable design.

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