Network Initialization in a Switch-Level Simulator

A.J. van Genderen
Department of Electrical Engineering
Delft University of Technology
2600 GA Delft, the Netherlands

Abstract

In some cases, it can be a cumbersome task to initialize the nodes in a network that is simulated with a switch-level simulator. In this paper, we describe how nodes in a switch-level network are initialized via (1) user-defined initialization and (2) random initialization. The new initialization algorithms have been implemented in the switch-level simulator SLS.

1 Introduction

Switch-level simulators are widely used to simulate the logic and timing behavior of large digital MOS circuits. During simulation, an important problem can be the initialization of the network. In general, a circuit should be designed such that no initialization is necessary for the circuit other than via its input terminals. However, for simulation, it may be necessary to initialize also the internal nodes of the network.

An example of a situation where an initialization of the internal nodes is required is when an initial design of a memory circuit is simulated that has not yet a reset input. Another example is when, for efficiency reasons, a circuit is simulated starting from a particular state that is in fact only reached after many clock periods. Yet another reason may be that a user wants to simulate the power-on effect of the circuit, i.e. some nodes in the circuit receive a value that is O or I but that is not a priori known.

2 User-defined Initialization

One way to initialize nodes in a switch-level network consists of an explicit definition of the state of these nodes by the user. This approach is useful if it is known which nodes must be initialized and at which state.

An explicit initialization is achieved in the switch-level model [1] by temporarily defining these nodes as input nodes, applying the desired logic state, and next redefining these nodes as normal nodes.

3 Random Initialization

A second method consists of performing a random initialization of the network. This option is used to simulate the power-on effect, or when the first method does not work due to a large number of internal nodes and/or because the nodes are difficult to select (e.g. because a large circuit is simulated that was obtained via layout-to-circuit extraction).

With this method, it is important that first the circuit parts are initialized that are input to other circuit parts. This is achieved in the switch-level model by considering the subdivision of the network into its channel graphs and by initializing these channel graphs in a depth-first order [2].

4 Final Remarks

The initialization algorithms have been implemented in the switch-level simulator SLS [1]. They allow to find a consistent initial network state in all cases, using explicit initialization and/or using random initialization. The SLS simulator is available, under the terms of the GNU license, via anonymous ftp from //dutentb.et.tudelft.nl:ftp/pub/sls.

References

[1] A.J. van Genderen, "SLS: An Efficient Switch-Level Timing Simulator Using Min-Max Voltage Waveforms," *Proc. VLSI 89 Conference*, Munich, pp. 79-88, Aug. 1989.

[2] R. Sedgewick, *Algorithms,* Addison-Wesley, Reading, Massachusetts, 1984.