An audio FIR-DAC in a BCD process for high power Class-D amplifiers

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Abstract:

A 322 coefficient semi-digital FIR-DAC using a 1-bit PWM input signal was designed and implemented in a high voltage, audio power Bipolar CMOS DMOS (BCD) process. This facilitates digital input signals for an analog class-D amplifier in BCD. The FIR-DAC performance depends on the ISI-resistant nature of this PWM-signal. An impulse response with only positive coefficients was chosen, because of its resistance to deadzone and mismatch. With a DAC current of 0.5 mA, the dynamic range is 111 dB (A-weighted), with SINAD = 103 dB (A-weighted). The current consumption is 1mA for the analog part and 4.8 mA for the digital part. The power consumption is 29 mW at V_{dd} = 5 V and the chip area is 2 mm^2 including the reference diode that can be shared by more channels.

1. Introduction

Class-D amplifiers are replacing the traditional class-AB amplifiers in many new applications. Multichannel, high power sound is demanded by applications like DVD players and Flat TV's and for class-AB amplifiers the available space for the heatsink is often not sufficient. New BCD processes are very wel suited for the design of high power class-D amplifiers but the CMOS feature size in these processes is large (1.0 µm) and the speed is low compared to state-of-the-art CMOS. Despite these drawbacks, it is desirable to facilitate digital input signals. The best audio quality can be achieved if a class-D amplier with feedback and analog input signal is used. Compared to digital class-D amplifiers, analog class-D amplifiers have a lower distortion and a much better Power Supply Rejection Ratio.
In figure 1 the combination of a class-D amplifier with a one-bit ΣΔ-DAC is shown. To sufficiently attenuate the quantization noise a 3rd order Low Pass Filter (LPF) has to be added. The noise and the distortion of this filter should be low, so large on-chip capacitors are needed.

Figure 1: One bit ΣΔ-DAC for class-D amplifier

The area per channel would be about 2 mm^2 for CD quality audio. Additional measures must be taken to reduce Intersymbol Interference (ISI). Return to zero coding is a solution to this at the price of a lot of extra transitions and a proportional increase of the noise in the audio band [1].
An alternative for a one-bit ΣΔ-DAC is a multibit ΣΔ-DAC, for instance with a resolution of 5 bits. Then quantization noise will decrease with about 30 dB, which is still too much noise for the class-D amplifier. Furthermore, low distortion requires a 16-bit precision. Insufficient matching accuracy necessitates some kind of calibration or Dynamic Element Matching (DEM) [2]. The DEM solution has a high digital complexity and at least a 1st order analog filter would still be needed. In this paper we introduce a solution for ISI and virtually distortionless low-pass filtering, without the need for external components or filters, by using a FIR-DAC.

2. System Considerations

ISI is decreased or even completely avoided if the number of signal transitions is kept constant. A Pulse Width Modulated (PWM) signal can be used for this. Figure 2 shows the block diagram of our 1-bit ΣΔ modulator that is controlled in such a way that the output signal behaves like a digital PWM signal.

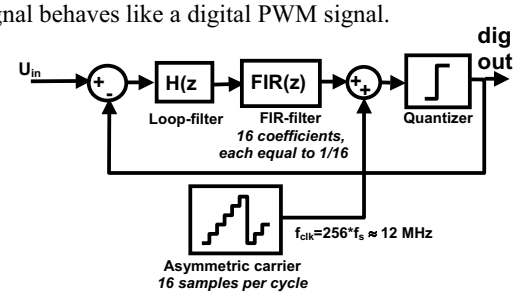

Figure 2: One-bit ΣΔ PWM modulator

It differs from a standard ΣΔ modulator in two ways. First a digital 16 step sawtooth is added to the output signal of the loopfilter to force the PWM frequency regime. Second the loopfilter is cascaded with a 16-tap unitary FIR interpolation filter to improve loop stability. This filter has its first zero located at the PWM frequency. The PWM signal has a 4-bit time resolution, coresponding to 16 discrete pulsewidths. With a PWM frequency of 16 f_s the frequency in the modulator loop becomes 256 f_s. A PWM resolution of 4 bit means that there is still a lot of quantization noise. With the moderate 16 times of oversampling a digital 5th order loopfilter is needed to keep the noise in the audioband sufficiently low. The multibit behavior of the PWM

coder has a positive effect on the loop stability. Therefore, aggressive noise-shaping can be used, while the modulator is still inherently stable up to a modulation depth of 85%. State-limiters inside the loop-filter enable nearly 100% modulation depth. In figure 3 the block diagram of the complete DAC is shown. The input signal is a 1 f_s digital audio signal e.g. from a CD player. First the signal is upsampled to 4 f_s with a high-order interpolation filter. Next, the signal is upsampled to 256 f_s by a simple zero-order hold function that generates the input signal for the modulator. The FIR-DAC performs the D/A conversion and low pass filtering simulaneously.

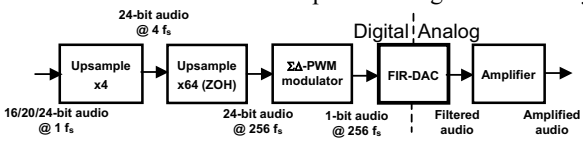

Figure 3: Block diagram of the total DAC system

The block diagram of the FIR-DAC is shown in figure 4. It consists of a digital delayline for the PWM bitstream. Each delayline tap is connected to a one-bit DAC. This DAC is a switchable differential current source. The value of the current is proportional to the coefficient value that is needed to get the intended filter characteristics.

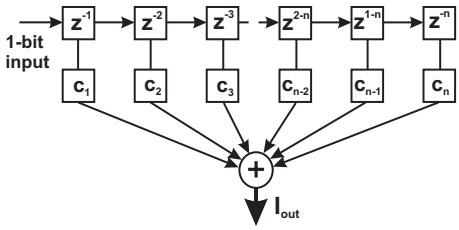

Figure 4: FIR-DAC block diagram

The starting point of the filter is a 128 tap moving average FIR filter. The noise attenuation of this filter is moderate. For this reason 3 filter sections are cascaded. This means that the time domain convolution of the 3 cascades has to be calculated. The resulting filter has a bell-shaped impulse response of 3x128-2 = 382 taps. However, for implementation reasons, the ratio between the smallest and the biggest coefficient is limited to 25. Smaller coefficients are left out of the filter, introducing a deadzone and reducing the filter length to 322 taps. A positive coefficient filter is resistant to this deadzone, whereas a filter with a sin(x)/x impulse response is highly sensitive to it. This resistance to deadzone and its much shorter length are the reasons to use a positive coefficient filter, despite a less ideal transition band.

An important observation is that all separate one bit DACs work in parallel. A one-bit converter produces zero distortion, so the summation of the independent output signals does not add any distortion by itself. The filter action comes from the summation of delayed (and weighted) versions of the same output signal. Errors in the coefficient weights only influence the filter characteristic, mainly in the stopband. The passband of positive coefficient FIR filters shows some attenuation at higher frequencies that must be compensated for in the preceding signal processing.

In figure 5 the spectrum of a 10 kHz signal at the output of the modulator is shown in light grey. The peaks in the out of band noise spectrum represent the PWM carrier frequency and its harmonics. The black spectrum includes the filter action of an ideal FIR-DAC and the dark grey spectrum is that of a non-ideal FIR-DAC. The noise attenuation by the FIR-DAC is sufficient for a class-AB analog amplifier or a class-D amplifier with analog feedback. The total noise power is about 60 dB lower than the maximum audio signal and the amplifier will contribute some extra noise attenuation due to its limited bandwidth.

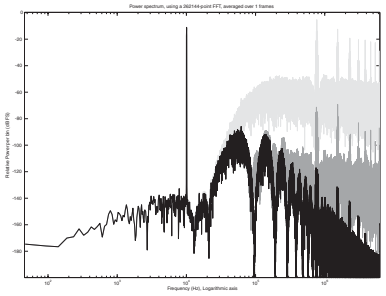

Figure 5: Spectrum with 10 kHz tone at the modulator output (light grey), at the output of a FIR-DAC with deadzone and mismatch (dark grey) and an ideal FIR-DAC output (black)

3. Filter Coefficient Accuracy & Noise

One of the design targets was to minimize area and power consumption for a given level of performance. To accurately balance the trade-offs, an analytical model was developed that allows optimization of both area and power, given mismatch and noise requirements.

3.1 Linear Width Scaling

The multiplication factors of the filter coefficients are implemented as single-transistor current sources (M_{tail} in figure 7). To minimize mismatch of the coefficients, only the widths of the current source transistors are proportionally scaled to match their intended current values. The smallest coefficient has a width W_{min}, the smallest transistor width in the BCD process. The combined width of all tail current sources W_{tot} is now fixed by the sum of the coefficient values of the filter.

3.2 Thermal Noise

The thermal white Gaussian noise of the delayline tail current sources determines the dynamic range of the FIR-DAC. Since this noise is uncorrelated for all 322 taps of the filter, the variances of the noise contributions of each of the current sources can be added. Therefore, all tail current sources are modelled as one large equivalent transistor, with an area A_{tot} equal to the sum of the sizes of all tail current sources.

Using standard CMOS transistor equations for noise density and saturation current, it is possible to derive a

formula (eq. 1) that equates the required active area A_{tot} and current I_{tot}, for a certain signal-to-noise ratio (SNR).

$$A_{tot} = \frac{128\mu C_{ox}\left(kT\gamma\Delta f 10^{SNR/10}\right)^2 W_{tot}^2}{I_{tot}^3} \qquad \text{Eq. 1}$$

3.3 Mismatch & 1/f-noise

Mismatch of the tail current sources results in a suboptimal filter characteristic and thus reduced out of band noise suppression. The extent of mismatch is mainly determined by the area of the devices and to a lesser extent by their currents. Because of the relatively low values for V_{gt}, V_t-mismatch dominates over -mismatch. Given a mismatch specification, the V_t-mismatch equation from [3], results in a relation between V_{gt} and the required active area for the smallest transistor A_{min}. Using the standard saturation current equation for CMOS-transistors, V_{gt} can be removed from the formula. Upscaling the active area and current to A_{tot} resp. I_{tot} results in eq. 2. This is again a relation between required total active area and total current, but now given a mismatch specification for the *smallest* current source I_{min}. For this filter $\sigma(I_{min})/I_{min} = 0.05$ is sufficient.

$$A_{tot} = \frac{W_{tot}\sqrt{2\mu C_{ox} W_{tot}/W_{\min}}}{\sigma\left(I_{\min}\right)/I_{\min}} \cdot \frac{1}{\sqrt{I_{tot}}} \qquad \text{Eq. 2}$$

1/f-noise is implicitly included in the mismatch equations, since they both scale similarly with area. It is not explicitly included in the analysis, because 1/f-noise is only present for large input signals. At small input signals, 1/f-noise is modulated with the PWM-carrier to 16 f_s. It does not influence the dynamic range, but only the SINAD.

3.4 Area / Current Trade-off

In figure 6, equations 1 and 2 visualize that required area can be exchanged for current, while continuing to meet specifications for SNR and mismatch (figure 6). It is evident from figure 6 that down to 0.18mm^2, it is very advantageous to decrease the required area at the expense of increased current.

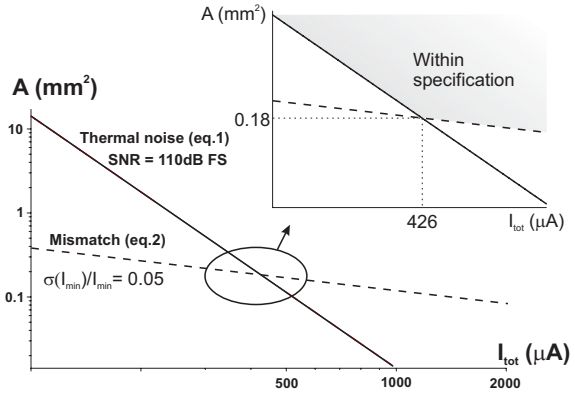

Figure 6: Required area and current to meet a given SNR and mismatch. The SNR on the solid line is exactly 110 dB FS, whereas the mismatch of the smallest coefficient is 0.05 on the dashed line.

Below 0.18 mm^2, decreasing the area requires a quadratic current increase to remain within specification. An area of 0.18 mm^2 and a current of 426 µA are a good trade-off between area and power consumption. Because accurate mismatch data was unavailable at the time, the active area was doubled to 0.36 mm^2 by doubling the length of all current source transistors to L = 58 µm.

4. FIR-filter Implementation with Dynamic Delayline

A dynamic delayline is used to ripple the digital PWM-signal through the filter and to control the differential outputs. The implementation for one coefficient is depicted in figure 7.

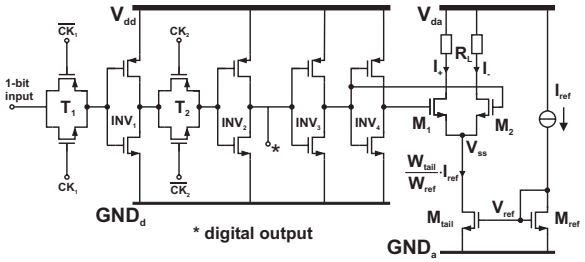

Figure 7: Implementat. of 1 FIR-DAC coefficient using a dynamic delayline. M_{ref} can be shared by mult. chan's.

Two non-overlapping clock pairs control the transmission gates, while maintaining data integrity. Clock signal transitions cause glitches at the analog output through the overlap capacitances and channel charge of the transmission gate transistors. Due to the nature of the PWM-signal, static glitches in the output current only produce a DC-offset in the output signal. To also prevent this small DC-offset from occurring in the output signal, two buffer inverters INV_3 and INV_4 are inserted. Another source of glitches is the differential pair that dumps channel charge into the analog output. As this cannot be prevented, minimum sized transistors are used.

Through $V_{gt,}$, reference transistor M_{ref} influences the 1/f-noise floor. To keep its 1/f-noise contribution low, M_{ref} is given an active area equal to A_{tot}.

5. Automatic Layout Generation

For a semi-digital filter of 322 coefficients, a manual layout is time consuming, so it was generated automatically. A layout of the circuit of a single coefficient was made and the width of the tail current source was parameterized. Precautions are taken to prevent the digital signals from interfering with the analog signals and to facilitate automatic layout generation. The most unconventional precaution is that the tail current source is length folded (U-shaped) to match its dimensions to the delayline and allow simple stacking of the coefficients. This has the additional benefit that all analog signals are separated from the digital signals.

A layout script passes the correct width of the tail current source to the parameterized coefficient layout and places all cells at their correct position. Dummy cells are placed at the boundaries of the delayline to create a homogeneous environment for all coefficients. This script allows a redesign of the FIR-filter within hours, provided that only the filter coefficients are changed.

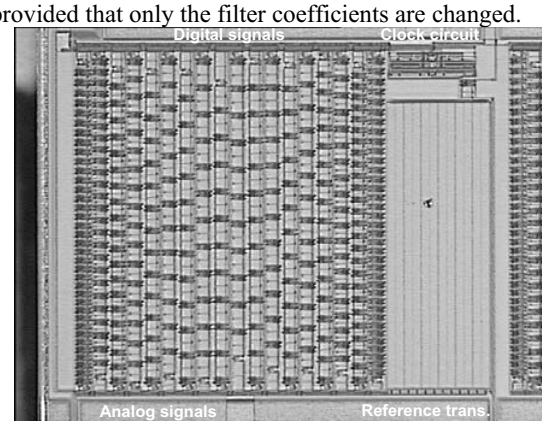

Figure 8: Die photograph of the FIR-DAC

The total layout of the one-channel FIR-DAC, including reference transistor and non-overlapping clock generation circuit amounts to 1.95 mm^2 (figure 8).

6. Measurements

Since the current sources are very long transistors, they exhibit a very linear output resistance, resulting in a good compliance, so no virtual ground is needed at the analog output. For the measurements 2kΩ load resistors (figure 7) were used to do I/V conversion, with V_{da}= 7 V. Figure 9 (left) shows the measured spectrum of the FIR-DAC up to 120 kHz, with an input signal of –60 dB FS. The total out of band noise up to 120 kHz is –66 dB, which matches the simulated amount.

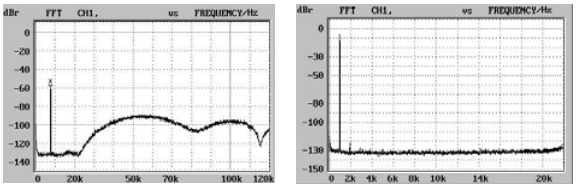

Figure 9: FIR-DAC measured spectrum up to 120 kHz (left) and audio spectrum for –6dB, 955Hz input (right)

Fig. 9 (right) shows that the audio band is nearly free of distortion, with a –114 dB second harmonic for a –6 dB, 955Hz signal. The measured SINAD is shown in fig. 10.

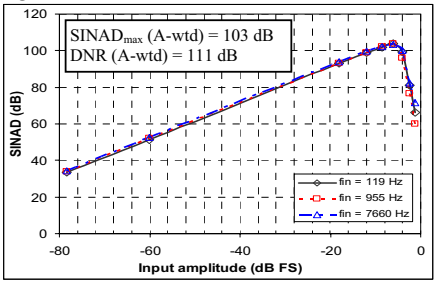

Figure 10: Measured SINAD, I_{ref} = 0.5mA

Below amplitudes of –4 dBFS, the DAC is completely noise-limited with thermal noise limiting the DNR and 1/f-noise that limits the $SINAD_{max}$.
The drop in SINAD for input signals larger than –4 dB FS is caused by the fact that the switching frequency of the PWM-modulator is no longer constant for these signals and ISI is introduced. Table 1 shows the performance overview of the FIR-DAC.

Noise shaping	5^{th} order
Oversampling ratio	256
Dynamic range (I_{ref} = 0.5mA)	108 dB (111 dB*)
$SINAD_{max}$ (I_{ref} = 0.5mA, V_{in} = -6 dB)	100 dB (103 dB*)
Dynamic range (I_{ref} = 1mA)	111 dB (114 dB*)
$SINAD_{max}$ (I_{ref} = 1mA, V_{in} = -6 dB)	103 dB (106 dB*)
Analog power dissipat. (I_{ref} = 0.5mA)	5 mW / chan.
Digital power dissipation (V_{dd}=5V)	23.8 mW / chan.
Die area	1.95 mm^2

Table 1: FIR-DAC performance overview (* A-wtd)

7. Conclusions

A 322 coefficient semi-digital FIR-DAC using a 1-bit PWM input signal was designed and implemented. The FIR-DAC principle depends on the ISI-resistant nature of this PWM-signal. An impulse response with only positive coefficients is chosen, because of its resistance to deadzone and mismatch. Its small non-zero attenuation in the audio band is compensated in the upsample filter. With an analytical model, the optimal area and current requirements were determined, given SNR and mismatch specifications.
Measurements show good agreement with simulation results. Using a reference current of 0.5 mA, the measured A-weighted dynamic range is 111 dB, with the A-weighted SINAD = 103 dB. Including all current sources (0.5 mA), reference current (0.5 mA) and the digital part (4.75 mA), the power consumption amounts to less than 29 mW at V_{dd} = 5 V.
The realisation of the FIR-DAC enables the design of a fully integrated class-D amplifier with digital inputs.

8. Acknowledgements

Marius Rolsma is thanked for his support on circuit simulations and Arnold Freeke for project coordination.

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