A Fully On-Chip LDO Voltage Regulator for Remotely Powered Cortical Implants

Vahid Majidzadeh, Alexandre Schmid, and Yusuf Leblebici
Microelectronic Systems Laboratory (LSM)
Ecole Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland
e-mail: vahid.majidzadeh@epfl.ch

***Abstract*—This article presents a fully on-chip low-power low drop-out (LDO) voltage regulator dedicated to remotely powered wireless cortical implants. This regulator is stable over the full range of alternating current without the need of dedicated active circuitry and increase in ground current. A new compensation technique is proposed to improve PSRR beyond the performance which can be achieved by regular cascode compensation technique. Measurement results show that the regulator has a load regulation of 0.175V/A, a line regulation of 0.024%, and a PSRR of 37dB at 1MHz power carrier frequency. The output of the regulator settles within 10-bit accuracy of the nominal voltage (1.8V) within 1.6µs, at full load transition. The output spot noise at 100Hz and 100kHz are 1.1µV/sqrt (Hz) and 390nV/sqrt (Hz), respectively. The total ground current including the bandgap reference circuit is 28µA and the active chip area measures 290µm×360µm in 0.18µm CMOS technology.**

Keywords— Cortical implants, Inductive Power Coupling, LDO Voltage Regulator, PSRR

I. INTRODUCTION

Minimally invasive monitoring of the electrical activity of specific brain areas using implantable microsystems offers the promise of diagnosing brain diseases, as well as detecting and identifying neural patterns which are specific to some behavioral phenomena [1].

Fig. 1 shows the block diagram of the wireless brain data acquisition system. This system is composed of two main parts, the external reader and the implanted system. The external reader sends power and control information to the implant, whereas the implanted device records the neural activity of a specific area of the brain and sends recorded data back to the external system. The far field controller located in the external module communicates with a host computer or health center for chronical monitoring. The implantable IC includes a power conversion chain (PCC), a data acquisition block, and a transmitter. The PCC, which is enclosed in the shaded box of Fig. 1, is composed of a resonance tank, a rectifier and a voltage regulator. The resonance tank is tuned to 1 MHz, which is the carrier frequency of the inductive link. Further in the chain, the voltage rectifier extracts the DC component from the carrier. Finally, the voltage regulator filters out residual ripples.

The voltage regulator is a critical element of the PCC, which should exhibit high PSRR at carrier frequency, low standby current, low drop-out voltage, monolithic integration,

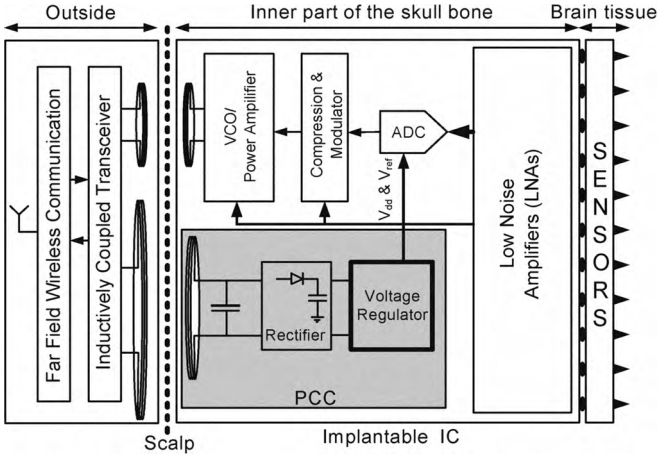

Fig 1. Block diagram of the wireless brain data acquisition system.

and stable operation at low load current. Moreover, the output of the voltage regulator is used as a reference voltage for analog blocks, where fast line and load transient responses are also extremely important. Existing fully on-chip solutions only partially address the aforementioned issues. The DFC technique provides high PSRR (-30dB at 1MHz) in [2], but the regulator is unstable at low load current. In [3] a derivative feedback path guarantees the stability at the expense of additional active circuitry and power consumption (65µA). Cascode compensation with a dynamic bandwidth boosting is proposed in [4], which guarantees stability over the full range of alternating load current, at the cost of increased power penalty.

In this paper, we demonstrate that a symmetric single-ended cascode compensation technique can be used to stabilize the regulator over the full range of alternating load current, thereby eluding the need of a dynamic bandwidth boosting technique [4] or any additional active circuitry [3]. In order to minimize the ground current, optimum pole-zero allocation of the loop gain transfer function has been investigated in time domain rather than in the frequency domain. Moreover, a novel technique is introduced to enhance the PSRR beyond the performance which can be achieved by regular cascode compensation technique.

This paper is organized as follows. Section II describes the proposed voltage regulator, section III presents measurement results, and section IV concludes the paper.

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II. PROPOSED VOLTAGE REGULATOR

Fig. 2(a) shows the architecture of the fully on-chip voltage regulator. No external component is required in this architecture, which reduces the total cost and facilitates the regulator implantation *in-vivo*. The supply voltage denoted as V_{ripple} is provided by the rectifier output, and can be as low as 2.1V. Two-stage cascaded regulation is used to improve PSRR, including two on-chip 100pF MOS capacitors. Both stages are identical; they only differ in reference voltages V_{REF1} and V_{REF2}. A bandgap reference circuit [5] with dynamic start-up and power-on reset circuitry is used to generate the required reference voltages and currents. The bandgap is supplied from the regulator output, which mitigates the need for high PSRR reference voltage generation. Subthreshold MOS transistors are utilized as a feedback network instead of conventional poly or N-well resistors in order to save standby current and silicon area. Indeed, the bandgap current drained through the pass transistors provide enough phase margin to guarantee stability, even at no load condition.

Fig. 2(b) shows the circuit schematic of the first stage with improved frequency compensation and PSRR. The core of the error amplifier consists of a single-ended telescopic cascode amplifier using C_{c1} and M_{2b} as compensation network, which provides a fast derivative feedback path [4]. However, this compensation technique creates asymmetric left-half plane (LHP) and right-half-plane (RHP) zeros with varying load, which degrades the transient response. Dynamic bandwidth boosting proposed in [4] pushes these asymmetric LHP/RHP zeros to higher frequencies when the load current increases, at the cost of increasing ground current. Another solution to avoid these asymmetric zeros consists of canceling the feed-forward path created by the compensation capacitor C_{c1}, using a dedicated active pseudo-differentiator feedback [3] at the cost of increased power consumption. In this work, we propose a simple passive solution making use of C_{c2} as an auxiliary compensation capacitor, without causing any power penalty.

A. Frequency Response

It can be easily shown that without auxiliary compensation capacitor C_{c2}, two asymmetric zero are created in the open loop transfer function:

$$\omega_{z1} \approx -\frac{1}{\tau_{z1}} = -\frac{2g_{m2}}{C_{c1}}, \quad \omega_{z2} \approx -\frac{1}{\tau_{z2}} = \frac{g_{mp}}{C_1} \qquad (1)$$

Where g_{m2} and g_{mp} are the transconductances of M_{2b} and M_P, respectively, and C_1 accounts for the parasitic capacitance at node x_{2b}. Increasing the load current, g_{mp}, the RHP zero and the non-dominant pole formed at the circuit output move to higher frequencies, while the unity-gain frequency and the LHP zero remain almost unchanged. Indeed, the injection of excess phase slows down the transient response. Using C_{c2}=C_{c1}, the resultant transfer function sees its poles remaining unchanged, while zeros move to the following symmetrical locations:

$$\omega'_{z1,z2} = \mp\frac{1}{\tau'_{z1,z2}} = \pm\sqrt{\frac{2g_{m2}g_{mp}}{C_1 C_{c1}}} \qquad (2)$$

It is quite obvious that by increasing the load current, g_{mp}, the zeros are moved to high frequencies at the same rate.

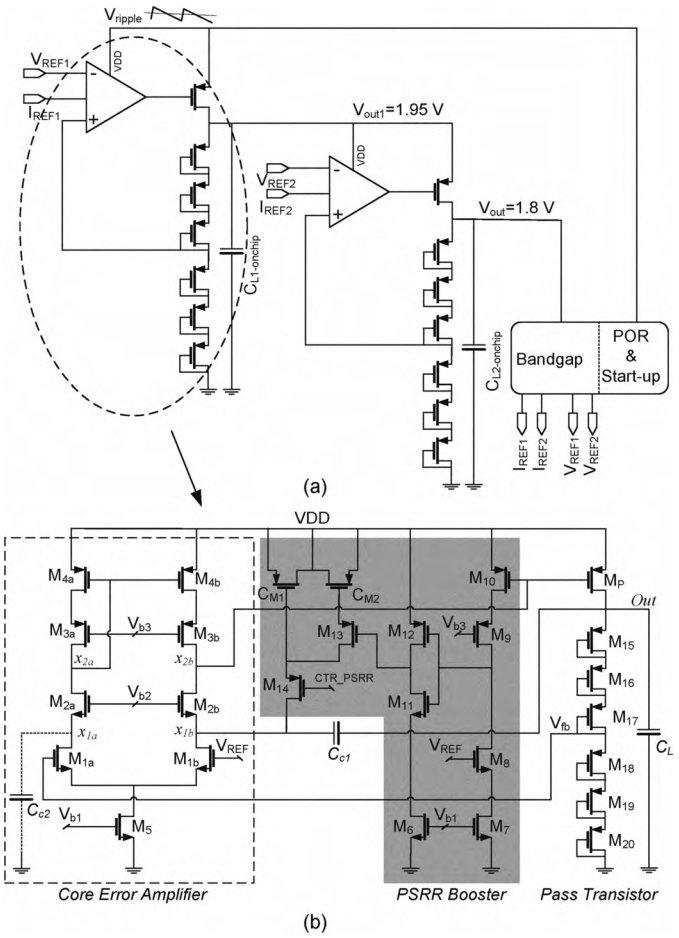

Fig 2. (a) Architecture of the fully on-chip voltage regulator, (b) Circuit schematic of the first stage.

Therefore, increasing the load current has a negligible effect on the phase margin and the related transient response.

B. Design Methodology

As the output of the voltage regulator is used as a reference voltage for analog blocks, the transient response and settling behavior are very important. Special considerations are necessary to find an optimum solution in terms of power and speed. In this study, a time-domain design methodology is developed, which results in minimum power consumption for a desired settling behavior. The closed-loop transfer function is analyzed in order to characterize the transient response of the regulator as follows.

$$H_{cl}(S) = \frac{1}{\beta_0}\frac{\left(1+\tau'_{z1}S\right)\left(1+\tau'_{z2}S\right)}{\left(1+\frac{1}{\omega_{cl}}S\right)\left(1+\frac{2\xi}{\omega_n}S+\frac{1}{\omega_n^2}S\right)} \qquad (3)$$

where β_0 is the feedback factor (here 0.5), τ'_{z1} and τ'_{z2} are time constants related to the symmetric zeros calculated in (2). The extra parameters are expressed in (4), where R_L and C_L are the effective output resistance and capacitance respectively, resistance r_1 is the small-signal output resistance at node x_{2b}, and g_{m1} is the transconductance of $M_{1a,b}$.

$$\omega_{cl} \approx \beta_0 \frac{g_{m1}}{C_{c1}}, \quad \omega_n \approx \sqrt{\frac{g_{m2} g_{mp}}{C_1 C_L}}$$
$$\xi \approx \frac{1}{2}\left(\frac{1}{g_{mp} R_L}\sqrt{\frac{C_1 g_{mp}}{C_L g_{m2}}} + \left(\frac{1}{g_{m2} r_1} + \frac{C_1}{C_{c1}}\right)\sqrt{\frac{C_L g_{m2}}{C_1 g_{mp}}}\right) \quad (4)$$

The settling behavior is characterized by its step response and its associated settling error [6]. The percentage settling error at the regulator output and at a specific time t_s is expressed as follows:

$$e_{ss} = \frac{I_{Full}\Delta t}{C_L V_{out}} \left\{ \begin{array}{l} \dfrac{e^{-\alpha\xi\omega_n t_s}}{1-2\alpha\xi^2+\alpha^2\xi^2} + \dfrac{\alpha\xi e^{-\xi\omega_n t_s}}{1-2\alpha\xi^2+\alpha^2\xi^2} \\ \left[\begin{array}{l} (-2\xi+\alpha\xi)\cos\left(\omega_n t_s\sqrt{1-\xi^2}\right) + \dfrac{1-2\xi^2+\alpha\xi^2}{\sqrt{1-\xi^2}} \\ \sin\left(\omega_n t_s\sqrt{1-\xi^2}\right) \end{array} \right] \end{array} \right\} \quad (5)$$

where $\alpha=\omega_{cl}/\xi\omega_n$, V_{out}=1.8 V is the nominal output voltage, I_{Full}=4 mA refers to the instantaneous full-load current drained from the output, and Δt is the time it takes for the loop to react to changes at the output. A two-step optimization process results in ξ=0.55 and α=1.1 for 10-bit accuracy (0.1% settling error) and minimum power consumption. Given the pole-zero locations, the optimum values of circuit parameters in (4) are derived.

C. *Power Supply Rejection Ratio (PSRR)*

Cascode compensation is not only effective in terms of pole splitting in comparison to Miller compensation, but also is beneficial in terms of PSRR. In this work, a new technique is proposed which improves PSRR beyond the performance which can be achieved by cascode compensation. The circuit is shown in the shaded box of Fig. 2b. The mathematical analysis of voltage gain from power supply to regulator output in (6) shows that the MOSFET compensation capacitor bank C_{M1} and C_{M2} introduces a negative time constant at node x_{2b} and pushes the zero to high frequencies, while it does not affect the main frequency response of the error amplifier.

$$H_{ps}(S) = \frac{V_{out}(S)}{V_{dd}(S)} \approx g_{mp} R_L \frac{\left(1+\dfrac{C_c}{g_{m2}}S\right)\left(1+\gamma' S\right)}{1+a_1 S+a_2 S^2+a_3 S^3} \quad (6)$$

where

$$\gamma' = \gamma - \left(\frac{C_{ps}\cdot g_{mp} r_p}{1+g_{mp} r_p}\right) r_1 + \frac{C_{ps}}{g_{m2}}, \quad \gamma = \left(c_{gdp} + \frac{c_{gsp}}{1+g_{mp} r_p}\right) r_1 \quad (7)$$

Here C_{ps} is the equivalent compensation capacitor formed by C_{M1} and C_{M2}, c_{gsp} and c_{gdp} are the parasitic gate capacitances of the pass transistor M_p. Without compensation (C_{ps}=0 and $\gamma=\gamma'$), the dominant zero is determined by the time constant γ. When the compensation technique is applied, the negative time constant formed by C_{ps} is subtracted from the time constant of the dominant zero. Consequently, the dominant zero is moved to higher frequencies resulting in higher roll-up frequency. The optimum value of C_{ps} tracks the time constant represented by γ under process and load variations, which is expressed in (8). Obviously, the optimum value of C_{ps} depends on the load current. Thus, an adaptive compensation network is required. Its physical implementation is realized by the adaptation circuit $M_{6\text{-}13}$. A very small fraction of the pass current (0.1%) is copied by M_{10} and is compared with the reference current of M_7. If it exceeds 1.6mA, C_{M2} is activated; otherwise only C_{M1} is operational. M_6 limits the maximum short-circuit current of $M_{11\text{-}12}$ to a reasonable value of 1.6μA at the switching point.

$$C_{ps} = \frac{c_{gdp}\left(1+g_{mp} r_p\right)}{g_{mp} r_p} + \frac{c_{gsp}}{g_{mp} r_p} \approx \begin{cases} c_{gdp} & \text{no-load, } g_{mp} r_p >> 1 \\ 2c_{gdp} + c_{gsp} & \text{full-load, } g_{mp} r_p \approx 1 \end{cases} \quad (8)$$

III. EXPERIMENTAL RESULTS

Fig. 3 shows the microphotograph of the active chip area of the monolithic LDO voltage regulator, which is fabricated in a 0.18μm CMOS technology. The active chip area is 290μm×360μm and is dominated by on-chip MOS capacitors.

Fig. 4 shows the measured supply voltage gain at 2mA load current. Without boosting, the PSRR is 33.7dB at 1MHz, while it reaches 37dB when the boosting technique is applied. The measured improvement is 5dB less than the value predicted from simulations, due to extra parasitic capacitance on the gate node of the pass transistor M_p in Fig. 2(b). Fig. 5 shows the measured supply voltage gain versus load current at 1MHz. The PSRR improvement is preserved through the entire dynamic range of the load current by using two-level adaptation, with a switching point centered at 1.6mA.

Fig. 6 shows the measured load transient response when the load current increases from 0mA to 4mA within 200ns. The settling time for 0.1% accuracy is 1.6μs, which enables the use of this unit as a reference voltage for an embedded 10-bit ADC. The measured load regulation is 0.7mV for a 4mA load current. The line transient response is measured for 400 $mV_{p\text{-}p}$ step with 2μs rise and fall time for full load condition. The worst-case line regulation measured in this experiment is 97μV/400mV (0.024%), which is very promising result for burst mode powering applications such as inductively powered circuits.

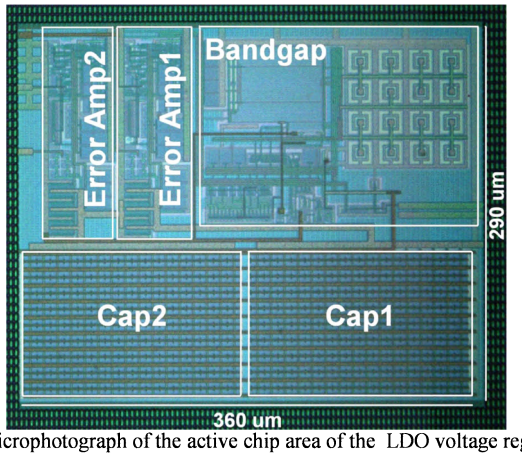

Fig 3. Microphotograph of the active chip area of the LDO voltage regulator.

The measured output spot noise is 1.1μV/sqrt(Hz) at 100Hz and decays to 390nV/sqrt(Hz) at 100kHz. The total current sink from the 2.1V rectifier output is 28μA, where the major contributor is the bandgap reference circuit which consumes 16μA. Table 1 shows the summary of the results and

comparison with the state-of-the-art published on-chip voltage regulators, demonstrating the usefulness of the proposed regulator for implantable applications, where demand low-power and small silicon area, high PSRR, and good line/load regulation.

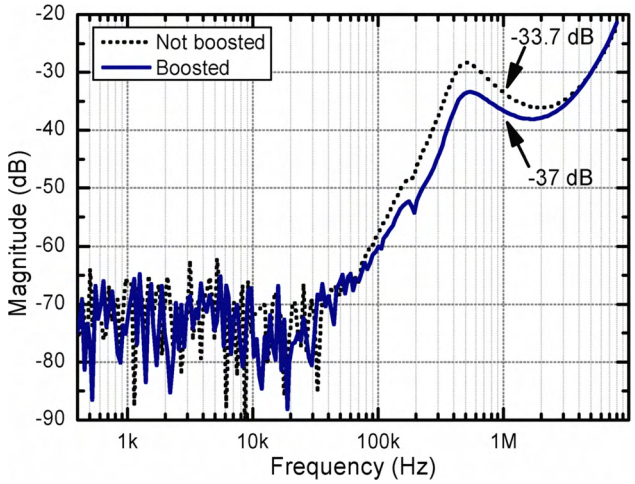

Fig 4. Measured supply voltage gain at 2mA load current.

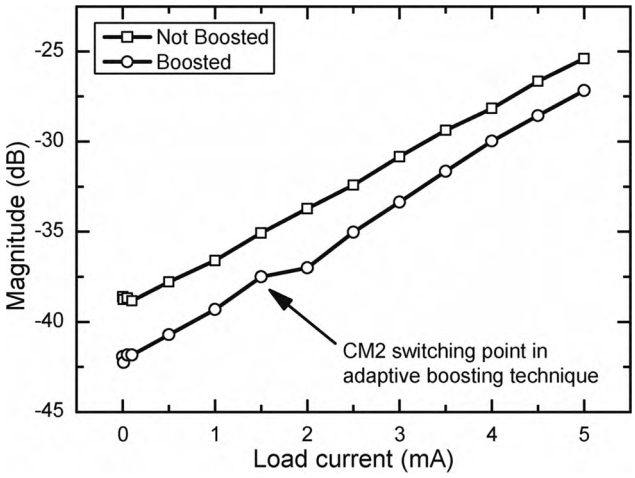

Fig 5. Measured supply voltage gain vs. load current at 1MHz.

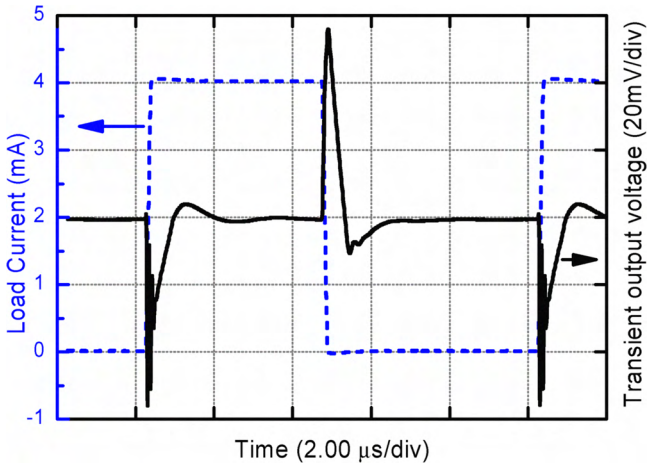

Fig 6. Measured load transient response when load current increases from 0mA to 4mA within 200ns.

TABLE I. SUMMARY OF THE RESULTS AND COMPARISON WITH OTHER WORKS

Parameter		[2]*	[3]	This work
Technology (CMOS)		0.6µm	0.35µm	0.18µm
drop voltage (mV)		200	200	300
Ground Current		38µA	65µA	28µA
Bandgap included		yes	No	yes
Load Regulation		-	40mV/50mA	0.7mV/4mA
Line Regulation ($\Delta V_{out}/\Delta V_{in}$)%		0.15%	0.3%	0.024%
Stability Range		I_L>10mA	Full load	Full load
Settling time		2 µs	15 µs	1.6 µs
Accuracy		Not mentioned	Not mentioned	10-bit
PSRR@	1kHz	-60 dB	-57 dB	-70 dB
	1MHz	-30 dB	-	-37 dB
Spot Noise@	100Hz	1.8 µV/√Hz	4.6 µV/√Hz	1.1 µV/√Hz
	100kHz	380 nV/√Hz	630 nV/√Hz	390 nV/√Hz
Active Chip Area		568µm × 541µm	538µm × 538µm	290µm × 360µm

*ΔV_{out} was not provided for load regulation in fully on-chip version.

IV. CONCLUSION

A fully on-chip LDO voltage regulator for remotely powered cortical implants is presented. The regulator circuit design features and improved symmetric single-ended cascode compensation, which guarantees the stability through the full load current range. Moreover, a novel technique is introduced to boost the PSRR compared to conventional cascode compensation technique. A load regulation of 0.175V/A and a line regulation of 0.024% have been measured. The regulator is stable through the full load range and settles within 10-bit accuracy of the nominal voltage within 1.6µs when stimulated by the full load current. The PSRR at 1MHz is measured at 37 dB using the proposed PSRR booster circuit. The regulator is fabricated in a 0.18µm CMOS technology and drains 28µA from the supply. The active chip area is 0.105 mm^2. With these characteristics, the presented regulator is uniquely suitable for implanted applications where highly accurate and stable reference voltages are needed.

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