A 65-nm CMOS Temperature-Compensated Mobility-Based Frequency Reference for Wireless Sensor Networks

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***Abstract*—A temperature-compensated CMOS frequency reference based on the electron mobility in a MOS transistor is presented. Over the temperature range from $-55°C$ to $125°C$, the frequency spread of the complete reference is less than $\pm 0.5\%$ after a two-point trim and less than $\pm 2.7\%$ after a one-point trim. These results make it suitable for use in Wireless Sensor Network nodes. Fabricated in a baseline 65-nm CMOS process, the 150 kHz frequency reference occupies 0.2 mm^2 and draws 42.6 μA from a 1.2-V supply at room temperature.**

***Index Terms*—Charge carrier mobility, CMOS integrated circuits, crystal-less clock, frequency reference, low voltage, MOSFET, sigma-delta modulation, smart sensors, temperature compensation, temperature sensors, ultra-low power, wireless sensor networks.**

I. Introduction

WIRELESS Sensor Networks (WSN) are based on small, cheap and energy efficient nodes. Since the largest fraction of the energy used in each node is spent listening to the channel, synchronous networks are employed to shorten this wasted time [1]. In that case, the receiver predicts the timeslot that the transmitter will use and turns itself off when no incoming signal is expected. The duty-cycle of the receiver can be lower if the timeslot is predicted with a smaller error, i.e., if a more accurate time reference is available. Accuracies of a few ppm can be achieved by crystal-controlled oscillators (XCOs), but since such external components should be avoided to reduce the cost and size of the nodes, accuracy must be given up for the sake of integration.

The tradeoff between integration and time/frequency accuracy is also present in the RF front-end. While commercial communication systems require high frequency accuracy, radios for WSN can be optimized to relax such specifications and so frequency accuracies in the order of only a few percent are needed [1]–[3]. Thus, it is interesting to investigate the level of accuracy that can be reached without external components, while also operating at the low voltage and power levels typical of WSN. Moreover, since CMOS RF circuits can be implemented with higher power efficiency in deep-submicron processes [4], it is appropriate to pay attention to the possibility of fully integrating the entire node, including the frequency reference, in such processes.

Recently, much work has been devoted to implementing fully integrated frequency references in standard microelectronic technologies. *LC* oscillators [5] can provide accuracy and phase noise performances comparable to XCOs; however, their power consumption can hardly be reduced below 100 μW due to the limited quality factor of integrated inductors and the possible need for high-speed frequency dividers. Fully integrated frequency references based on ring oscillators [6] and silicon thermal diffusivity [7] are quite accurate, but dissipate several milliwatts of power. *RC* oscillators can achieve inaccuracies less than 1% while consuming less than 200 μW [8], [9], but their accuracy relies on the availability of on-chip resistors with low or, at least, accurately defined temperature coefficients.

As an alternative, the mobility of the charge carriers in a MOS transistor can be employed as a reference in a low-power fully integrated oscillator which does not require accurate components other than MOS transistors. It exhibits low process spread and, although its temperature dependence is large (approximately proportional to $T^{-1.6}$, where T is the absolute temperature), it is well defined for a given process and thus can be compensated for. The effect of process spread can then be removed by a one-point or two-point temperature calibration.

In this paper, we explore the level of accuracy that can be achieved by a fully integrated temperature-compensated oscillator that is referenced to the electron mobility [10]. The mobility-based oscillator presented in [11] and the temperature sensor presented in [12] have been integrated on the same die and combined to realize a novel temperature compensation scheme. Experimental validation of this approach will be provided, demonstrating that, after a two-point calibration, a frequency spread of less than $\pm 0.5\%$ can be achieved over the military temperature range. Section II describes the architecture of the overall frequency reference. The implementation of the main blocks composing the frequency reference (mo-

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bility-referenced oscillator, temperature sensor and temperature compensation) is described in detail in Section III. Experimental results are shown in Section IV and conclusions are given in Section V.

II. System Architecture

The core of the proposed frequency reference is a current-controlled relaxation oscillator, in which the current is proportional to the electron mobility. Consequently, as explained in details in Section III-A, its output frequency has the same temperature dependency as the electron mobility and so temperature compensation is needed. This can be implemented either in analog or in digital way. An analog compensation can be realized by adjusting one of the many analog control variables possible in the oscillator. For example, the control current of the oscillator can be implemented as the sum of the mobility-dependent current and a current with a complementary temperature dependency. This would be fairly easy if a physical effect with such a complementary temperature dependance would exist. However, it does not and the generation of a suitable current would increase circuit complexity and be subject to errors which would lower the accuracy of the frequency reference.

Digital temperature compensation schemes do not suffer from these problems. It can be easily implemented by dividing or multiplying the oscillator frequency by a temperature-dependent factor. Operations in the time domain (frequency multiplication and division) are well suited to deep-submicron implementation, since the inherent speed of the process can be exploited to achieve accurate performances by reducing the delays in any time operation. Moreover, as will be explained in the following, a large part of the compensation can be implemented by re-using circuit blocks already present in the system. This minimizes circuit overhead and, consequently, power consumption.

Fig. 1 shows the proposed compensation schemes. In Fig. 1(a), the output frequency of the mobility-based oscillator $f_{\rm osc}$ is used as the reference of an integer-N phase-locked loop (PLL), composed of a phase detector (PD), a loop filter, a voltage-controlled oscillator (VCO) and an divider. Via a pre-determined compensation curve, the digital output of a temperature sensor (TS) is mapped to the divider factor $N_{\rm mul}$, in such a way that the output frequency $f_{\rm RF}$ remains constant over temperature. In Fig. 1(b), $f_{\rm out}$ is obtained by direct division of $f_{\rm osc}$ by a temperature-dependent $N_{\rm div}$. As already mentioned in the introduction, a WSN node needs both a low-frequency reference for time synchronization of the network protocol and a high-frequency reference for RF communication. Thus, most of the blocks for temperature compensation in Fig. 1, i.e., the PLL to generate $f_{\rm RF}$ and the divider to generate $f_{\rm out}$, are already present in the WSN node. If both systems of Fig. 1 would be integrated in the WSN node, only the nonlinear mapping function should be added to obtain both the high-frequency and low-frequency temperature-independent references.

In order to simplify hardware implementation, it would be convenient for both $N_{\rm mul}$ and $N_{\rm div}$ to be integers. To make the

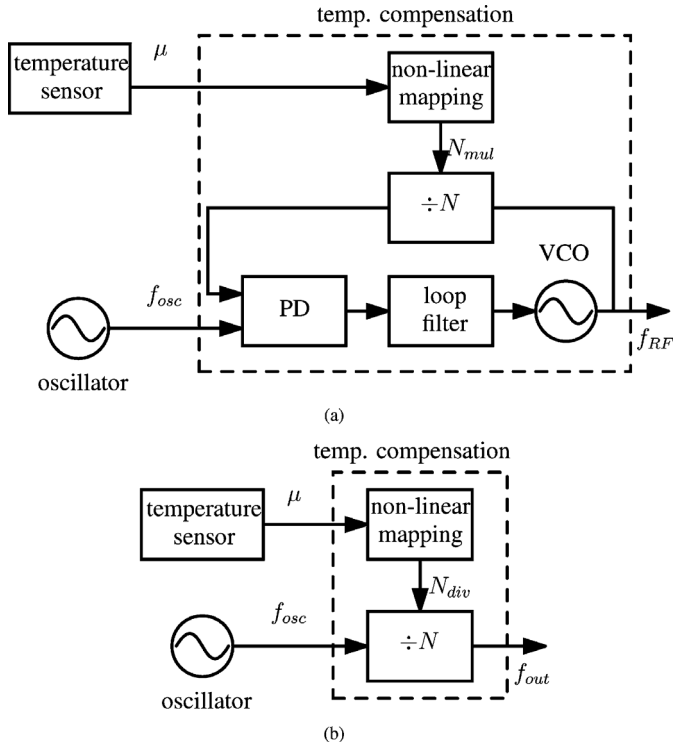

Fig. 1. Architectures for the frequency reference with temperature compensation implemented by means of (a) frequency multiplication and (b) frequency division.

effect of temperature compensation negligible in the total accuracy, the quantization error due to the temperature compensation should be low enough, which can be expressed, for $N_{\rm mul}$ and $N_{\rm div}$ integers, as

$$N_{\rm mul}, N_{\rm div} > N_{\rm res} \tag{1}$$

$$N_{\rm res} = \left\lfloor \frac{10}{a} \right\rfloor \tag{2}$$

where $N_{\rm res}$ is the minimum factor needed to achieve the required resolution, a is the aimed accuracy for the whole reference and a factor 10 has been assumed between the reference accuracy and the quantization error of the compensation scheme, to make the latter negligible. Considering that $N_{\rm mul} = f_{\rm RF}/f_{\rm osc}$ and $N_{\rm div} = f_{\rm osc}T_{\rm synch}$ with $T_{\rm synch} = f_{\rm out}^{-1}$, the following inequality must be satisfied

$$\frac{f_{\rm RF}}{\left\lfloor \frac{10}{a} \right\rfloor} > f_{\rm osc} > \frac{\left\lfloor \frac{10}{a} \right\rfloor}{T_{\rm synch}}. \tag{3}$$

It has been proven that WSNs can tolerate $a \approx 1\%$, while adopting an RF frequency of the order of 1 GHz and using time spans between 10 ms and 100 ms for the network synchronization [1], [2]. It follows from (3) that the oscillator frequency must be in the range between 1 MHz and 10 kHz, while keeping at least 10 bits of resolution for the divider ratios. A value of $f_{\rm osc} = 150$ kHz is then used in this work. Since the accuracy of the proposed mobility-based reference can be demonstrated by any of the two systems of Fig. 1, only the system in Fig. 1(b) has been implemented and it is discussed in the following.

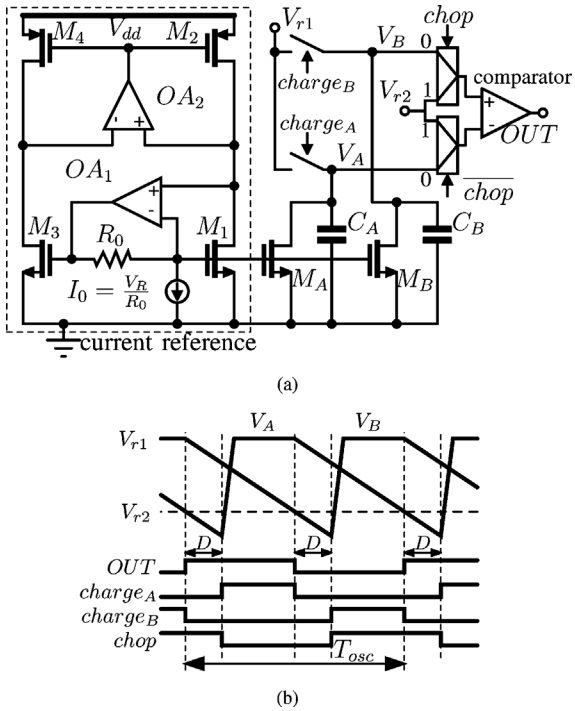

Fig. 2. (a) Mobility-referenced oscillator and (b) its waveforms, from [11].

III. Circuit Implementation

A. Mobility-Based Oscillator

A simplified schematic of the mobility-based frequency reference is shown in Fig. 2(a). As shown in [11] and with reference to Fig. 2, the oscillation frequency is

$$f_{\rm osc} = \frac{\mu_n C_{\rm ox}}{4C}\frac{W_1}{L_1}\frac{V_R^2}{V_{r1}-V_{r2}} \tag{4}$$

where μ_n is the electron mobility, $C_{\rm ox}$ is the oxide capacitance per unit area, W_1 and L_1 are the width and length of M_1 and $C = C_A = C_B \propto C_{\rm ox}$. If V_R, V_{r1} and V_{r2} are reference voltages (or if at least they are proportional), then $f_{\rm osc}$ has the same temperature dependence as μ_n. The typical measured output frequency of the mobility-based oscillator is shown in Fig. 3. The plot, obtained by measurement of the test chip described in Section IV, is shown here to illustrate the temperature dependence of $f_{\rm osc}$, which, in turn, is needed in the next section to derive the requirements for the TS.

B. Temperature Sensor

1) Requirements: Besides the need for a low-power low-voltage circuit implementation, the main specifications of the TS are accuracy and conversion rate. With regards to accuracy, if the reading of the TS has an error ΔT, the error in the compensated frequency $f_{\rm out}$ is given, for an ideal temperature compensation, by

$$\frac{\Delta f_{\rm out}}{f_{\rm out}} \approx \frac{\Delta T}{f_{\rm osc}}\frac{\partial f_{\rm osc}}{\partial T}. \tag{5}$$

Using the data from Fig. 3, the error in the compensated frequency for different values of ΔT is shown in Fig. 4. As for the quantization error introduced by the compensation scheme, the error is kept to about 0.1%, which corresponds to $\Delta T = 0.2°\mathrm{C}$.

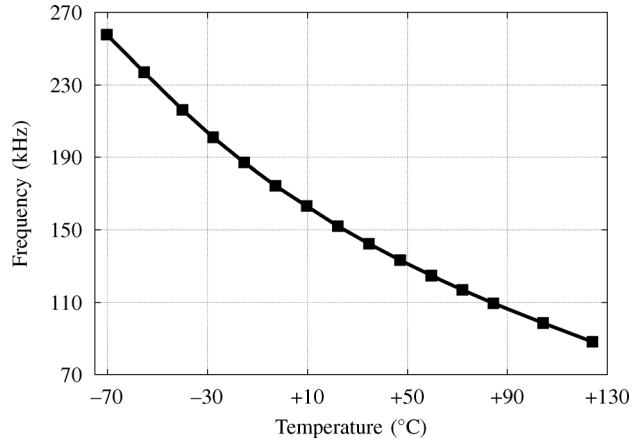

Fig. 3. Uncompensated oscillator output frequency ($f_{\rm osc}$).

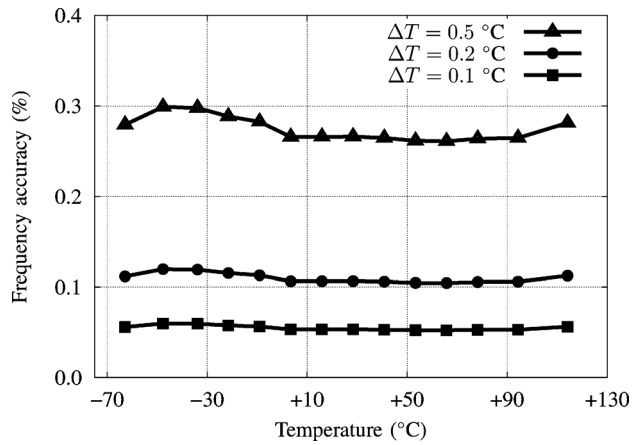

Fig. 4. Accuracy of the output frequency after compensation using a temperature sensor with an accuracy ΔT.

The conversion rate must be adequate to the temperature variations expected in the particular application. A slow sensor might not be able to accurately track such variations and would thus introduce extra readout errors. Temperature variations can be caused either by self-heating of the die or by environmental variations. The first can be neglected for a WSN node, since self-heating is limited to few hundredths of a degree Celsius for power dissipations of a few 100 μW, considering a thermal resistance between die and ambient in the order[1] of 100°C/W. The latter is limited to a variation of a few degrees in a time span ranging from seconds to minutes for typical WSN applications, such as environmental monitoring. Moreover, the thermal mass of the silicon die itself ($C_{\rm die}$) combined with the thermal resistance of the package ($R_{\rm pkg}$) filters the high-frequency components of environmental temperature variations down to few hertz.[2]

[1]A package thermal resistance R_{pkg} in the order of 100°C/W is typical for the most common IC packages [13].

[2]For a typical silicon die of 1 mm^2 area, $C_{die} = 0.5$ mJ/°C. Considering a simple RC lumped-element thermal model, this together with $R_{pkg} = 100°\mathrm{C/W}$ results in a 3-Hz cut-off frequency.

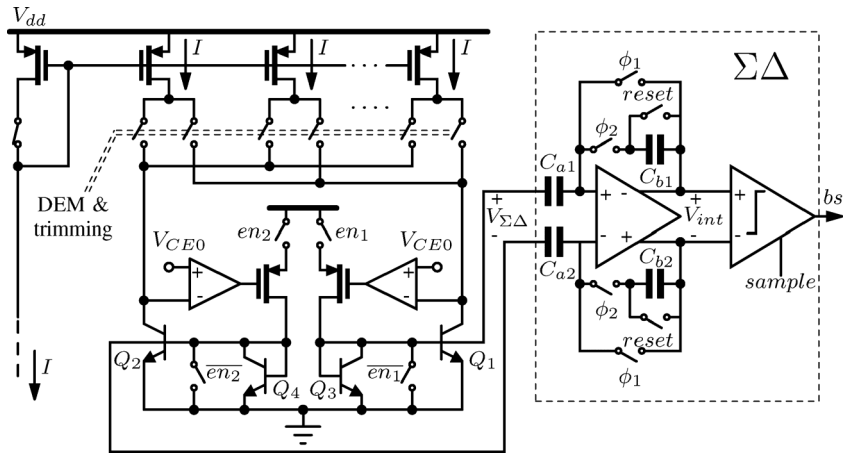

Fig. 5. Simplified schematic of the bandgap temperature sensor (from [12]).

2) Proposed Temperature Sensor: Several sensing principles have been proposed for deep-submicron CMOS temperature sensors [14]–[17]. However, only bandgap temperature sensors achieve an accuracy below 1°C without the need for an expensive multi-point temperature calibration and with a power consumption below 100 μW [18]. Consequently, a bandgap TS has been used in this work.

The proposed bandgap based TS is shown in Fig. 5 [12]. When $en_{1,2}$ are both high, the vertical NPN $Q_{1,2}$ are biased by the PMOS current sources array at a 1:4 collector current ratio to produce a proportional-to-absolute-temperature (PTAT) difference between their base emitter voltages $V_{\Sigma\Delta} = \Delta V_{be}$. When en_1 (en_2) is high and en_2 (en_1) is low, Q_1 (Q_2) is biased by a fixed current and the base-emitter junction of Q_2 (Q_1) is shorted to produce $V_{\Sigma\Delta} = +V_{be}$ ($V_{\Sigma\Delta} = -V_{be}$). The feedback loops comprising the amplifiers and the common-source buffers compensate the base current of $Q_{1,2}$, so that neither ΔV_{be} nor V_{be} depends on the bipolar current gain. Moreover, the two loops decrease the impedance at the collectors of $Q_{1,2}$, by fixing the collector voltages equal to the reference voltage V_{CE0}. To prevent the capacitive load of the analogue-to-digital converter from making the loops unstable, diode-connected $Q_{3,4}$ are added to lower the impedance at the base of $Q_{1,2}$.

A first-order $\Sigma\Delta$ analog-to-digital converter is used to produce an output bitstream bs whose average μ represents the TS output. The bitstream average is extracted by a cascaded sinc^2 decimation filter. The switched-capacitor integrator in the $\Sigma\Delta$ integrates $2 \cdot \Delta V_{be}$ when $bs = 0$ and $-V_{be}$ when $bs = 1$. Since the negative feedback forces the average integrated voltage to be zero, the bitstream average is

$$\mu = \langle bs \rangle = \frac{2 \cdot \Delta V_{be}}{V_{be} + 2 \cdot \Delta V_{be}}. \tag{6}$$

Although μ is a nonlinear function of temperature, the biasing of the NPNs has been chosen [12] such that a function that is PTAT can be obtained by applying the transformation

$$\mu_{\mathrm{PTAT}}(\mu) = \frac{9 \cdot \mu}{1 + 8 \cdot \mu}. \tag{7}$$

C. Temperature Compensation

To investigate the level of accuracy reachable by the mobility-based frequency reference, two distinct and independent temperature compensation schemes have been implemented, requiring either a single-point trim or a two-point trim. While the cost of a single-point trim is relatively low, the cost of a two-point trim can make the whole reference even more expensive than XCOs. However, its reduced size, thanks to the full integration, makes it the preferred choice in several applications. For both schemes, the resolution of the divider ratio N_{div} has been kept to 13 bits. As discussed in Section II, even a resolution of approximately 10 bits is high enough when aiming for accuracy in the order of 1%. However, a higher resolution is preferred to show that accuracy lower than 1% can be reached over a temperature range narrower than the industrial range.

For a single-point trim, the oscillation frequency of each sample at the trim temperature $f_{\mathrm{osc}}(T_{\mathrm{trim}})$ is measured. A seventh-order polynomial $P_7(\cdot)$, whose coefficients are fixed for all the samples, is then obtained via a batch calibration. The divider factor N_{div} is computed as

$$N_{\mathrm{div}} = \frac{f_{\mathrm{osc}}(T_{\mathrm{trim}})}{f_{\mathrm{nom}}} P_7(\mu) \tag{8}$$

where $f_{\mathrm{nom}} = 1/T_{\mathrm{synch}} = 1/50$ ms is the nominal frequency of oscillation, i.e., the desired output frequency.

For a two-point trim, the following procedure is adopted. The oscillator frequency f_{osc} and the on-chip TS decimated output μ are measured at two different temperatures, $T_{\mathrm{trim},1}$ and $T_{\mathrm{trim},2}$. This data is used to interpolate the frequency using the interpolant

$$f_{\mathrm{osc}} = A \cdot \mu_{\mathrm{PTAT}}^{B} \tag{9}$$

where μ_{PTAT} is computed from the TS output using (7) and A and B are the trim parameters for each sample. A fourth-order polynomial $Q_4(\cdot)$ is obtained from batch calibration so that the divider factor N computed for each sample is

$$N_{\mathrm{div}} = \frac{1}{f_{\mathrm{nom}}} A \cdot \left\{ \mu_{\mathrm{PTAT}} \left[Q_4(\mu) \right] \right\}^{B}. \tag{10}$$

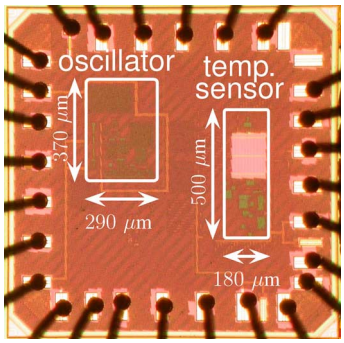

Fig. 6. Die micrograph of the test chip.

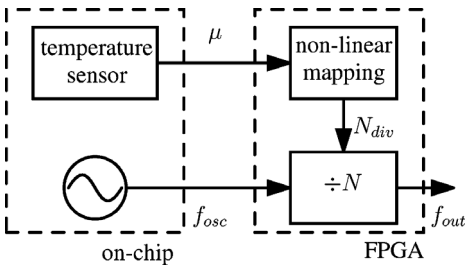

Fig. 7. System block diagram of the mobility-based frequency reference showing the partition in the implementation between on-chip circuitry and FPGA.

The polynomial[3] $Q_4(\cdot)$ is required to compensate for the fact that the power-law interpolant in (9) only approximately describes the temperature dependence of the electron mobility, especially over a wide temperature range.

In terms of complexity, the trimming procedure requires only the measurement of $f_{\rm osc}$ at one temperature for the single-point trim, and the measurement of $T_{\rm trim,1}$, $T_{\rm trim,2}$ and $f_{\rm osc}$ at such temperatures for the two-point trim. The trim parameter A and B can be computed by fitting an exponential function through the points $(T_{\rm trim,1}, f_{\rm osc}(T_{\rm trim,1}))$ and $(T_{\rm trim,2}, f_{\rm osc}(T_{\rm trim,2}))$. Finally, note that the computation of $N_{\rm div}$ requires only basic mathematical operation, i.e., computation of polynomial, multiplication and raise to the power, which are well-suited for implementation in a deep-submicron CMOS process.

IV. Experimental Results

The frequency reference was fabricated in a standard 65-nm CMOS process (Fig. 6). The circuit occupies 0.2 mm^2 (0.1 mm^2 for the oscillator and 0.1 mm^2 for the TS) and uses only 2.5-V I/O thick oxide MOS devices. For flexibility, some control logic, the TS's sinc^2 decimation filter (employing 6000 bitstream samples to produce one temperature reading) and the reference voltages (V_R, V_{r1}, V_{r2}) were implemented off-chip. The reference draws 42.6 μA (34.3 μA for the oscillator and 8.3 μA for the TS) from a 1.2-V supply at room temperature. The supply sensitivity is 1.2%/V. In order to flexibly test different compensation schemes, the temperature compensation scheme has been implemented in an off-chip FPGA, as shown in Fig. 7. However, if the temperature compensation had been implemented on-chip, its consumption would have been negligible. From simulations, the power consumption of a 13-bit frequency divider implemented in 65-nm CMOS is below 0.3 μW at room temperature for an input frequency of 150 kHz and a 1.2-V supply. The nonlinear-mapping block consumption would also be low considering that the value of $N_{\rm div}$ must be updated only at the rate of the TS, which is in the order[4] of 1 Hz.

Measurements on 12 samples from one batch were performed over the temperature range from -70°C to $+125^\circ$C using a temperature-controlled oven. For those measurements, the reference voltages were set to $V_R = 0.25$ V, $V_{r1} = 1.6$ V, and $V_{r2} = 1.2$ V and the supply of the comparator of Fig. 2(a) has been raised to 1.5 V. This ensures that MOS capacitor C_A and C_B are biased in deep inversion to prevent the spread of their threshold voltage from affecting the spread of the reference, and thus masking the inherent accuracy of the mobility-based reference. The temperature of the samples was measured using a Pt100 platinum thermometer and compared to the temperature reading of the on-chip TS. The TS shows a spread on $\mu_{\rm PTAT}$ of 0.5°C (3σ) over the range from -70°C to $+125^\circ$C.

Fig. 8 shows the uncompensated output frequency of the oscillator. At room temperature, its maximum deviation from the average is $\pm 6\%$. The temperature compensation has then been implemented off-line in Matlab. First, the samples were trimmed at $T_{\rm trim} = 22^\circ$C and compensated with an external Pt100 and an ideal temperature compensation curve. In those conditions, the maximum error is $\pm 2.6\%$ over the military range from -55°C to 125°C. Then, the compensation polynomial $P_7(\cdot)$ (see Section III-C) was extracted from batch calibration of the 12 devices. After a single-point trim at $T_{\rm trim} = 22^\circ$C, the error when compensating with the on-chip TS is less than $\pm 2.7\%$ (Fig. 9). Finally, a two-point trim at $T_{\rm trim,1} = -27^\circ$C and $T_{\rm trim,2} = 105^\circ$C was employed and the error improved to $\pm 0.5\%$ using another compensating polynomial $Q_4(\cdot)$ (see Section III-C) extracted from a batch calibration of the 12 devices (Fig. 10). The temperature of the two trimming points has been chosen to optimize the accuracy of the frequency reference over the temperature range of interest. For the adopted compensation schemes, the resolution of the integer divider factor $N_{\rm div}$ in Fig. 1 has been limited to 13 bits.

In order to study the dynamic performance of the temperature compensation, one of the samples already tested in the temperature-controlled oven has been tested under the effect of fast temperature variations. Fig. 11 shows the static frequency error of the tested sample over the temperature range, i.e., the frequency error under static temperature conditions. Note that the selected sample is among those with lowest static error, so that the error due to the dynamic behavior can be more easily observed. In this case, real-time temperature compensation has been performed on the FPGA, while the sample (packaged in a ceramic DIP28 package) was heated by a flux of hot air. For those measurements, the reference voltages were set to $V_R = 0.2$ V, $V_{r1} = 1.2$ V and $V_{r2} = 0.8$ V, $f_{\rm osc} = 96$ kHz and all supplies were set to 1.2 V. The TS was sampled at $f_{\rm sample} = 3$ Sa/s. The $\Sigma\Delta$

[3]Note that the order of the polynomials $P_7(\cdot)$ and $Q_4(\cdot)$ is the minimum required for the error due to the nonlinearity of the compensation to be negligible compared to the spread among the samples.

[4]The update rate of $N_{\rm div}$ depends on the temperature variations rate in the chosen application.

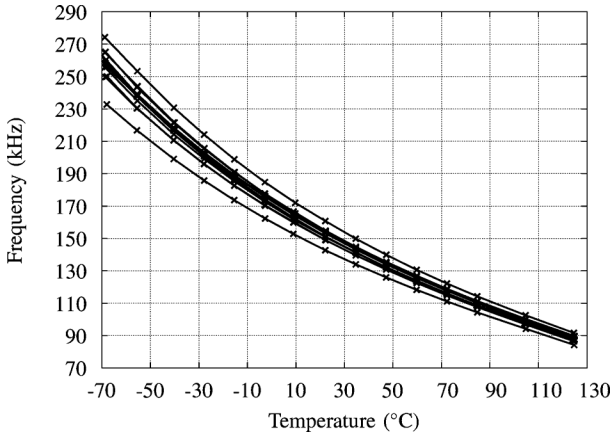

Fig. 8. Uncompensated oscillator output frequency ($f_{\rm osc}$).

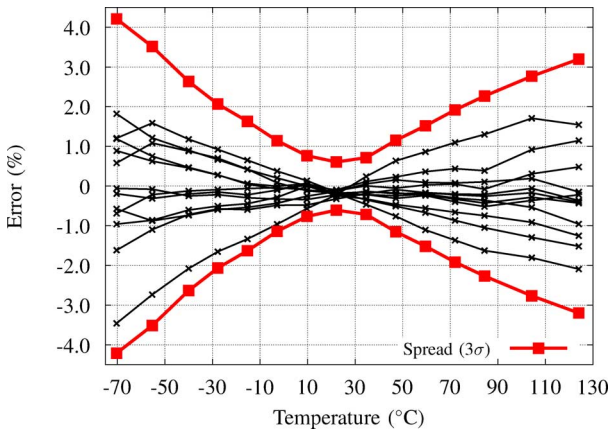

Fig. 9. Frequency error of the reference after single-point trim.

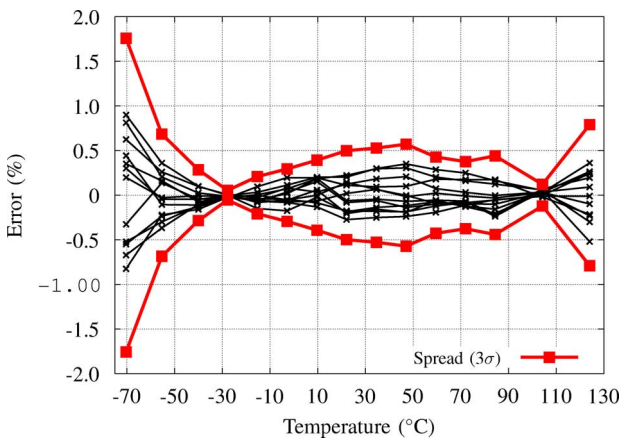

Fig. 10. Frequency error of the reference after two-point trim.

modulator in the TS is operated as an incremental converter: it is first reset and a temperature reading is produced after $1/f_{\rm sample}$. In the next period $1/f_{\rm sample}$, such temperature reading is produced to compute $N_{\rm div}$ and compensate $f_{\rm out}$. The output frequency is then affected by errors due to the delay of $1/f_{\rm sample}$ in the temperature compensation. Fig. 12 shows the measured time-domain waveforms acquired by the FPGA, including the temperature reading of the on-chip TS, the period of $f_{\rm out}$ and

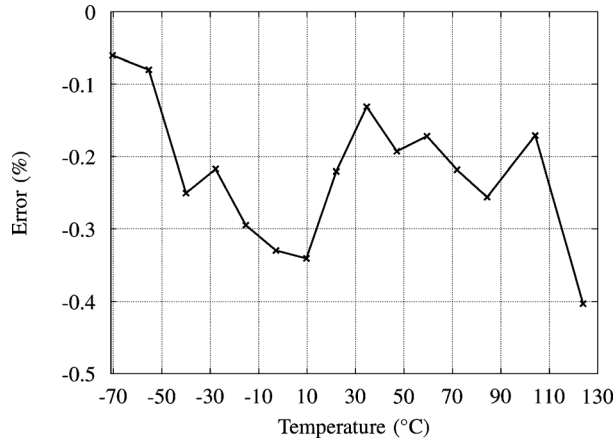

Fig. 11. Frequency error of the sample used for time-domain measurements (after a single-point trim at room temperature).

the divider ratio $N_{\rm div}$. When hot air is applied, the on-chip temperature rises from room temperature to approximately 100°C with an exponential response with time constant $\tau_1 = 20$ s. Due to the fast temperature variation, a step is observed in the oscillation period due to the temperature compensation delay. The amplitude of the step can be computed by considering the temperature reading error ΔT due to the delay and by applying (5). The amplitude of the step is given by

$$\Delta t_{\rm step} = t_0 \left(\frac{1}{f_{\rm osc}}\frac{\partial f_{\rm osc}}{\partial T}\right)\Delta T \approx t_0 \left(\frac{1}{f_{\rm osc}}\frac{\partial f_{\rm osc}}{\partial T}\right)\left(-\frac{T_{\rm step}}{\tau_1}\frac{1}{f_{\rm sample}}\right) \quad (11)$$

where t_0 is the oscillation period of the output signal ($1/f_{\rm out}$) in the steady state, ΔT is the equivalent temperature error due to the compensation delay and $T_{\rm step} = 75$°C is the step in the die temperature. ΔT has been calculated by considering an exponential settling of the temperature with time constant τ_1. Using the data from (5) and the data from Fig. 4, $\Delta t_{\rm step} \approx 0.3$ ms, which is in good agreement with the value measured in Fig. 12. When the flow of hot air stops, the temperature drop exponentially to the room temperature.[5] Even if a negative step in the oscillation period is expected at the onset of the cooling, it is not visible in the measurements. This is because the cooling transient is slow enough to make the dynamic error much smaller than the static error reported in Fig. 11. The oscillation period is also affected by random noise with standard deviation of 0.1%, in agreement with the long-term jitter measurements shown previously in [11]. This proves that also under excitation with large and fast temperature variations, the frequency reference error is kept in the order of 1%.

The frequency reference's performance is summarized in Table I and compared to other low-power fully integrated CMOS frequency references. The silicon area and the power consumption of the proposed frequency reference are comparable to the other designs in Table I, even if a fair comparison is

[5]The time constant of the exponential settling is in this case $\tau_2 = 180$ s due to the lack of induced air flow on the sample and the consequent increase in thermal resistance $R_{\rm pkg}$.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Reference	[8]	[9]	[19]	This work	
Oscillator frequency	6 MHz	10 MHz	30 MHz	150 kHz	
Temp. compensated frequency	6 MHz	10 MHz	30 MHz	20 Hz	
Supply	1.2 V	1.2 V	3.3 V	1.2 V	
Power	66 μW	80 μW	180 μW	51 μW	
Technology	65 nm	0.18 μm	0.35 μm	65 nm	
Area	0.03 mm^2	0.22 mm^2	0.08 mm^2	0.2 mm^2	
Temp. range (°C)	0∼120	-20∼100	-20∼100	-55∼125	
Inaccuracy (max)	±0.9%	±0.4%	±0.7%	±0.5%	±2.7%
Calibration	single	N.A.[a]	N.A.[a]	double	single
Samples tested over temp.	4	1	1	12	

[a]No calibration defined for a single sample.

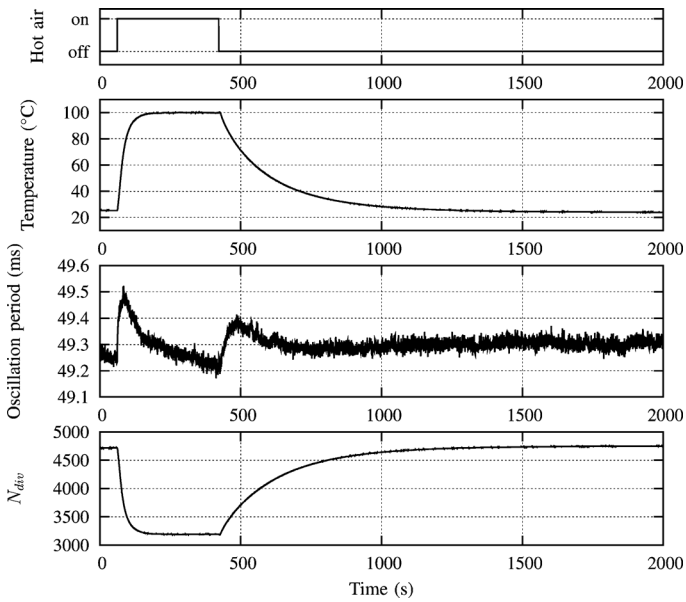

Fig. 12. Measured time-domain waveforms of the compensated frequency reference, including the on-chip TS reading, the period of the output signal $(1/f_{\rm out})$ and the divider ratio $N_{\rm div}$, when the sample is heated by a flux of hot air (whose timing is shown on the upper plot).

challenging due to the lower oscillator frequency chosen in this work. Because of the temperature compensation by frequency division shown in Fig. 7, the output frequency is only 20 Hz. However, both in this work and in those cited in Table I, the power dissipated for temperature compensation is, to first order, independent of the output frequency. With regard to the performance of the temperature compensation scheme, the proposed frequency reference achieves accuracy comparable to the state-of-the-art over a wider temperature range and for significantly more measured samples.

V. CONCLUSION

A fully integrated temperature-compensated frequency reference based on electron mobility has been presented. The inaccuracy of the complete system, including mobility-based oscillator, bandgap temperature sensor and temperature compensation, is less than ±2.7% after single-point trim and less than ±0.5% after two-point trim over the military temperature range. This demonstrates that frequency references with inaccuracies less than 1% over a wide temperature range can be realized with MOS transistors, even in nanometer CMOS. Those references are accurate enough for WSN applications, while working at low voltage and low power, as required for use in autonomous sensor nodes.

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