A high PSRR Class-D audio amplifier IC based on a self-adjusting voltage reference

Alexandre Huffenus, Gaël Pillonnet, Nacer Abouchi, Frédéric Goutti, Vincent Rabary, Robert Cittadini

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Alexandre Huffenus, Gaël Pillonnet, Nacer Abouchi
Lyon Institute of Nanotechnology
University of Lyon
Villeurbanne, France
alexandre.huffenus@cpe.fr

Frédéric Goutti, Vincent Rabary, Robert Cittadini
AMPS
STMicroelectronics
Grenoble, France
frederic.goutti@st.com

***Abstract*—In a wide range of applications, audio amplifiers require a large Power Supply Rejection Ratio (PSRR) that the current Class-D architecture cannot reach. This paper proposes a self-adjusting internal voltage reference scheme that sets the bias voltages of the amplifier without losing on output dynamics. This solution relaxes the constraints on gain and feedback resistors matching that were previously the limiting factor for the PSRR. Theory of operation, design and IC evaluation in a Class-D amplifier in CMOS 0.25µm will be shown in this paper. The use of this voltage reference increased the amplifier's PSRR by 15dB, with only a 140µA increase in current consumption.**

I. INTRODUCTION

In environments with a large power supply noise, like mobile phones using the GSM protocol [1], the PSRR of the audio subsystem should be high to prevent from an audible "GSM noise" on the output. Audio speaker amplifiers for mobile applications usually have PSRRs about 65dB [2] in the audio band, limited by a combination of the bias voltage's PSRR and the matching of the feedback network as Section II will explain. IC techniques exist to improve components matching like area increase, interdigitizing or trimming, but they increase the IC production cost and still have limits in terms of attainable matching and PSRR. An architecture change is proposed in Section III, modifying the way the voltage reference is generated. The low-PSRR resistive divider is replaced by a self-adjusting high-PSRR reference which design will be shown in Section IV. Simulation and measurement results of a Class-D amplifier using this new voltage reference will be presented in Section V.

II. ACTUAL ARCHITECTHRE LIMITATIONS

A. Bias Voltage Generation

Fig. 1 shows the block diagram of a Class-D amplifier for mobile applications. The amplifiers in the signal chain (the input preamplifier and the integrator in the Class-D loop) require a voltage bias to set their common mode voltages. In order to maximize the output swing, this reference needs to be equal to *Vdd/2* as illustrated in Fig. 2.

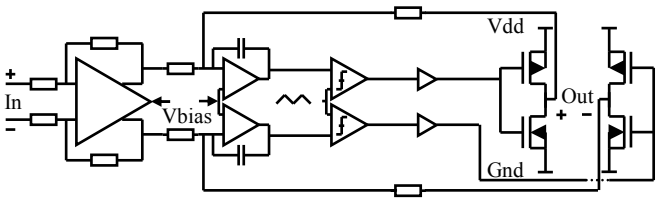


Figure 1. Class-D amplifier signal path

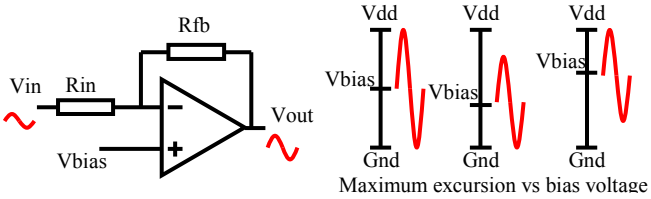


Figure 2. Bias voltage and excursion

Typically, this bias voltage is generated with a resistive divider between *Vdd* and *Gnd* as presented in Fig. 3, with the addition of an internal bypass capacitor to improve the supply ripple rejection. Since high-ohmic resistors and large capacitors cannot be integrated, the corner frequency of this RC filter is too high to offer a good enough PSRR in the audio band. Values like 2*200kΩ and 100pF are realistic, leading to a corner frequency of 16kHz. The PSRR of this voltage reference is then only -6dB in most of the audio range.

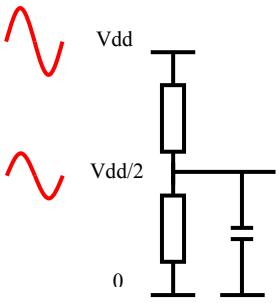


Figure 3. Filtered resistive divider as reference

B. *Influence of Resistor Mismatch on the PSRR*

In the structure from Fig. 1, the inputs are typically fed by a DAC, which outputs have a fixed common-mode [3]. The preamplifier's outputs have a common-mode set to *Vdd/2* via its Common Mode FeedBack (CMFB) loop as in Fig. 4.

If *Vdd* varies, AC currents will flow through *R1-R2* and *R'1-R'2*. If *R1/R2* does not exactly equal *R'1/R'2*, a differential AC signal will show on the preamplifier's output, limiting the PSRR of the signal chain [4].

Equation (1) defines the differential output voltage of the preamplifier, according to its open loop gain *Av*, *R1/R2=a* and *R'1/R'2=b*. If *Av* is large, this leads to (2) and shows that it depends both on the matching of the resistors and the variation of the common-mode voltage. The latter having 6dB of PSRR with a resistive divider, the impact of resistors mismatch on the differential output is large. With *a* and *b* differing from 0.1%, the PSRR is 66dB. Using a high-PSRR bias voltage for the CMFB loop would then significantly improve the PSRR of the preamplifier.

$$\begin{aligned}(V1-V2) &= -Av(V1*a - V2*b) \\ &= -Av\left((V1-V2)\frac{a+b}{2} + (V1+V2)\frac{a-b}{2}\right)\end{aligned} \quad (1)$$

$$(V1-V2) \approx 2\frac{a-b}{a+b}\frac{(V1+V2)}{2} \quad (2)$$

The Class-D loop has a high PSRR, as long as a supply feed-forward scheme is used [5]. Also, its input common-mode voltage matches its bias voltage so it does not suffer from the above-explained issue. Monte-Carlo simulations on the Class-D stage alone show that its PSRR can exceed 90dB.

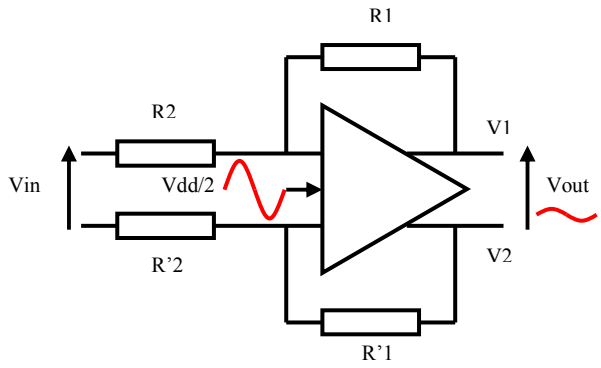


Figure 4. Fully differential operational amplifier

III. New Architecture Overview

In order to improve the PSRR of the amplifier, a new way to generate the bias voltage reference is required. This circuit will have to meet the following requirements:

- PSRR significantly higher than 6dB
- DC voltage equal to *Vdd/2*, whatever the *Vdd* voltage is (from 2.3 to 5.5V) to maximize the voltage swing
- Low current consumption not to impact battery life
- Low IC area to reduce its impact on IC size and cost

The way the voltage of *Vdd/2* is generated and varies with time will depend on the topology chosen for the voltage reference. It can be a fully analog signal with a large time constant (like a low-pass filter with a subsonic corner frequency) that follows the slow variations of *Vdd* (like battery discharge), a steady state system that refreshes its value every second or so (a slow sample & hold) or a system that adjusts its value to Vdd/2 once during the startup phase. Those three configurations are illustrated by Fig 5.

An analog system like a low-pass filter is not realizable in actual IC technology. Having 60dB of PSRR at 217Hz (the frequency of GSM bursts) requires really high-value resistors and capacitors like 10MΩ and 100nF. External bypass capacitors are not allowed in modern amplifier circuits to spare PCB real estate so analog filtering cannot be considered.

Using a switched capacitor solution [6] (like a sample & hold or a switched capacitor low pass filter) at a subsonic frequency causes problems due to leakage current: the hold capacitor leaks through the substrate diodes of the MOSFETs. Currents of a few pA flow, with a refresh rate of 1Hz and capacitor values around 10pF this causes a too high voltage drop of 100mV during a period.

The retained solution is a programmable voltage reference, controlled by a digital word. One possible implementation is an R-2R ladder Digital to Analog Converter (DAC). This DAC is combined with a voltage comparator and a digital counter. The comparator's inputs are connected to the DAC's output and to *Vdd/2* from the resistive divider. During the adjustment phase, the comparator's output state increases or decreases the DAC's output value until it reaches *Vdd/2*. When this condition is met, the comparator toggles and the DAC's output is adjusted to *Vdd/2* (±1LSB). The design of this system will be detailed in the next section.

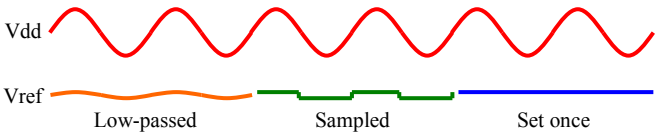


Figure 5. Voltage reference generation methods

IV. VOLTAGE REFERENCE DESIGN

The complete voltage reference is illustrated in Fig. 6, while the DAC architecture is detailed in Fig. 7. It consists of:

- A resistive divider providing *Vdd/2*
- A comparator
- A counter
- A DAC composed of a bandgap voltage reference, an R-2R network and an output amplifier converting the R-2R output current into voltage

The bandgap reference is centered on 1.25V and goes through a voltage divider to feed the I/V converter with a 1.15V voltage, compatible with the lowest *Vdd* of 2.3V. A full CMOS technology has been used, with substrate PNP transistors to generate the bandgap voltage. Its PSRR is 80dB.

The counter and DAC have an 8-bit resolution, and are clocked with the 280kHz oscillator from the Class-D amplifier. At power-up, the system starts from its minimum value (1.15V) and ramps up to *Vdd*/2. It requires less than 1ms to reach the full scale value. If a lower *Vdd* than 5.5V is used the adjustment will be faster. The comparator is powered down in the end of the adjustment phase to reduce current consumption.

In this implementation, the reference is only adjusted during the circuit startup and the counter is allowed to count upwards only. When the DAC voltage crosses *Vdd/2*, the comparator toggles and the counter stops. This is done to adjust the reference voltage to the peak value of *Vdd/2* because in case there is GSM noise on the battery during the amplifier startup, *Vdd* will have voltage dips of a few hundreds of millivolts. The value required for the adjustment is the peak *Vdd*, without the load from the GSM RF Power Amplifier. Fig. 8 shows the startup of the reference voltage when there is noise on the supply voltage. The characteristics of the voltage reference circuit are summarized in Table 1.

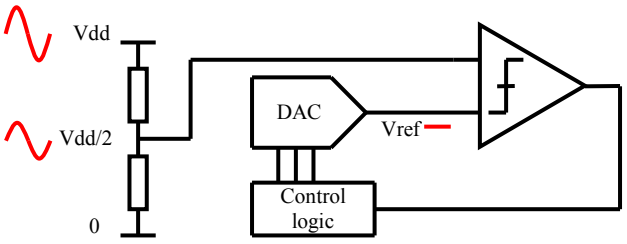


Figure 6. Voltage reference block diagram

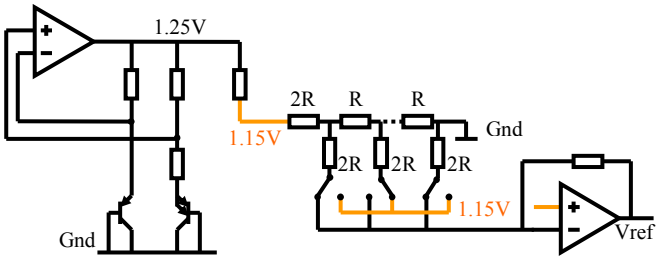


Figure 7. DAC schematic

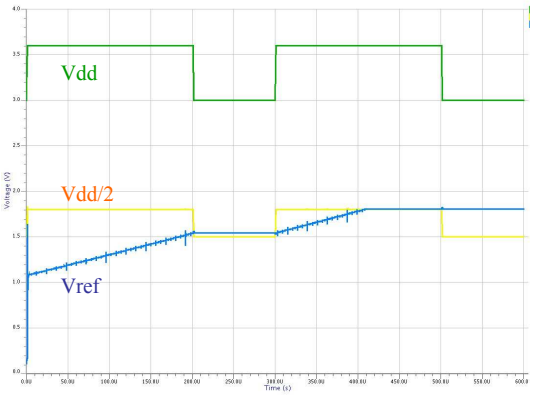


Figure 8. Startup phase adjustment with a noisy Vdd

TABLE I
VOLTAGE REFERENCE CHARACTERISTICS

Parameter	Value	Conditions
PSRR	76dB	Vdd=3.6V
Idd	140µA	Vdd=3.6V
Resolution	8 bit	
Step size	7mV	Typical
Range	1.15-2.75V	All corners
Size	340*210µm	CMOS 0.25µm

V. PSRR PERFORMANCE OF THE NEW SOLUTION

When this new biasing scheme is used on a fully differential amplifier (like the preamplifier in Fig. 4) with a mismatch on the input and feedback resistors, the PSRR obtained is plotted in Fig. 9. The orange (light) curve is the PSRR when a resistive divider is used for the bias voltage, while the green (dark) shows the PSRR with the voltage reference (called Vref) presented in this paper. There is a 25dB improvement in the frequencies up to 4kHz.

With a complete Class-D amplifier as in Fig. 1 and the Vref biasing the differential preamplifier and the integrators, the measured performance is shown in Fig 10.

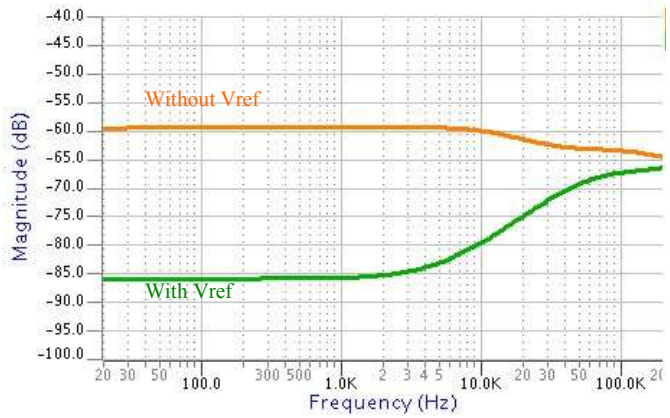


Figure 9. Differential amplifier PSRR (simulated)

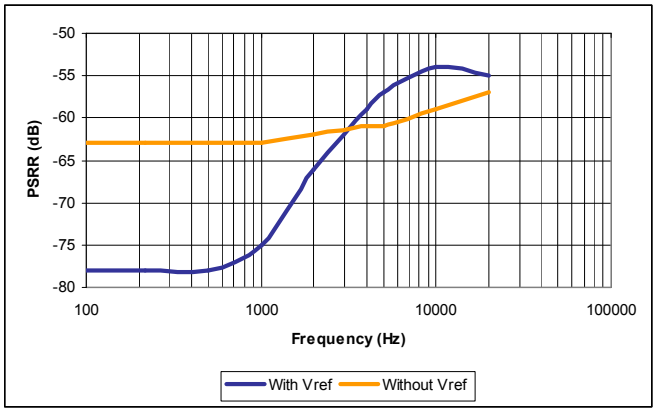


Figure 10. Class-D amplifier PSRR

The use of the new voltage reference considerably increased the low-frequency PSRR, where GSM noise can be found. The PSRR, however, rapidly decreases with increasing frequency. The origin of this effect has been found in the Pulse Width Modulation and the way the sawtooth signal is generated. The amplitude of the sawtooth is *Vdd*-dependant to generate a supply-feedforward [5] and its common-mode voltage is centered on *Vdd/2*, as shows Fig. 11. The integrator has a fixed bias voltage at *Vref,* so when *Vdd* varies, the integrator and sawtooth signals are not properly centered anymore. The feedback loop will act to center the integrator signal correctly, but its loop gain and bandwidth are limited so it compromises the PSRR performance.

A solution is presented in Fig. 12, adding a *Vdd*-dependant signal after the integrator. This way, when *Vdd* varies, both the sawtooth signal and the integrator output will vary together. This is a feedforward scheme, hence not relying on the limited feedback loop. Performance of this structure is shown in Fig. 13 and gives a significant improvement in high frequencies. Fig. 14 shows the amplifier IC in CMOS 0.25µm technology.

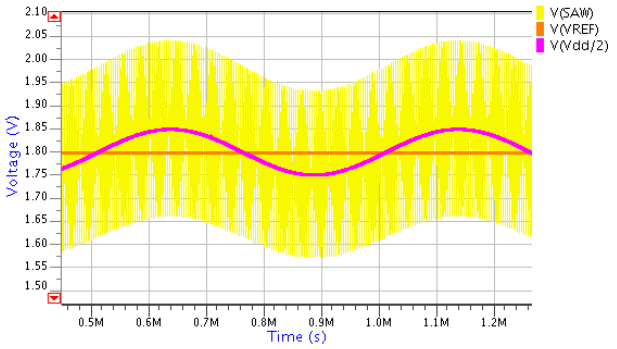


Figure 11. Voltage levels with a ripple on Vdd

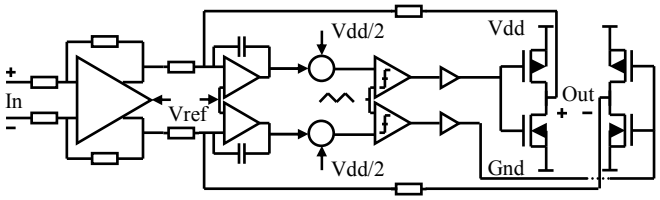


Figure 12. Class-D amplifier with Vdd compensation

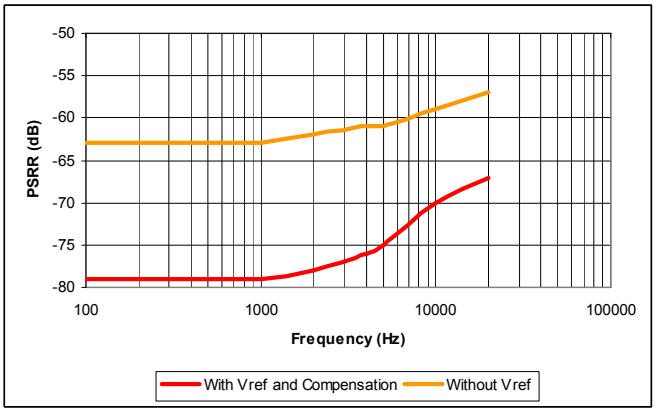
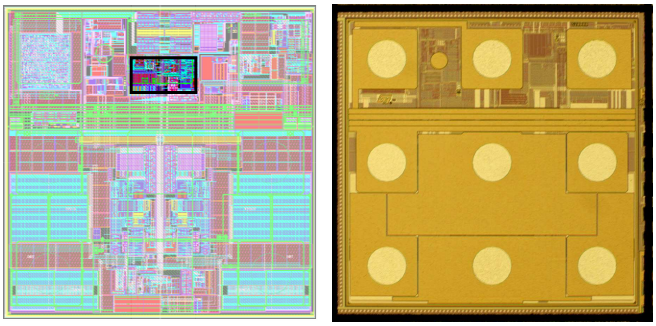


Figure 13. Class-D amplifier PSRR with Vdd compensation



Dimensions: 1500*1500µm

Figure 14. IC layout (left) and photograph (right)

VI. CONCLUSION

This paper has shown that the origins of the low PSRR of mobile Class-D amplifiers are the mismatch between the input and feedback resistors and the PSRR of its bias voltage. A new high-PSRR voltage reference scheme has been designed to help on this issue, and the Class-D amplifier using this reference showed a PSRR improvement of 15dB in most of the audio band. The current consumption of the reference was 140µA, in a circuit designed in 0.25µm CMOS technology. A patent application has been filed on this realization.

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