Direct-Digital Modulation (DIDIMO) Transmitter with -156dBc/Hz Rx-Band Noise using FIR structure

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***Abstract*— A direct-digital modulation (DIDIMO) transmitter employing 3-taps 10-bit Finite Impulse Response configuration is proposed and evaluated. FIR-DIDIMO provides simultaneous combination of D/A conversion, up-conversion, power control and also quantization noise filtering at arbitrary offset frequency from the carrier. This makes the circuit suitable for multi-standard transmitters by eliminating the area-consuming analog baseband low-pass filter. Moreover it enables optimum RF noise shaping against various modes and bands requirement. The noise shape adjustment scheme is also detailed in this paper. Using a WCDMA signal, the transmitter achieves 81dB of power control range, EVM of less than 3% from -42dBm to +6.0dBm output power for band I operation with 568.32MHz sampling frequency. The RX band (190 MHz offset) noise floor achieves -156.3dBc/Hz measured with 291mW analog power consumption at +6.0dBm output. WCDMA band II and LTE 20M band1 performances are also demonstrated. The chip is designed and implemented with a low-power 0.13um 1.5V/3.3V CMOS process and the transmitter analog area measures 1.3mm^2.**

I. INTRODUCTION

There is an increasing demand for RF transceivers handling several radio standards (e.g. WCDMA, LTE, GSM and WLAN). In the TX side, a compact transmitter capable for multi-standard is a popular topic. In [4, 5], a highly- digitized transmitter for multi-standard is reported. They are Cartesian transmitters, denoted as a direct-digital RF modulator, that combines D/A conversion and up-conversion functions into arrayed single mixer unit cells. In [4], a unit cell is composed by stacking of an n-type Gilbert up-conversion mixer and current steering D/A converter on top of that. The transmitter performance using WCDMA, EDGE and WLAN signals is examined with the various signal bandwidths according to the standards. Multi-standard capability could be almost fully implemented in the digital part except the RF output matching circuit [4]. It eliminates analog baseband circuitry including analog post filter (low-pass filter after D/A converter) which should be adjusted from standard to standard according to the signal bandwidth and would require chip area for parallel/tunable capacitors for cut-off frequency adjustment. In addition, since digital part can benefit from "technology scaling", the whole transmitter's area and power dissipation can be reduced along with process downscaling. A demonstrated 10-bit digital WCDMA modulator with a sampling rate of 307.2MSPS reaches a RX band noise floor of -144dBc/Hz at -2dBm output power. The noise floor is dominated by its quantization noise from D/A conversion. In [5], by using FIR-like configuration, this transmitter achieves a noise floor of -148dBc/Hz at notched frequency at +5.8dBm output power with 4MHz band width.

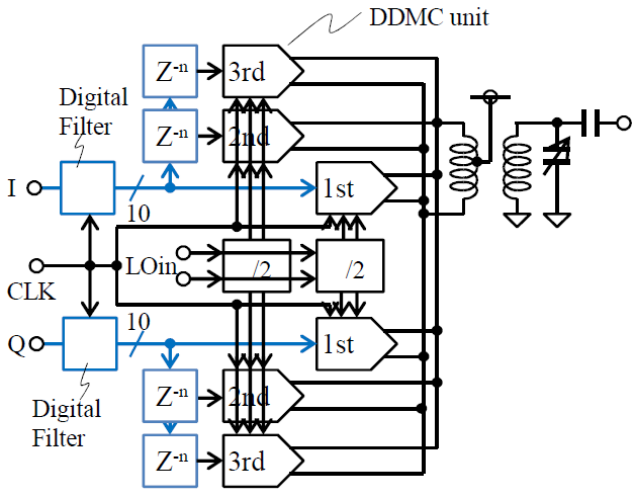

Fig. 1. FIR-DIDIMO Transmitter block diagram described for 3-tap FIR case

Especially in FDD system such as WCDMA, the elimination of a SAW filter between transceiver's TX output and PA also becomes popular. For this purpose, a stringently low TX noise floor such as -156dBc/Hz for WCDMA is necessary at RX band frequencies of the TX output spectrum to avoid desensitization of co-operating RX in the same transceiver [1-3]. The TX-RX frequency separation depends on operating bands (e.g. 190, 80, 95, 45MHz for UMTS band I, II, III, V respectively) and the required RX-band noise level is determined on leakage level from TX to RX via the duplexer. Although the emission levels into air are also regulated by the 3GPP standard, the requirement for TX noise floor is not as stringent as this RX-band noise. For example in [3], a transmitter using direct quadrature voltage modulator achieves -159dBc/Hz at RX band noise, in which analog I/Q base band signal generated by conventional D/A converter and analog low-pass filter are assumed.

So far, a direct-digital modulation transmitter associated with superior RX-band noise performance has not been found in literature. In a direct-digital modulation transmitter, the noise floor level as low as -156dBc/Hz corresponds to 12-bit resolution converter with 500MHz sampling frequency, which would be really challenging. In addition, current source area for a 12-bit DA converter would become quite large. Generally,

when number of bits becomes 2 bits larger, current source area becomes 16 times larger to keep the same static linearity (INL, expressed in LSBs). Therefore a 12-bit DA converter would consume a too large area to justify this architecture.

In this paper, we propose a direct digital modulation (DIDIMO) transmitter with low noise, medium D/A resolution and low power consumption. Here, we use a 3-taps Finite Impulse Response (FIR) configuration, which improves quantization noise performance at the targeted frequency region in the TX output spectrum. This notched low noise frequency area is determined by 2 factors; sampling frequency of D/A conversion and delay time between the compounded converters, both of which are to be controlled arbitrarily to realize the low RX-band noise performance according to the selected band/ mode operation.

The general architecture of FIR-DIDIMO transmitter is described in section II along with the case of 3-tap 10-bit FIR. In section III, we present the CMOS level circuit implementation of the proposed transmitter. The experimental results using WCDMA signal are presented in section IV.

II. ARCHITECTURE

A. FIR-DIDIMO Transmitter

Fig. 1 shows block diagram for one example of proposed FIR-DIDIMO transmitter. This is for the case of 3-tap FIR configuration. The transmitter is I/Q-modulator, which consists of two 32-time up-sampled digital interpolation filters with 10-bit output, six 10-bit direct-digital modulation converters (DDMCs) operating at sampling frequency (568.32MHz), on-chip balun and output matching circuit by capacitor array. Both I and Q branch have 3 DDMCs each and their outputs connect to each other in differential configuration. According to the digital input signal, each unit converter makes the D/A-conversion and frequency up-conversion. Delay blocks expressed z^{-n} are placed among the DDMCs as shown in Fig. 1. In the z-domain, z^{-n} means the delay correspond to n periods of sampling clock. Therefore delayed data is provided for the 2nd and 3rd DDMC. This configuration resembling digital 3-tap FIR filter provides additional discrete-time noise shaping for the quantization noise at the RF frequency. Accordingly, transfer function H(z) of m-tap FIR-DIDIMO is expressed by

$$H(z)=(1+z^{-n}+z^{-2n}+\cdots+z^{-(m-1)n})/m, \qquad (1)$$

where the fundamental frequency of Eq. (1) corresponds to the

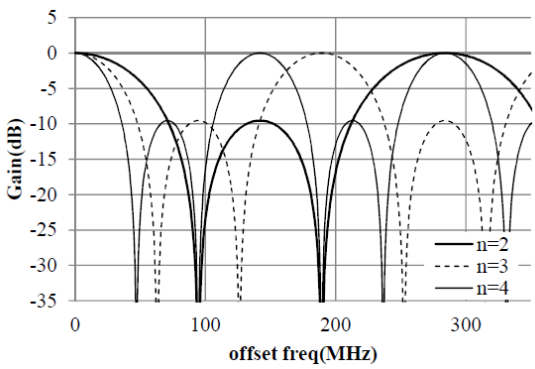

Fig. 2. 3-tap FIR-DIDIMO filter shaping for fs=568.32MHz and n=2, 3, 4

local oscillator (LO) frequency. It is possible to set the notch point at arbitrary offset frequency by choosing sampling frequency (f_s), m and data delay coefficient n. For example, the adopted 3-tap structure with 568.32MHz sampling frequency is still capable to tune its notch frequency by changing n. The filter shape calculated by Eq. (1) with 568.32MHz sampling frequency is shown in Fig. 2 for n=2, 3 and 4. Generally, signal to quantization noise ratio (SQNR) of k-bit DIDIMO transmitter is calculated by Eq. (2).

$$SQNR=+6.02\cdot k+4.77+10\cdot \log_{10}(f_s/2) \qquad (2)$$

The SQNR[dBc/Hz] is in turn filtered by the Gain(m,n,f) in figure 2, resulting in the FIR filtered SQNR.

B. Sampling Frequency

Sampling frequency (f_s) of D/A conversion is also important with respect to spurious emission. If the matching between I and Q branch is perfect, there appear only two types of image components caused by D/A conversion. The image spurious frequencies (F_{imag}) are calculated by Eq. (3) and Eq. (4), where, coefficient i is the order of the image and f_{data} stands for data frequency. The spurious level is limited by Eq. (5).

$$F_{imag}=f_{LO}\pm i\cdot f_s+f_{data} \qquad (3)$$

$$F_{imag}=-f_{LO}+i\cdot f_s+f_{data} \qquad (4)$$

$$G_{imag}=\mathrm{sinc}(i+f_{data}/f_s) \qquad (5)$$

The higher the sampling frequency is, the lower spurious level. Generally, the sampling frequency is chosen as a multiple of the baseband data rate.

C. Noise Shaping Determination

Eq. (1)-(5) can be used to decide the appropriate sampling frequency (fs), number of bits (k), number of taps (m) and delay coefficient (n) which satisfy spurious emission and noise requirements for various applications. Though the higher fs, k and m values the lower spurious and noise, chip area becomes larger. Total current source area of 12-bit DIDIMO (1-tap) is 16/3 times larger than that of 3-tap 10-bit FIR-DIDIMO which keeps the same bias condition and static linearity target (INL) and provides good SQNR performance at the aimed offset frequency.

Here, fs=568.32MHz, k=10bit and m=3tap are chosen for WCDMA band I specification, in which the offset frequency is 190MHz. The FIR-DIDIMO transmitter is to provide +161.5(dBc/Hz) FIR filtered SQNR at 190MHz offset where 12dB attenuation is reasonably presumed by the FIR calculation shown in Fig. 2 with n=2. It is low enough for SAW-less TX noise requirement (-156dBc/Hz) discussed in Section I.

In addition, FIR-DIDIMO transmitter could be applied for more stringent noise requirements, which for example exists for GSM application in GSM850/EGSM900 bands (-162dBc/Hz). For this case, 6-tap 11-bit transmitter with 450.67MHz sampling frequency is to provide +166.5(dBc/Hz) SQNR from 20MHz offset to 120 MHz offset according to the similar calculation using Eq. (1)-(5).

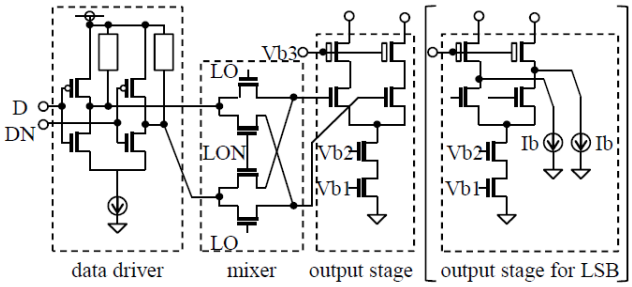

Fig. 3. DDMC 1 bit unit cell

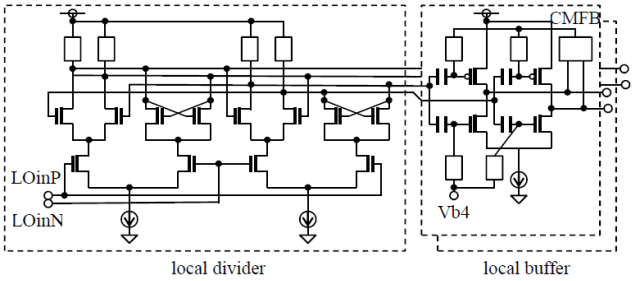

Fig. 4. Local Oscillator divider and circuit

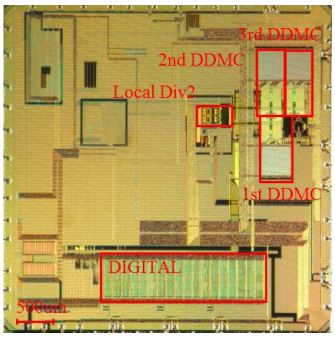

Fig. 5. Chip Micrograph

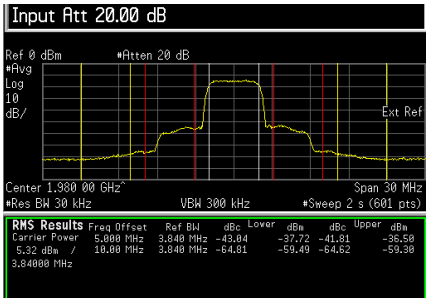

Fig. 6. WCDMA ACLR

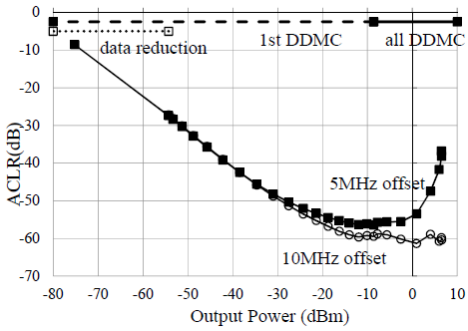

Fig. 7. WCDMA ACLR over all power control range

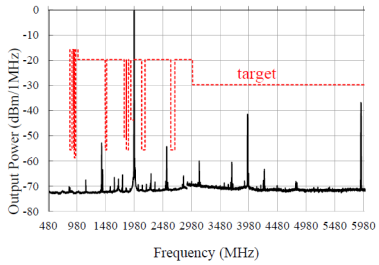

Fig. 8. Measurement WCDMA output spectrum

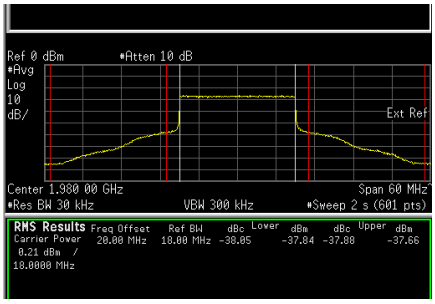

Fig. 9. LTE20MHz ACLR

III. Circuit Implementation of 3-tap 10-bit FIR-DIDIMO Transmitter

Test chip is designed using a low-power 0.13um CMOS 1.5V/3.3V process. For high speed digital filters, data decoders and delay blocks shown in Fig. 1, low-Vt MOS digital standard cell is used.

A. DDMC

As shown in Fig. 3, a DDMC 1 bit unit cell, based on current steering D/A converter consists of data driver, passive mixer and output stage. To ensure data synchronization, data latches are placed before data drivers. Output current of the unit cells is controlled by bias voltage Vb1 coming from reference bias circuit. For reliability reason, thick oxide transistor is adopted for the cascode transistor of the output stage.

For 10-bit DDMC unit, “3+7” segmentation architecture is adopted. The 7 LSBs are binary coded while the remained 3 MSBs are thermometer (unary) coded employing row-column binary-to-thermometer decoding. In 3 LSBs of the binary part, gate width of differential pair and cascoding transistors are not able to be ideally sized down by process limit. Since this causes rise and fall delay of output current waveform, unit cells with bypass current as shown in the right side of Fig. 3 are adopted for the 3 LSBs. Data driver and output stage operate at 1.5V and 1.9V respectively.

B. Local Oscillator Dvider

As shown in Fig. 4, the LO divider consists of conventional current mode divide-by-2 logic and current-inverter based LO buffer. This structure provides high drivability with large voltage swing, even at low voltage supply by separating biases using AC coupling. As shown in Fig. 1, two separated I/Q-dividers are used. The 1st divider connects to the 1st DDMC and the 2nd divider connects to the 2nd and the 3rd DDMC. This 2nd divider is turned off with the 2nd/3rd DDMC below the middle output power range for saving power consumption.

C. Output Power Control

For output power control, two bias reference circuits are implemented. One provides bias for the 1st DDMC, the other provides bias for the 2nd and 3rd DDMC respectively. This double bias-controlled structure provides approximately 60dB output power control range. Besides, amplitude reduction of

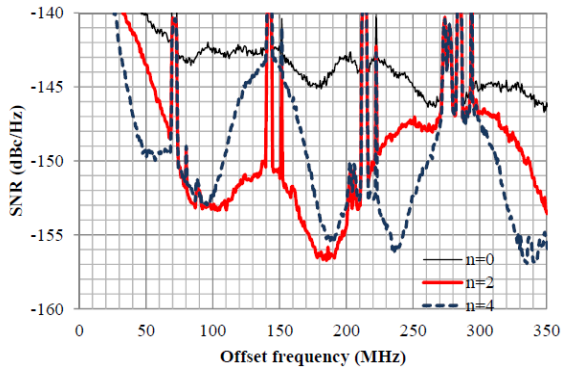

Fig. 10. Measured WCDMA noise performance

digital input I/Q signals provides additional power control range below the lower limit of this bias circuits control range.

IV. Experimental Results

A test chip was fabricated in a low-power 0.13um CMOS 1.5V/3.3V process. The die size is 4.52mm x 4.52mm and its micrograph is shown in Fig. 5, where the active area of the analog circuit blocks including the on-chip matching is 1.3mm^2 and digital blocks including Serial/Parallel circuit is 1.2mm^2, approximately.

The 12 bit I/Q digital baseband signals are fed together with their sampling clock into the IC via a LVDS (Low Voltage Differential Signals) interface. After this interface the signals are converted to parallel signals and fed into the interpolation digital filters.

The measured WCDMA Adjacent Channel Leakage Ratio (ACLR) spectrum with 1.98GHz carrier frequency, 568.32MHz sampling frequency and data delay coefficient n=2 is shown in Fig. 6. With channel power of +6.0dBm (0.64dB cable loss extracted), ACLR is -41.8dBc at 5MHz offset and -64.6dBc at 10MHz offset, respectively. ACLR against total output control range is shown in Fig. 7. For more than -9dBm output power, all of the DDMCs are enabled. Operation from -54dBm to -9dBm, only the 1st DDMCs are enabled. Below -54dBm, amplitude reduction of digital input I/Q signals is done to obtain minimum power of -75.2dBm. The modulator resultantly achieved 81.2dB power control range. The EVM less than 3% is observed from -42dBm to +6.0dBm.

Fig. 8 shows the output spectrum compared to the emission target based on 3GPP specification, in which duplexer attenuation of 30dB up to 3GHz or 20dB above 3GHz is taken into account. All the image components calculated by Eq. (3) and Eq. (4) are observed to be below this target.

Fig. 10 shows the measured noise spectrum with n set to 0, 2 and 4 in WCDMA. In each case, the notch frequencies exactly correspond to the simulation results shown in Fig. 2. The SNR with 3.84MHz band width at 190MHz offset is -144.0dBc/Hz when n set to 0 (without FIR filtering) and -156.3dBc/Hz with 12.3dB FIR filter attenuation when n set to 2. Still this floor (-156dBc/Hz) seems limited by digital noise floor generated inside the chip, this value is low enough to be applied as TX SAW less transmitter.

TABLE I. Summary of Measured WCDMA Performance

Parameter	This transmitter			[4]	[5][a]
Process	0.13um CMOS			0.13um CMOS	0.13um CMOS
Resolution /fs	3-taps 10-bit / 568.32MHz			10-bit / 307.2MHz	4-taps 7-bit / 85MHz
LO freq.	1.98GHz			1.92GHz	850MHz
Power Consumption	Analog Digital Output	291mW/74mW 81mW/74mW +6dBm/-9dBm		92mW/46mW 65mW/65mW -2dBm/-45dBm	N/A N/A +6dBm
Suppression	Carrier : -54dBc@+6dBm Image : -40dBc@+6dBm			-56dBc@+2dBm -43dBc@+2dBm	N/A N/A
Gain control	81dB			> 90dB	N/A
ACLR (dBc)	5MHz : -42dBc @+6dBm 10MHz:-65dBc @+6dBm			-58dBc @-2dBm -61dBc@-2dBm	-35dBc@+6dBm -47dBc@+6dBm
EVM	< 3%			< 2%	-27.4dB
Noise (dBc/Hz)	@offset	n=0	n=2	N/A	n=N/A
	45MHz	-139.5	-142.6	N/A	-148[b]
	190MHz	-144.0	-156.3	-144	N/A
	BW	3.84MHz		3.84MHz	4MHz
Active area	Analog 1.3mm^2/ Digital 1.2mm^2			Analog 1mm^2	Chip 2.3mm^2

a) Not measured with WCDMA input, but with 16QAM (4MHz BW) . b) Measured with a baseband tone.

To check the flexibility of the transmitter, various standards with the setting of LO, fs and n were measured. WCDMA band II (LO=1880MHz, fs=568.32MHz, n=3) and LTE20MHz band 1 (LO=1980MHz, fs=552.96MHz, n=2, BW=18MHz) performance were measured. In WCDMA band II, the SNR at 80MHz offset is -151dBc/Hz and ACLR is -41dBc at 5MHz offset with channel power of +6dBm. In LTE20MHz band 1, the SNR at 190MHz offset is -152dBc/Hz and E-UTRA ACLR is -38dBc (shown in Fig. 9) with channel power of +1dBm.

A summary of measured WCDMA performance of the transmitter prototype is provided in Table I.

V. Conclusion

A Finite Impulse Response configuration Direct-Digital Modulation transmitter is proposed. This 3x10-bit I/Q FIR configuration performs: DA conversion, up-conversion and FIR filtering of the quantization noise, resulting in a significant area and power reduction compared to a straightforward 1x12-bit I/Q implementation with similar noise level. Implemented 3-taps 10-bit FIR-DIDIMO transmitter shows +6dBm output with -156dBc/Hz noise at 190MHz offset and with 1.4% power efficiency.

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