Active RFID: Perpetual Wireless Communications Platform for Sensors

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***Abstract*— A highly integrated 2.4GHz wireless communications platform for an Active RFID system supporting perpetual operation in indoor lighting conditions is presented. The system requires no external components except an antenna, two BAW resonators, a small solar panel, and a rechargeable battery. It is implemented in 65nm CMOS, comprising of a BAW-based transceiver, digital baseband and integrated power management unit. Including converter losses, the system consumes 850nW when idle, 155µW in receive mode, and 4.7mW in transmit mode.**

I. Introduction

Active RFIDs [1] supplement the low cost and ease of use of traditional RFIDs with an enhanced interrogation range and superior processing capabilities, as essential for usage as wireless sensor nodes. Active RFID links combined with advanced sensing platforms [2] can substantially extend the applicability of wireless sensing networks. This work presents a highly integrated prototype of an active RFID platform, combining advanced radio topologies for low power with fully integrated power conditioning to provide high efficiency over a very wide range of operating conditions.

The paper sequentially addresses the architectural design of the system, the individual circuit blocks, and the measurement results of the fabricated prototype. It concludes with a summary of the key results.

II. Architecture Design

With the recent push for energy efficiency in buildings, transportation and logistics, and industrial processes, wireless sensor networks (WSN) have become a promising technique to help monitor the world and prevent waste. In order to be most effective, these sensors need to be inexpensive, easy to deploy, and require little to no maintenance after installation. This work proposes one way to achieve these goals by utilizing highly scaled CMOS, recent advances in MEMS components, and energy harvesting. Careful system design with multiple modes of operation allows a wireless communications platform to operate perpetually by harvesting ambient energy from its environment through solar cells to target indoor sensing applications that require a moderate range of roughly 10 meters and moderate data rates.

This prototype has been implemented in a standard 65nm digital CMOS process with metal-insulator-metal (MIM) capacitors. The only external components are a 25x10mm solar panel, a small NiMH battery for temporary energy storage, a printed antenna, and two bulk acoustic wave (BAW) resonators. The wireless link supports 100kbps of on-off keying (OOK)-modulated Manchester-coded data. The block diagram of the chip is shown in Fig. 1.

To ensure perpetual operation with the limited energy supply from the solar cells, the system requires an average power of 3µW under the duty cycle conditions between the three modes of operation specified in Fig. 2. During the sleep mode, the only active components are a wakeup timer (controlling the period of the sleep cycle), system state registers, and the power management unit (PMU). Upon wakeup, the receiver and synchronizer listen to the channel for Manchester-encoded data and wake the protocol processor upon detecting synchronization. If a valid tag request is received, the protocol processor prepares a packet

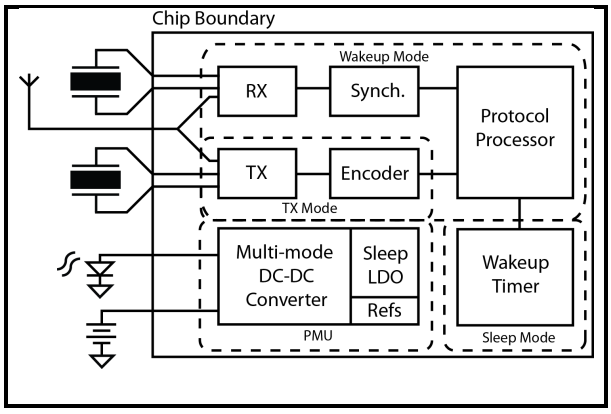

Fig. 1 Active RFID Block Diagram

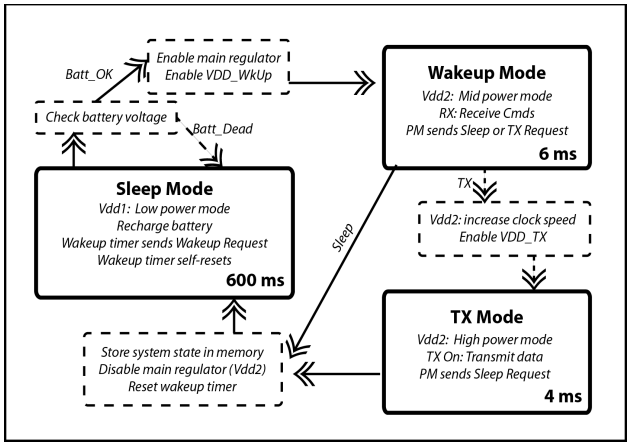

Fig. 2 Example operational modes

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acknowledging the reader and transmits its unique identification code during TX mode. Otherwise, the system reenters sleep mode and resets the wakeup timer.

The solar panel, consisting of 4 cells in series, provides an open-circuit voltage up to 2.8V and about 7µW average power in typical office light. The harvested energy is directly stored on the battery. To minimize active power, circuit blocks operate at reduced supply voltages ranging from 450mV to 650mV. A fully integrated switched capacitor (SC) DC-DC converter [3] was chosen as the primary topology for voltage conversion to provide high efficiency across the wide range of active operating loads, from the 110µW RX to the 3.2mW TX.

III. Circuit Design

A. Power Management Unit

Fully integrated SC DC-DC converters, incorporating all necessary switches and passive components on-chip, are well suited for millimeter-scale applications where minimizing system complexity, size, and cost are critical. The primary SC converter utilizes two topologies, providing both a 2:1 and a 3:1 mode to account for potential battery voltages from 1.2V to 1.8V, chosen by an internal comparator and an on-chip voltage reference. MIM devices are used for the flying capacitors, and all switches are standard low-voltage MOS devices.

With sensitive components such as the receiver on the same die, minimizing the output voltage ripple is essential. This can be accomplished either by increasing switching frequency at the cost of efficiency, a larger output filtering capacitor at the cost of die area or external components, or a series linear regulator again at the cost of efficiency. A multiple interleave method [4] was selected to enable a higher effective frequency while still allowing for good efficiency, as shown in Fig. 3. This approach uses a 16-phase interleaved topology with the converter partitioned into identical smaller units that are switched on symmetrically skewed clock phases, generated by an 8-stage, fully differential ring oscillator (RO) that is digitally controlled between 800kHz and 15MHz. The wide tuning range allows the converter to operate at the optimal frequency that reduces switching losses for each mode of active operation (i.e. Wakeup, TX).

The digital loads are designed to run at a minimum supply voltage of 550mV. Voltage regulation is achieved by first implementing a coarse control by choosing the proper unloaded conversion ratio (i.e. 2:1 or 3:1), then finely controlled by a hysteretic feedback loop that reduces the effective clocking frequency, minimizing gate and dynamic losses. Sensitive components, such as the analog front end of the RX and its local oscillator (LO) are placed on a cascaded LDO linear regulator to further suppress the effects of ripple at a nominal supply voltage of 500mV. In addition to the main DC-DC converter used during active modes, a ultra low power LDO linear regulator provides the nominal 450mV supply needed during sleep mode, allowing the sleep state registers, wakeup timer, and power manager to operate, while minimizing the leakage from the wakeup supply by turning it off.

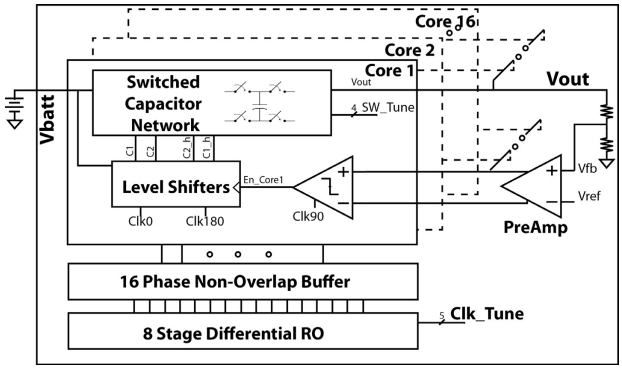

Fig. 3 16-Phase Switched Capacitor DC-DC Converter

The solar cell interface was designed with minimal overhead in order to function even in low light conditions. The proposed implementation uses an on-chip blocking diode in series with the battery as a charging circuit. The diode also blocks reverse current from the battery flowing into the module at night. The battery voltage is monitored with a comparator clocked using the 2 Hz wakeup signal from the duty-cycle oscillator. Overvoltage protection is required to prevent damage to the battery and is provided by a parallel shunt MOSFET that bypasses current to ground when the battery is fully charged. If the detected battery voltage is too low, the system remains in sleep mode until enough energy is harvested and stored.

B. Transceiver

Upon wakeup from sleep mode, the RX listens for a wakeup command from the reader. The uncertain-IF receiver, based on the topology from [5] and illustrated along with the TX in Fig. 4, utilizes a BAW resonator to provide both a matching network and filtering directly following the antenna. A passive mixer down-converts the signal to a wideband IF channel, providing good noise performance with low power consumption. The first IF stage can be viewed as an LNA of the receiver, as its noise performance dominates the overall noise figure. Subsequent IF amplifier stages provide additional gain, for a total of roughly 60dB of voltage gain, to bring the signal to a convenient level for sampling, while limiting the bandwidth of the IF signal to 30 MHz. Due to the high gain and difficulty in completely suppressing voltage ripple caused by the PMU, all gain is performed with fully differential

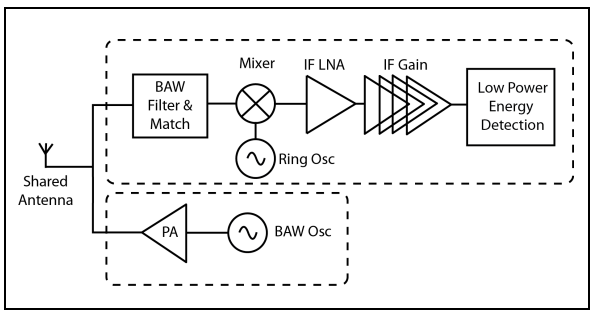

Fig. 4 Block diagram of the transceiver.

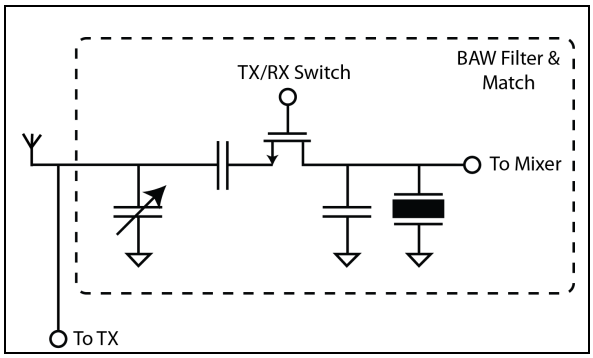

Fig. 5 Schematic of the matching network and TX/RX switch for sharing the antenna.

circuits to improve supply rejection.

The OOK data at IF is directly sampled using two comparators operating at 30MHz, which register a 1 when the magnitude of the signal exceeds a programmable threshold. The result of this absolute value operation is stored into a 100-bit register, on which a majority vote operation is performed. This technique effectively oversamples the incoming signal and provides averaging, which brings the signal down from the IF frequency to baseband, while filtering some of the additional noise injected from the wideband IF [6].

The TX utilizes a BAW Pierce oscillator to provide the RF frequency, which directly drives the power amplifier (PA). The PA is biased in class B and is modulated by switching the gate bias on and off to provide OOK signaling. A board antenna is co-designed with the circuit to provide the optimal impedance of 140Ω for providing 0dBm of output power from the nominal 550mV wakeup mode supply, following a similar approach as [7]. By matching the output impedance to the desired power level, this topology avoids the need for a lossy matching network and improves efficiency.

All bias voltages and clocks are generated on-chip. To facilitate sharing the antenna between the TX and RX, a MOSFET switch has been added in the matching network as shown in Fig. 5 to decouple the RX BAW from the antenna port during transmit mode, making the RX load appear to simply be a shunt capacitance to the transmitter.

C. Digital Baseband

The protocol processor and wakeup timer are implemented using synthesized standard CMOS logic to provide control for the system. The wakeup timer uses an ultra low power relaxation oscillator to generate a 2Hz pulse, which turns on the PMU's wakeup mode and initiates the RX to listen for a signal. Because this timer is not duty cycled, it is critically important that it uses a minimal amount of power, which directly impacts the overall power budget of the system. The protocol processor, which fully supports the standard in [1] with its data layer, includes a synchronizer, encoder and decoder, packet detection and assembly logic, random number generator, and state machines to determine the presence of incoming data and generate packets for response.

A broadcast command, which addresses every device in a network, requires the wakeup sequence to be long enough to make sure every device receives the signal and wakes from sleep mode. To minimize the waiting energy, linear coding is introduced in wakeup sequence, such that each device can identify the proper time to wake up for the command. Additionally, a random number back off strategy is used to minimize the excess energy due to collision.

IV. Measurement Results

The PMU achieves the nominal supply voltages for all modes of operation. The low power sleep mode converter, along with the wake-up timer, consumes 600nA from a 1.4V nominal battery. When the wakeup timer signals the system to turn on, the supply voltage reaches its steady state within 100µs, initiating a 6ms wakeup period for the system to listen to incoming RF signals. Fig. 6 shows the transient response of the wakeup clock and the wakeup power supply. At the nominal battery voltage of 1.4V, during the lower current wakeup mode, the SC converter operates in 2:1 mode with 68% peak efficiency with a 50mV pk-pk ripple, as shown in Fig. 7. For the RX front-end loads, the ripple is further reduced to less than 10mV using a cascaded LDO. During the high current TX mode, it operates with 71% peak efficiency. The SC converter provides a 1.75x improvement over using a only an LDO.

The RX achieves a 10^{-3} bit error rate (BER) sensitivity of -66dBm at 100kbps. The measured RX sensitivity is worse than expected from simulation due to an unexpected

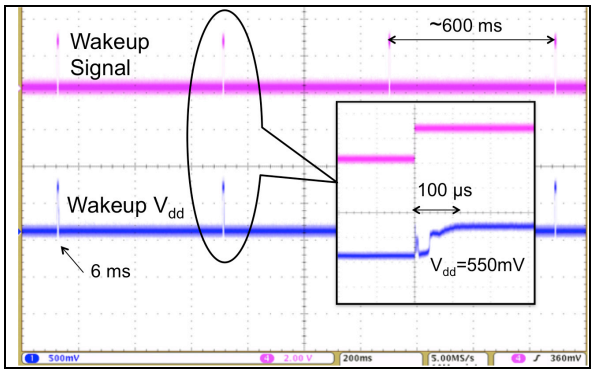

Fig. 6 Measured duty-cycled wake-up operation and supply startup transition

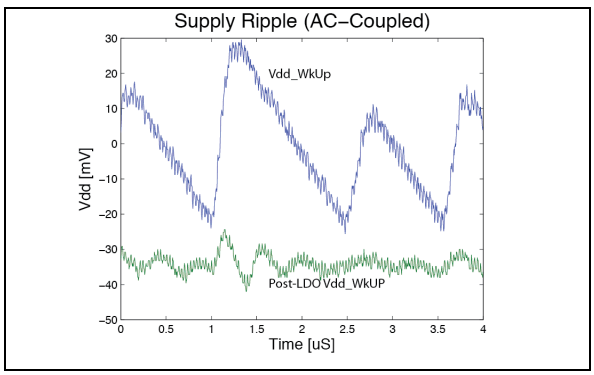

Fig. 7 Measured ripple at output of SC converter and post LDO during wakeup mode

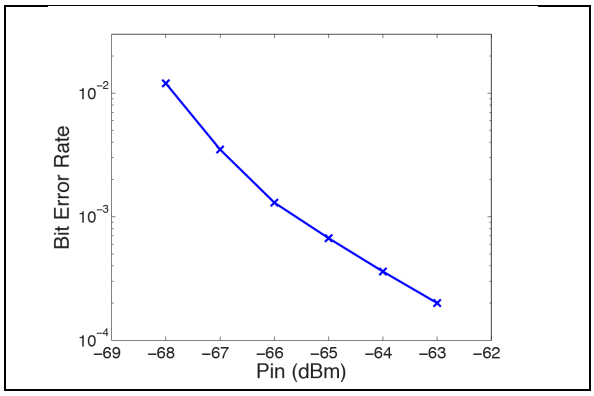

Fig. 8 Measured BER of the receiver at 100kbps.

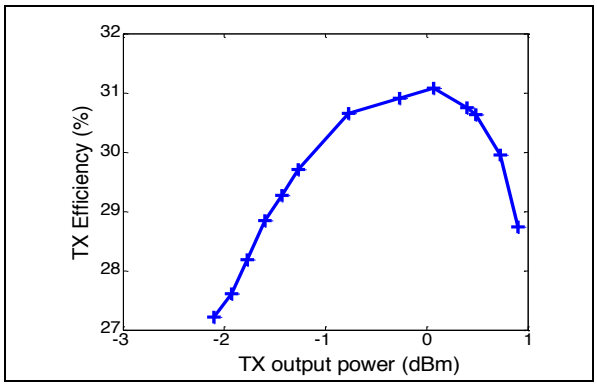

Fig. 9 Measured TX efficiency versus output power.

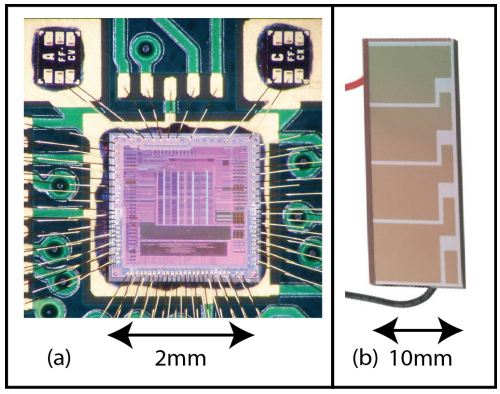

Fig. 10 (a) Chip bonded with 2 BAW resonators (b) Solar panel with 4 cells in series

Battery Voltage	1.2-1.8V
Die Size	2mm x 2mm
Process Node	65nm CMOS
Core Supply Voltage	550mV
RF Supply Voltage	500mV
RX Sensitivity	-66dBm
TX Efficiency	31%
TX Output Power	0dBm, nom.
Carrier Frequency	2.47GHz
Modulation	OOK
Data Rate	100kbps Manchester

Table 1 Specifications Summary

capacitive coupling from the sampling circuit block. The analog front-end consisting of the mixer, LO, and IF gain consumes 48µW. The sampler, majority vote, synchronizer, and protocol processor consume an additional 61µW. Due to a minor flaw in the programming of the majority vote logic, for testing purposes, this block was bypassed and re-implemented with an FPGA in an Opal Kelly XEM3001 board off-chip. Fig. 8 shows the measured BER of the RX across input power while supplied by the on-chip PMU. The TX consumes 3.3mW while outputting 0dBm, thus resulting in a TX efficiency of 31% as shown in Fig. 9. The maximum data rate supported by the TX is 350kbps, while the RX supports a maximum of 300kbps, limited by its 30MHz sampling rate and 100 times oversampling.

A die photo of the measured prototype, along with the attached BAW resonators, and photo of the solar panel is shown in Fig. 10. Additionally, a summary of the major performance specifications and implementation details are shown in Table 1.

V. Conclusions

This work presents a highly integrated, ultra-low power communications platform, including a complete digital baseband and transceiver, for an Active RFID. Full integration of the power management unit along with a top-down focus on energy management enables perpetual operation from harvested indoor solar energy.

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