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A 12b 50MS/s 2.1mW SAR ADC with Redundancy and Digital Background Calibration

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Abstract—A 12-bit 50MS/s SAR ADC implemented in 65nm CMOS technology is presented. The design employs redundancy to relax the DAC settling requirement and to provide sufficient room for errors such that the static nonlinearity caused by capacitor mismatches can be digitally removed. The redundancy is incorporated into the design using a tri-level switching scheme and our modified split-capacitor array to achieve the highest switching efficiency while still preserving the symmetry in error tolerance. A new code-density based digital background calibration algorithm that requires no special calibration signals or additional analog hardware is also developed. The calibration is performed by using the input signal as stimulus and the effectiveness is verified both in simulation and through measured data. The prototype achieves a 67.4dB SNDR at 50MS/s, while dissipating 2.1mW from a 1.2V supply, leading to FoM of 21.9 fJ/conv.-step at Nyquist frequency.

I. INTRODUCTION

There is a growing demand for low-power, high-speed and high-resolution A/D converters for applications such as wideband wired/wireless communication, software radio and millimeter-wave imaging systems. For many years, the successive-approximation-register (SAR) ADC mostly appears in low-speed and low-power applications. The unprecedented improvement in speed and energy efficiency of scaled CMOS technologies helps expand the SAR architecture into the medium-to-high-speed application domains that are traditionally designed using the flash or pipelined architectures. Along with other benefits, such as good digital compatibility, excellent power and area efficiency, and rail-to-rail input swings, the SAR architecture has become one of the more popular topologies.

Recent SAR designs have demonstrated outstanding bandwidth (running at hundreds of MS/s to GS/s range) and superior energy efficiency (with FoM < 100 fJ/conv.-step), but the resolution is limited to less than 10b ENOB. While scaling benefits speed and power efficiency, it does not improve capacitor matching and the reduced supply headroom makes designing high-resolution ADCs more difficult. Moreover, reference voltage settling also places stringent settling requirements that limit the maximum operating speed. In this work, redundancy and calibration are introduced in the design to help alleviate the settling and the mismatch problems. A sub-radix-2 SAR ADC is presented here with several new contributions. First, we incorporate tri-level based switching [1] into a new split capacitor architecture to achieve higher energy efficiency. Second, we introduce a new method to implement redundancy

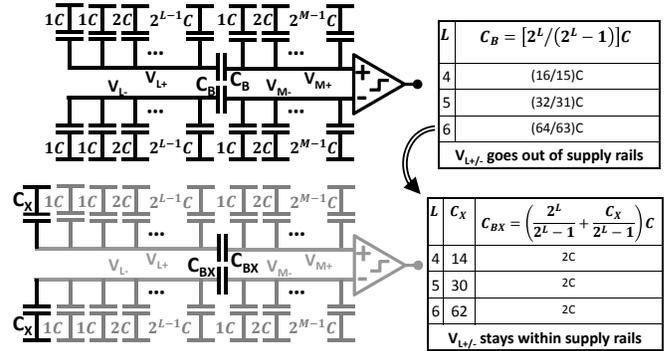


Fig. 1. Split-capacitor architecture.

directly into the SAR ADC with symmetric error-tolerance windows without increasing design complexity and area overhead. Third, a new code-density based background calibration algorithm is developed for this architecture to calibrate against capacitor mismatches.

II. ADC ARCHITECTURE AND IMPLEMENTATION

A. Split Capacitor Architecture

In a SAR design, the input loading and the area/layout complexity of the DAC increase exponentially with the number of bits. To avoid this in a high resolution design, a split-capacitor array is typically employed as shown in Fig. 1. A common problem associated with split-cap is that the parasitic capacitance at the output of the sub-DAC and the fractional value of the bridge capacitor both add uncertainty in the gain of the sub-DAC, and hence is a major limiting factor in accuracy. Another problem in a split-cap array is that when the inputs are rail-to-rail, the output of the sub-DAC (V_L nodes) can go beyond the rails [2]. To resolve the matching problem, Agnes *et al.* in [3] replaces the fractional bridge capacitor by a unit capacitor, but the design suffers from a constant gain error. Chen *et al.* in [4] pick a value of the bridge capacitor that is slightly larger than the desired size. A tunable capacitor is then added on the LSB side of the array to adjust the total weight of the sub-DAC in order to calibrate out the mismatches. To resolve the over-range problem, Yoshioka *et al.* in [2] reduce the input range at the cost of SNR.

In our prototype, an additional grounding capacitor C_X is added to the V_L nodes as shown in Fig. 1. By properly choosing the value of C_X , the value of the bridge capacitor

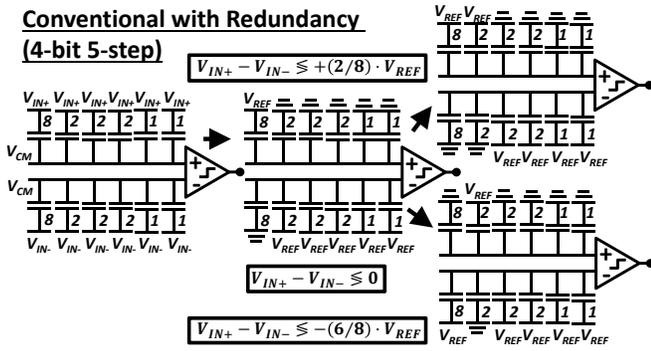


Fig. 2. Redundancy implementation using a conventional switching scheme. It has unequal error-tolerance windows during the “up” and “down” transition.

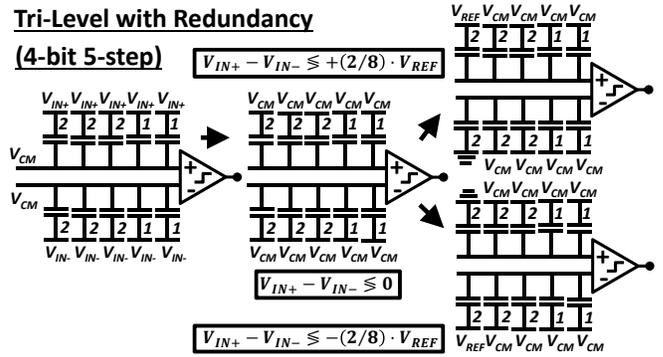


Fig. 3. Redundancy implementation with a tri-level switching algorithm. It has symmetric error-tolerance windows and 93% better energy efficiency.

can be an integer value. As an example, if the LSB DAC has 4-bit resolution ($L = 4$), when C_X is chosen to be 14, the bridge capacitor C_{BX} has an integer value of 2. Moreover, since the size of the C_X capacitor is approximately equal to the sum of the remaining capacitors on the sub-DAC, the swing on V_L nodes is effectively reduced by half, thereby removing the over-range problem and allowing rail-to-rail input swing. The SNR is not affected because only the sub-DAC output swing is reduced in half. The uncertainty in the weights of sub-DAC capacitors is resolved by digital calibration.

B. Redundancy Implementation

Redundancy helps improve conversion rate by allowing room for errors, especially for large voltage jumps during transitions of the first few MSBs. A previous approach introduces redundancy into the SAR algorithm at the cost of extra complexity and power [5]. The design requires one decoder unit for each of the 2^N capacitors, row and column thermometer decoders, and an arithmetical unit to calculate the next decision level. Another technique bypasses such complexity and implements the redundancy algorithm directly by sizing the capacitors with a sub-binary ratio [6]. The technique in [6] allows the design to incorporate redundancy directly without the previous complexity, but the search steps become asymmetric, thus the tolerance to errors also becomes asymmetric. For example, to implement sub-binary search steps equal to $[8, 2, 2, 2, 1]$, the capacitors in the DAC are sized proportional to the desired stepping sizes, as shown in Fig. 2. After the first comparison, which is the sign bit, the input is compared with either $+(2/8)V_{REF}$ or $-(6/8)V_{REF}$, stepping up/down by different amounts. In our prototype, we incorporate redundancy into tri-level based switching as shown by an example in Fig. 3. With this new approach, the stepping size during the sub-binary search is directly proportional to the sizing of the capacitors. After the first comparison, the input is compared with $(\pm 2/8)V_{REF}$, stepping up/down by the amount equal to the size of the first capacitor in the DAC.

Fig. 4 shows the decision levels along with their highlighted error-tolerance windows (ϵ_t). Using the conventional switching scheme [6], the stepping sizes and the error-tolerance windows are asymmetric, while in our work, they are symmetric around

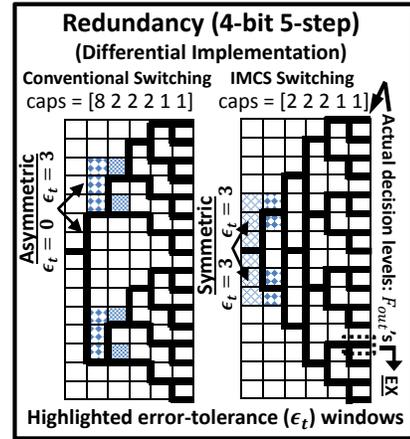


Fig. 4. Comparison between implementing redundancy using the conventional versus tri-level switching algorithms.

each decision level. The asymmetry implies that errors made in one direction can be corrected while it cannot be corrected in the other direction. In real implementation, the input has equal likelihood of making errors in either direction. If the error tolerance windows are asymmetric, then redundancy algorithm would not be as effective in correcting dynamic switching errors as it was originally designed for. Combining the tri-level switching algorithm with redundancy not only avoids the complexity in [5] to achieve symmetric search, but the algorithm also achieves 93% better energy efficiency compared to using a conventional switching algorithm.

C. Digital Background Calibration

A new code-density based calibration algorithm is developed for the redundant search algorithm. It can run in the background at the start of the ADC operation. Unlike the approach in [6], this new digital calibration scheme does not require injection of a calibration signal, a redundant channel or a reference converter to calibrate against. In an N -bit M -step redundant SAR ADC (in which $M > N$), the actual decision levels (F_{out} 's) are a function of actual capacitor values and

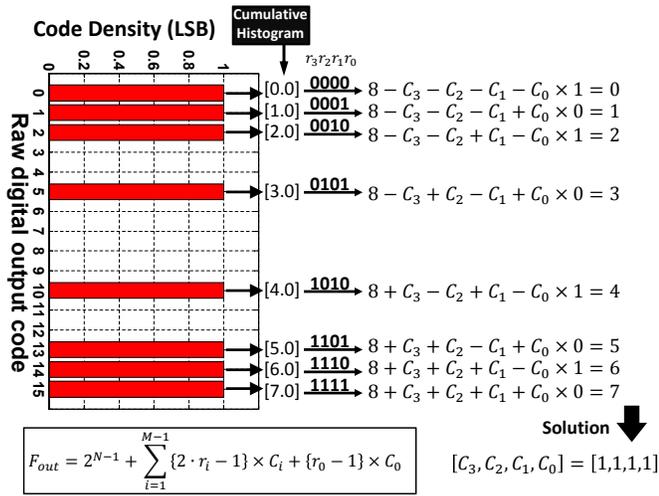


Fig. 5. Demonstration of the new digital background calibration algorithm.

raw output bits (r_i 's) as given in Equation 1.

$$F_{out} = 2^{N-1} + \sum_{i=1}^{M-1} C_i \times (2 \times r_i - 1) + C_0 \times (r_0 - 1) \quad (1)$$

The calibration algorithm finds the true weights (C_i 's) that map the raw output bits into an N -bit digitalized output accurately. A histogram is created by counting the number of occurrences of the 2^M raw output codes. Because of redundancy, many codes never show up at the outputs. If the input signal is uniformly distributed over the full scale and if the ADC is noise free, with enough samples, the number of occurrences of each code is proportional to its bin width; therefore, the ratio of the counts to the total number of samples can estimate the ratio of bin width to the full input scale. Fig. 5 shows a simple example that demonstrates the calibration procedure. Many code bins (bins 3, 4, etc.) are empty due to redundancy. The counts are accumulated to form a cumulative histogram, from which estimates of the actual decision levels (F_{out} 's) for each code bin are obtained. With F_{out} 's and the raw output bits, an equation associated with each code bin is formulated. By subtracting the neighboring equations and putting the results into a matrix form, we obtain a sparse matrix filled with mostly 0's and some entries with ± 1 and ± 2 . Even though the size of the matrix can grow exponentially with the number of bits, since it is a sparse matrix with only a few distinct elements, techniques such as the Markowitz reordering can be used to minimize the fill-in and solve the matrix efficiently. As shown in Fig. 5, we are able to obtain the actual capacitor sizes by solving these equations.

For input signals with non-uniform probability density, the histogram is locally normalized over a small input range for which the probability density of input remains reasonably constant, which makes the calibration independent of the input signal waveform. It can be shown that, with enough samples, random noise does not affect the capacitor value extraction. The calibration is tested with a sine wave, ramp, and uniformly

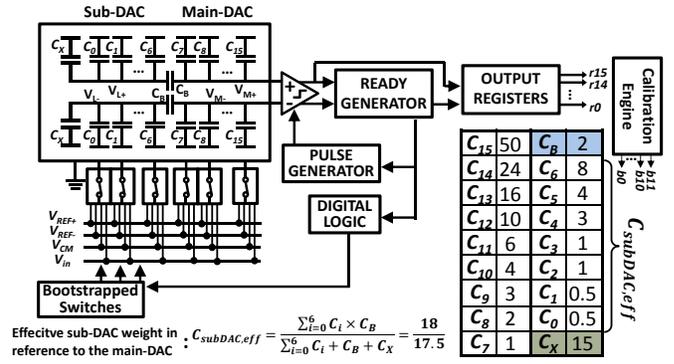


Fig. 6. The overall architecture of the prototype ADC.

random inputs without prior knowledge of the input and is shown to be insensitive to the input waveform.

III. MEASUREMENT RESULT

Fig. 6 shows the overall architecture of the ADC. An asynchronous implementation, similar to [7], is used to speed up the sampling rates and to avoid large jitter by not bringing a high speed clock from off chip. Digital logic circuits, such as the ready generator, pulse generator and digital controls, are designed using dynamic logic to improve energy efficiency and speed. No static pre-amplifier is placed in front of the latch comparator to further increase the sampling rate. Bootstrapped switches are used for all reference voltages to improve linearity and all capacitors are sized to be integer related.

Two identical channels are time-interleaved. Sixteen raw output bits are generated for 12-bit effective resolution. The calibration is done off chip. The estimated calibration power is added to the total power consumption. The prototype ADC is fabricated in standard 1P9M 65nm LP CMOS with 1.2V supply. The active die area is 0.083mm^2 ($330\mu\text{m} \times 125\mu\text{m} \times 2$). The die micrograph is shown in Fig. 7. The implementation allows full input swing ($2.4V_{p-p}$) because of the C_X capacitor. The DAC is implemented with standard MOM cap with a total capacitance of 1.6pF . Several chips are measured and all the measurement is done at room temperature.

While the ADC operates at 50MS/s, a 24.7MHz full-scale sine wave input is used to test the static and dynamic performance. Fig. 8 shows the measured DNL and INL before and after the calibration. Before calibration, the maximum DNL and INL errors are $+1.3/-1.1\text{LSB}_{12}$ and $+14.3/-14.0\text{LSB}_{12}$, respectively. The linearity is mainly limited by the capacitor mismatch. Normal sine wave input is used here as the calibration stimuli and 1 million data points are collected. After calibration, the maximum DNL and INL errors are reduced to $+0.5/-0.7\text{LSB}_{12}$ and $+1.0/-0.9\text{LSB}_{12}$, respectively. Fig. 9 shows the measured dynamic performance, based on 8192-point FFT. Before calibration, the ADC achieves 52.4dB of SNDR, 51.9dB of SFDR and 8.2b ENOB; after calibration, the ADC achieves 67.4dB of SNDR, 78.1dB of SFDR and 10.9b ENOB. The SNDR/SFDR versus input frequency at 50MS/s and the performance summary are provided in Fig. 10.

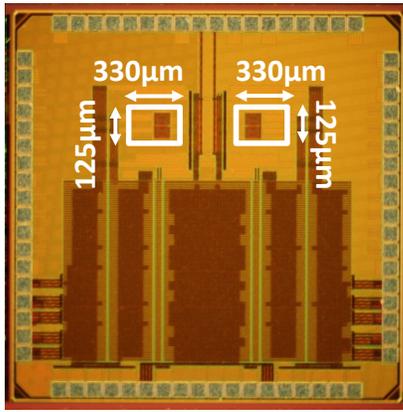


Fig. 7. Micrograph of the ADC chip in standard 65nm LP CMOS technology.

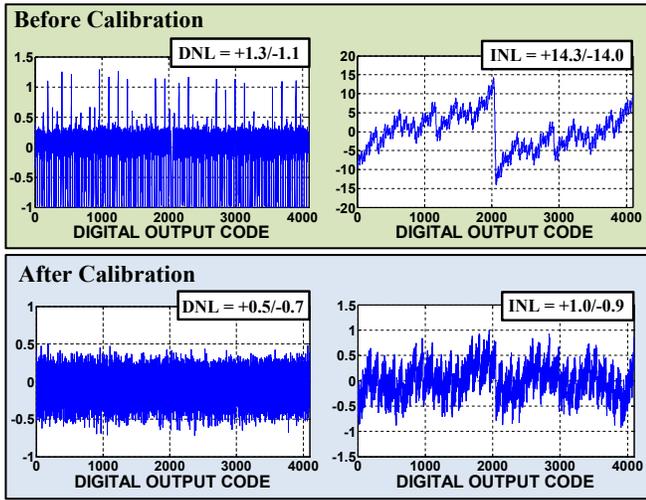


Fig. 8. Measured DNL/INL plot with 1.2V supply at 50MS/s with a 24.7MHz input signal.

Total power consumption including the estimated calibration and reference power is 2.1mW for 21.9fJ/conv.-step FoM. Fig. 11 shows the comparison with the state-of-the-art.

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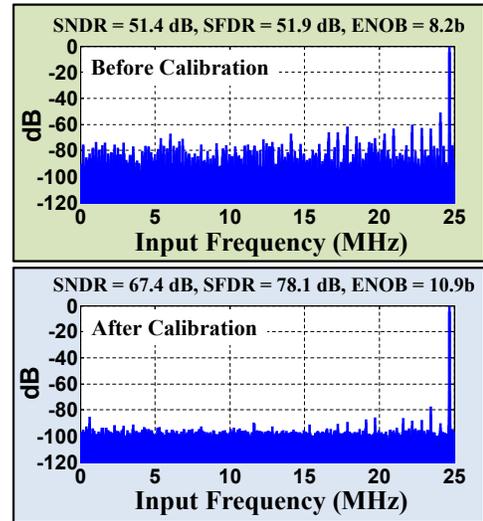


Fig. 9. Measured spectrum data with 1.2V supply at 50MS/s with a 24.7MHz input signal.

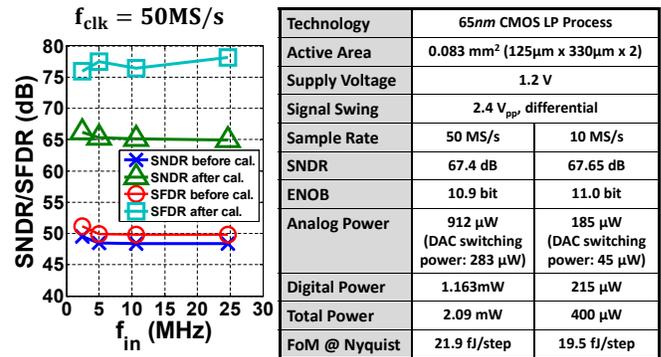


Fig. 10. Measured dynamic performance at different input frequencies and summary of the measurement results.

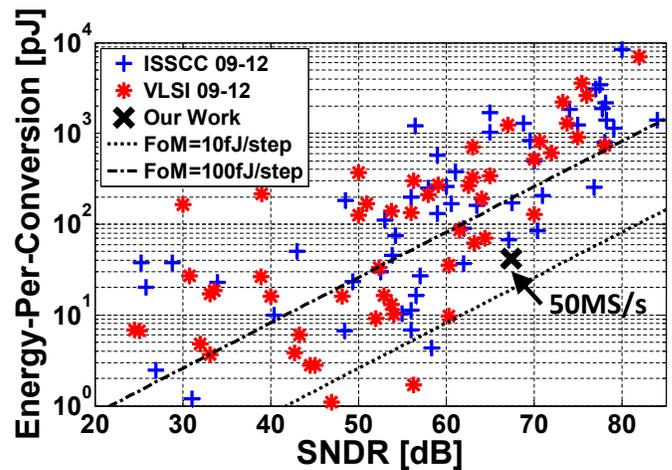


Fig. 11. Comparison with the state-of-the-art ADCs (data from B. Murmann, "ADC Performance Survey 1997-2012," <http://www.stanford.edu/~murmman/adcsurvey.html>).