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A Compact 0.135-mW/Channel LNA Array for Piezoelectric Ultrasound Transducers

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***Abstract*—This paper presents a power- and area-efficient 9-channel LNA array for piezoelectric ultrasound transducers to enable real-time 3D imaging with miniature endoscopic and catheter-based probes. In view of the relatively low impedance of piezoelectric transducers, the LNA is implemented as a capacitive feedback voltage amplifier, rather than a trans-impedance amplifier, to achieve a better noise-power trade-off. The use of a current-efficient inverter-based OTA with optimized bias scheme and dual-rail regulation further improves the power efficiency of the LNA while keeping the area compact: 0.01 mm^2 per channel. Electrical and acoustic measurement results show that the proposed LNA achieves a 0.6 mPa/√Hz input-referred noise at 4 MHz while consuming only 0.135 mW, which represents a noise efficiency 2.5 × better than the state-of-the-art.**

I. Introduction

The increasing clinical need for better visualization of human organs, such as the valves and chambers of the heart, calls for the development of miniature endoscopic and catheter-based ultrasound probes [1-3]. Such probes will be capable of providing the physician with valuable real-time 3D images for diagnostic purposes and for guiding interventional procedures, while being more patient-friendly and cost-effective than alternative imaging techniques. The acquisition of 3D images requires a 2D transducer array that consists of thousands of elements, and an associated front-end integrated circuit that connects the transducer array with the external imaging system. The strict constraints on the size and power dissipation of the probe tip present a challenge for the design of the front-end electronics. Hence, high power-efficiency and small silicon area become the main design targets for front-end circuits in such probes.

Fig. 1 shows the architecture of a front-end integrated circuit interfaced with a 2D piezoelectric transducer array [1]. Compared to capacitive micro-machined ultrasonic transducers (CMUTs), bulk piezoelectric transducers, typically based on PZT, offer a higher sensitivity without the need for a high DC bias voltage, while having a narrower bandwidth [4]. To simplify the implementation of the electronics, we adopt an architecture in which the 2D transducer is divided into a receive sub-array with associated integrated receive circuitry, and a smaller transmit sub-array directly wired to an imaging system [1]. The techniques presented in this paper, however, are equally applicable to architectures that include local transmit circuits. The receive circuitry for each transducer element consists of a low-noise amplifier (LNA), a

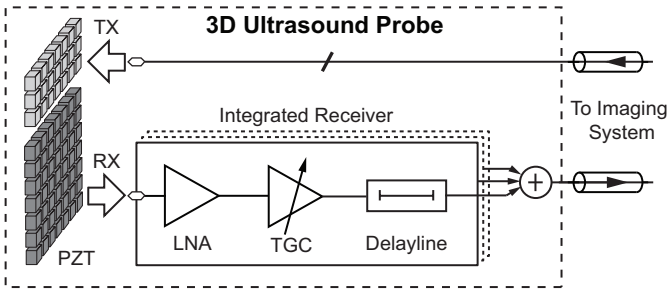

Fig. 1. Architecture of front-end integrated circuits for a 2D piezoelectric transducer array.

programmable-gain amplifier for time-gain compensation (TGC) and delay lines for local beamforming. Among these building blocks, optimizing the LNA is usually the key for minimizing power consumption because, in most cases, the majority of the power in the receive circuitry is consumed by the LNA to arrive at an input-referred noise level that is small compared to the transducer's noise.

In this work, an ultra-low power LNA array targeted for piezoelectric transducers is presented. It adopts a capacitive feedback topology to provide an accurate and programmable voltage gain for the received transducer signals, while optimizing the noise-power trade-off. Moreover, a single-ended cascoded inverter with local supply regulation is employed as the OTA to further improve the power efficiency. Implemented in a 0.18 μm CMOS technology, each LNA channel occupies less than 0.01 mm^2 of silicon area and consumes only 0.135 mW from a 1.8 V supply. Acoustic measurements have been performed by connecting the LNA array to a silicon-based PZT matrix implemented in-house. The acoustic results show that the design achieves a noise efficiency factor (NEF) of $0.22\ \mathrm{mPa}\cdot\sqrt{\mathrm{mW/Hz}}$, which is 2.5 × better than the state-of-the-art.

II. LNA Architecture

The choice of the LNA architecture is dictated by the electrical impedance of the target transducer. Most reported CMUT interface circuits utilize a trans-impedance amplifier (TIA) as the LNA [2-3, 7-8], with an input-impedance less than the transducer's impedance to sense the motional current. However, similarly-sized bulk PZT transducers, as applied in our work, have a much lower impedance around the center frequency [4], typically a couple of kΩs. This makes the TIA structure less effective, since creating a sufficiently low input-

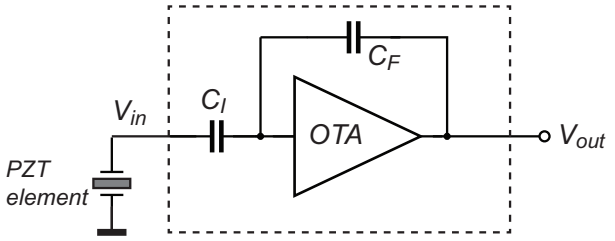

Fig. 2. The proposed LNA architecture.

impedance requires extra power spent on increasing the gain of the amplifier, rather than on reducing noise.

Instead, we propose to use a capacitive-feedback voltage amplifier, as shown in Fig. 2. It offers a mid-band voltage gain of $A_M = C_I / C_F$ and a bandwidth determined by the trans-conductance of the operational trans-conductance amplifier (OTA). Its input impedance is dictated by the input capacitor C_I and can be easily sized to tens of kΩs within the bandwidth of interest (1 MHz to 18 MHz), so as to sense the transducer's voltage, rather than its current.

III. Circuit Implementation

In order to minimize power consumption, the current-efficiency of the OTA has to be maximized, which makes the CMOS inverter an attractive candidate. A straightforward inverter-based implementation is shown in Fig. 3 [5]. In order to bias the NMOS and PMOS transistors in their optimal region, the input voltage is AC coupled to the gates, while a DC control loop sets the output voltage to the mid-supply.

When applied to the targeted ultrasound application, the circuit of Fig. 3 has the following limitations. The AC-coupling capacitors and the parasitic capacitor at the input gates form a capacitive divider, which attenuates the input signal and thus increases the input-referred noise of the LNA. Enlarging the AC-coupling capacitors is expensive in terms of the silicon area. Moreover, the circuit suffers from poor power-supply rejection, while in ultrasound probes, the supply lines can be noisy even in the signal band due to the co-integrated digital signal processing circuits. Finally, the feedback amplifier in the DC control loop is always connected to one of the inverter's input nodes, where it adds noise and introduces extra parasitic capacitance.

Here, these problems are solved by applying the following techniques.

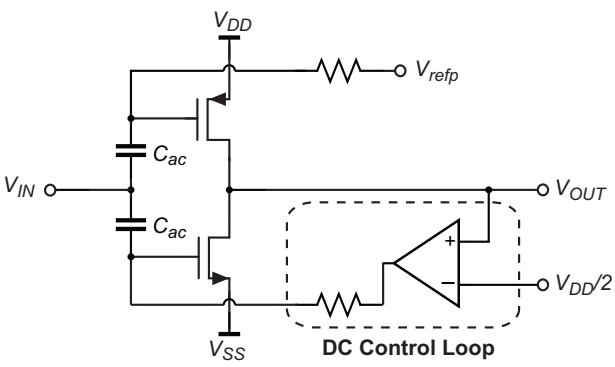

Fig. 3. Simplified schematic of the inverter-based OTA proposed in [5].

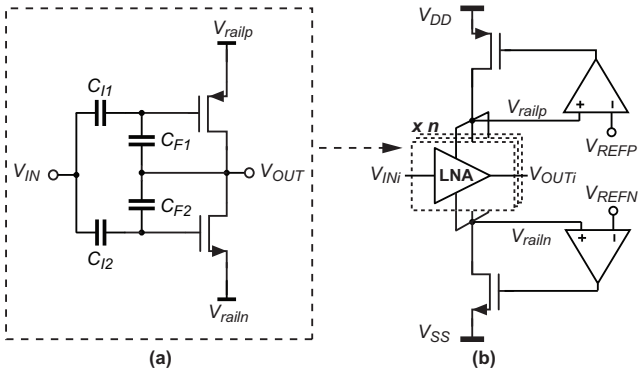

Fig. 4. (a) Capacitor splitting; (b) dual-rail local regulation (bias control circuits not shown).

A. Capacitor splitting

As shown in Fig. 4-a, the input bias for the NMOS and PMOS transistors can be separated by splitting the input and feedback capacitors into two equal pairs. As such, there is no need for adding extra AC-coupling capacitors. The mid-band gain becomes

$$A'_M = \frac{1}{2}\left(\frac{C_{I1}}{C_{F1}} + \frac{C_{I2}}{C_{F2}}\right) = \frac{C_I}{C_F} = A_M \qquad (1)$$

where $C_{I1} / C_{F1} = C_{I2} / C_{F2} = C_I / C_F$.

In order to maintain the same input impedance, the input capacitors in each half-branch should also be halved; so are the feedback capacitors. As result, the overall area of capacitors can be kept the same.

B. Dual-rail local regulation

An effective approach to improve the power-supply-rejection-ratio (PSRR) of an inverter-based amplifier is to regulate its supply lines. In this design, we propose to locally generate two internal power rails for an array of LNAs (Fig. 4-b), so as to reject noise from both the supply and the ground.

Given the fact that the loading currents for both regulators are known and approximately constant, the implementation of the regulators can be kept simple to save both power and area. A capacitor-less LDO based on a super source-follower [6] is adopted as the topology for both regulators. It provides sufficient loop gain and thus provides a reasonable PSRR even within the frequency range of the ultrasonic signals.

C. Dynamic bias control

To prevent the DC control loop from adding noise during the operation of the LNA, we propose to add switches that periodically activate the loop synchronously with the transmit/receive phases of the ultrasound system, as shown in Fig. 5. During the transmit phase, when the LNA is inactive, the feedback amplifier is connected to the inverter-based OTA to activate the bias control loop. Thus, the OTA is auto-zeroed, and the settled bias voltage is stored at the gates of the input transistors. After the transmit phase, the feedback amplifier is disconnected from the OTA and has both inputs connected to mid-supply, while the LNA starts receiving the echo signal, operating at the "memorized" bias condition stored on the parasitic capacitors of the input gates. To prevent the bias voltage from drifting, the bias control loop is periodically enabled in each transmit time slot.

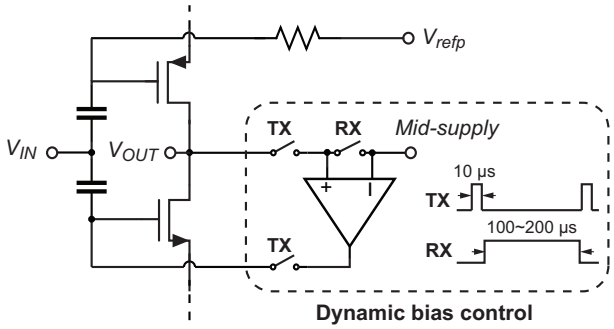

Fig. 5. Dynamic bias control scheme.

The effectiveness of this technique is guaranteed by the relatively short period of transmit/receive cycles in medical ultrasound imaging, which normally ranges from 100 µs to 200 µs, depending on the imaging depth. The relatively large sizes of the input transistors, needed to reduce flicker-noise, also helps to ensure the robustness of the bias voltages.

D. Complete LNA circuitry

Fig. 6 shows the complete schematic of the 9-channel LNA array. By applying the approaches discussed above, a power-efficient and area-compact implementation is obtained. In each LNA channel, an unity-gain-connected inverter, implemented with long-channel transistors and consuming only 0.4 µA, is connected between the two regulated supply rails to generate a reference voltage for the bias-control loop. The feedback amplifier is realized as a simple differential pair. It is designed to be able to settle within the transmit time slot (10 µs), resulting in a current consumption less than 1 µA. The inverter-based OTA is cascoded to ensure an accurate closed-loop gain, and input transistors M_1 and M_4 are biased in the weak-inversion region to enhance their current-efficiency. The bias voltage of M_1 is derived from a diode-generated voltage reference V_{refp} via a high-impedance pseudo-resistor. The same voltage is applied as the input of the positive-rail regulator. In such a way, the bias current of the OTA is defined by the difference of the reference currents ($I_{p1} - I_{p2}$) and the dimension ratio of M_1 and M_{p1}. While operating, 50 µA is consumed by each OTA, and 110 µA by each of the shared regulators, leading to a total power consumption of 670 µA @ 1.8V for 9 channels, corresponding to 0.135mW per channel.

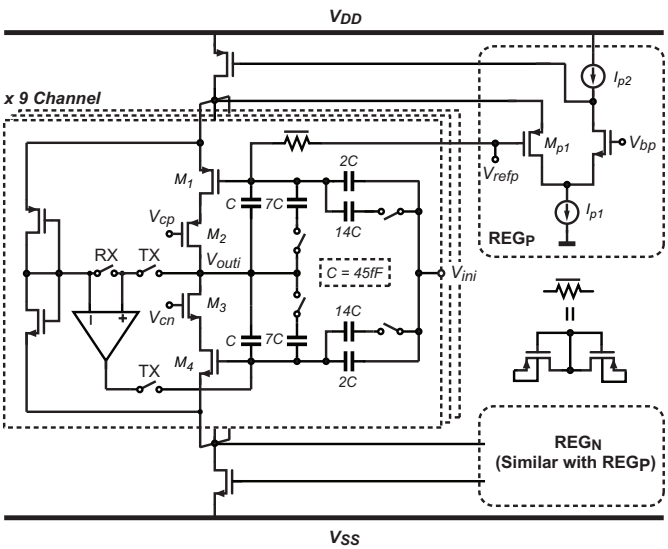

Fig. 6. Complete LNA circuitry.

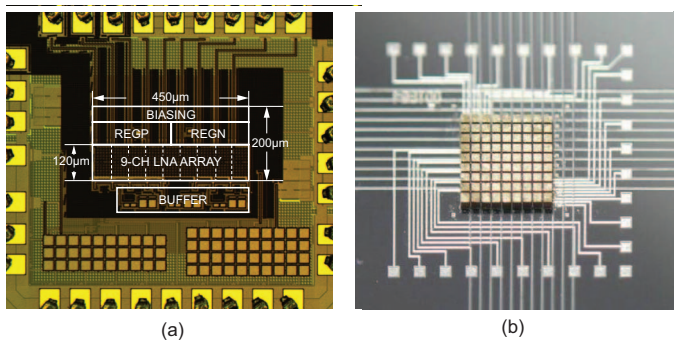

Fig. 7. Photograph of (a) the chip and (b) the silicon-based PZT matrix.

The cascoded inverter structure has a limited output swing. To enhance the dynamic range of the LNA, a programmable gain function is implemented by including switchable input and feedback capacitors. Three gain levels (24/6/-12 dB) are offered, of which the 24 dB gain is designed to achieve the best noise performance and the highest receive sensitivity.

IV. Experimental Results

The LNA array has been fabricated in a standard 0.18 µm CMOS technology. Fig. 7-a presents a micro-photograph of the prototype chip. The outputs of the LNA array are multiplexed to three buffers that drive the external cables. The core of the chip, including 9 LNAs, 2 regulators and bias circuits, occupies an area of 450 µm × 200 µm, which is equivalent to 0.01 mm^2 per channel.

To facilitate the acoustic characterization of the LNA array, a 10 × 10 array of PZT transducers with a 200-µm pitch, built on top of a silicon substrate with metal interconnects (Fig. 7-b), is connected to the inputs of the LNA array via PCB traces. The transducer provides a -6 dB bandwidth from 3.2 MHz to 4.8 MHz with a center frequency at 4 MHz.

Fig. 8-a shows the measured transfer function of the LNA at different gain settings. The measured mid-band gains at each gain setting are 22.50 dB, 4.65 dB and -13.15 dB respectively, which are approximately 1 dB lower than the designed gains due to attenuation of the output buffers. The measured –3 dB bandwidth is from 1.8 MHz to 11.6 MHz. Fig. 8-b shows the measured PSRR from 200 kHz to 20 MHz. The circuit

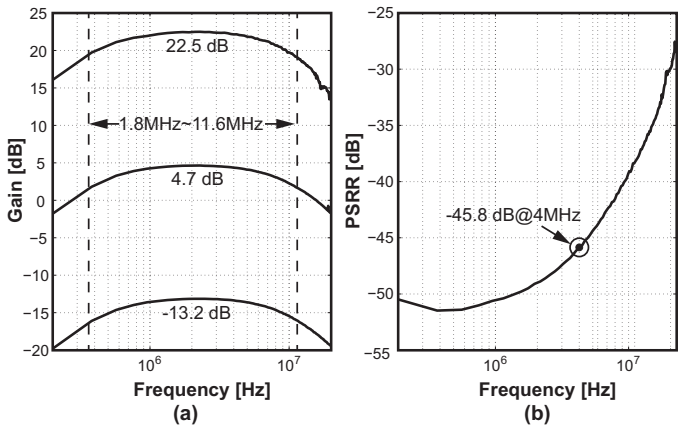

Fig. 8. Measured (a) transfer function and (b) PSRR.

TABLE I. PERFORMANCE SUMMARY AND COMPARISON

Specs	Target Transducer	Element Size (μm × μm)	LNA Bandwidth (MHz)	Power Consumption (mW)	Receive Sensitivity (mV/kPa)	Dynamic Range* (dB)	Input-referred Noise (mPa/√Hz)	NEF (mPa•√mW/Hz)
[2]	2D-CMUT	250 × 250	10	4.0	~70	N/A	1.8@5MHz	3.6
[3]	2D-CMUT	250 × 250	25	2.4	414	N/A	0.9@4.4MHz	1.4
[7]	1D-CMUT	300 × 3000	5.2	14.3	162	60	0.56@3MHz	2.1
[8]	2D-CMUT	250 × 250	10.2	1.4	123	N/A	2.3@5MHz	2.7
[9]	1D-CMUT	N/A	39.5	1.0	72	70	0.55**	0.55
This work	2D-PZT	200 × 200	9.8	0.135	130	81	0.6@4MHz	0.22

* Defined as the ratio of the maximum input signal at the 1-dB compression point and the minimum input signal at SNR = 0 dB.
** Averaged value across the bandwidth from 4.4 MHz to 15.4 MHz.

achieves a PSRR better than -45dB at 4 MHz. Fig. 9-a shows the measured input-referred voltage noise spectrum at the highest gain setting with a comparison to pre-layout simulation results. It is obtained by measuring the LNA output voltage noise and dividing it by the transfer function shown in Fig. 8-a, which indicates an input-referred voltage noise density of 5.9 nV/√Hz at 4 MHz. The integrated input noise voltage across the LNA bandwidth is 17.7 μVrms. The maximum input voltage is measured as 545 mVpp at the 1 dB compression point with the lowest LNA gain setting, where a -40 dB 2nd-harmonic distortion is guaranteed. Thus, the circuit achieves an 81 dB overall dynamic range. Moreover, the measured channel-to-channel crosstalk is below -46 dB at 4 MHz.

An acoustic measurement involving the LNA array and the silicon-based PZT matrix has been performed in a water-tank. A calibrated unfocused piezoelectric transducer, placed 8.5 cm away, is used as the source. Fig. 9-b shows the observed signal with a 1 Vpp 4 MHz 3-cycle burst sinusoidal wave applied to the transmitter. The incident pressure has been measured with a commercial hydrophone, giving an estimated receive sensitivity of 130 mV/kPa at the highest LNA gain setting.

A performance summary and comparison with state-of-the-art ultrasound front-end amplifiers is shown in Table I, including their noise-efficiency factor (NEF) as defined in [7]. With the lowest power consumption and a comparable input-referred noise, the proposed LNA achieves a NEF that is 2.5 × better than the state-of-the-art.

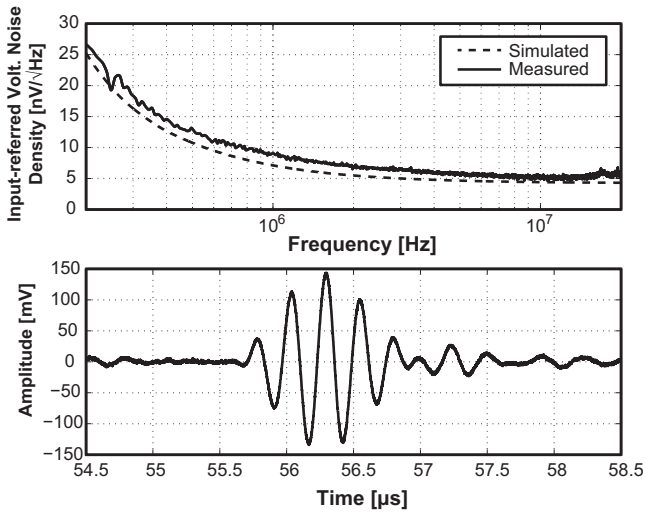

Fig. 9. (a) Measured and simulated input-referred voltage noise spectrum (top); (b) Received acoustic signal at the output of the LNA (bottom).

V. CONCLUSIONS

A power-efficient and compact LNA array for piezoelectric transducers has been presented. It is implemented as a capacitive-feedback voltage amplifier that senses the voltage from the transducer. A single-ended inverter-based OTA with dual-rail regulation and dynamic bias control is employed to achieve an ultra-low power consumption and a record NEF, which has been demonstrated by both electrical and acoustic measurements.

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