A readout circuit for tunnel magnetoresistive sensors employing an ultra-low-noise current source

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***Abstract*—We present a tunneling magnetoresistive (TMR) sensing microsystem consisting of a low flicker noise TMR sensor and a custom integrated readout frontend. The proposed sensor readout circuit introduces a novel ultra-low-noise current biasing scheme for the TMR sensor, which achieves a very low current noise floor of 2.2 pA/$\sqrt{\text{Hz}}$ for a 1 mA biasing current. The TMR output voltage is processed by a differential readout scheme to improve the baseline-to-signal ratio. The microsystem also features an on-chip 10-bit current DAC that allows compensating for the large process variations in the TMR base resistance value. The readout chip is manufactured in a 180 nm SOI CMOS technology and heterogeneously integrated with the TMR sensor. The readout chain provides a thermal noise floor of 4 nV/$\sqrt{\text{Hz}}$, while, together with the biasing scheme, consuming a total power of 38 mW. The complete sensor system consisting of the TMR and the readout circuit provides a state-of-the-art magnetic field noise floor of 120 pT/$\sqrt{\text{Hz}}$.**

I. Introduction

Nanoscale magnetoresistive (MR) sensors are attractive for many biosensing applications [1], [2] as well as human-machine interfaces [3]. Today, most of these systems use giant magnetoresistive (GMR) sensors due to their good overall performance. While tunnel magnetoresistive (TMR) sensors offer a superior sensitivity compared to GMR sensors, they typically display a much higher 1/f noise. Moreover, the high MR ratio of TMR sensors comes at the expense of large variations in its base resistance, leading to offsets that, if uncompensated, can reduce the dynamic range of the frontend. Fig. 1 shows different possible readout topologies for MR sensors. Here, the topologies of Fig. 1a and 1b are simple to realize but display inferior linearity since the change in resistance occurs in the denominator of the sensor output signal. This increased nonlinearity manifests itself as harmonic distortion in the output spectrum. In contrast, the current biasing scheme of Fig. 1c provides improved linearity at the expense of increased hardware complexity and a potentially increased noise floor due to the bias current source. More specifically, in the scheme of Fig. 1c, both the thermal and the flicker noise of the MOS current source typically dominate over the sensor and the frontend voltage amplifier, presenting the bottleneck for the achievable noise performance of the overall sensor system. To mitigate this problem, in [4], [5], the MOS transistor implementing the bias current source is embedded in a feedback loop to reduce its current noise.

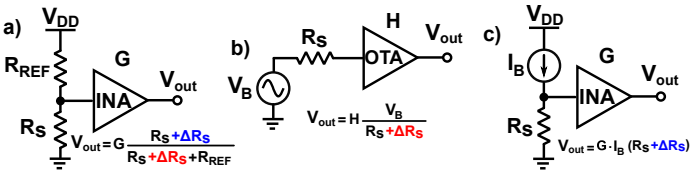

Fig. 1: Comparison of different MR readout topologies.

However, in the implementations of [4], [5], the noise of the opamp inside the feedback loop significantly contributes to the total output current noise, limiting the presented noise floor to about 10 pA/$\sqrt{\text{Hz}}$ for bias currents of around 500 µA [4]. To overcome this problem, in this paper, we propose an improved noise reduction loop for the current source based on a transimpedance amplifier (TIA). In the proposed scheme, any noise originating in the opamp of the TIA is greatly suppressed in the output current, allowing for significantly improved current noise floors compared to the prior arts.
The paper is organized as follows. In section II, the architecture of the proposed chip is introduced. Section III presents the measurement results of the readout chip and the TMR sensor system. The paper concludes with a summary in section IV.

II. Chip Description

Fig. 2a shows the architecture of the presented readout circuit, including the sensor current biasing block and the gain stages. The readout chip includes two current sources. One fixed current source to bias a reference sensor in a differential readout scheme for improved baseline-to-signal ratio [1] and a second adjustable current source to bias the TMR sensor. The DC-coupled scheme continuously monitors any offset between the TMR and the reference sensor. To compensate for the large process variations of the TMR sensor, the variable current source is realized as a 10-bit binary-weighted DAC that can provide bias currents up to 1 mA. The compensation is performed by an automatic calibration routine, which can be triggered via the chip's SPI interface.

A. Sensor biasing

The open-loop (OL) current noise power spectral density (PSD) of the current source transistor M_{CS} in Fig. 2b, is given by:

$$S_{\Delta I^2_{\mathrm{nD,OL}}} = 4kT\gamma g_{\mathrm{m}} + \frac{\mathrm{KF}\cdot g_{\mathrm{m}}^2}{C_{\mathrm{ox}}^{\mathrm{n}}\cdot W\cdot L\cdot f}, \qquad (1)$$

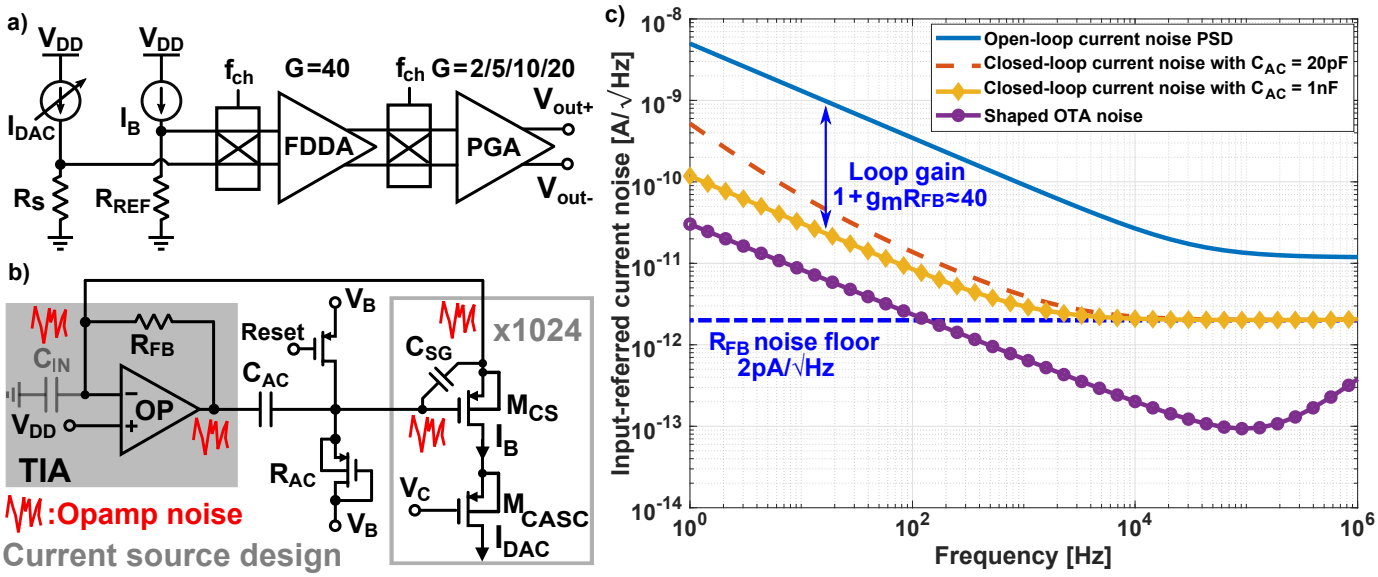

Fig. 2: a) System level block diagram of the readout chip. b) Block diagram of the sensor bias. c) Comparison of the simulated noise of the sensor bias with and without the feedback loop.

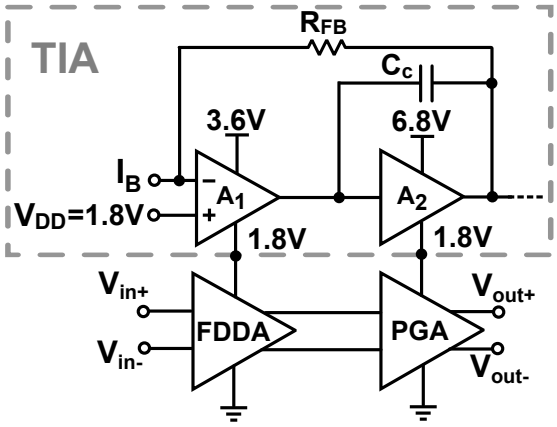

Fig. 3: Block diagram of the TIA embedded in the sensor bias loop and the current reuse technique for the amplifier chain.

where k is the Boltzmann constant, T is absolute temperature, γ is the excess noise factor, g_m is the transconductance of transistor $\mathrm{M_{CS}}$, W is the transistor width and L is the transistor length. According to eq. (1), the current noise PSD can be lowered by biasing the transistor $\mathrm{M_{CS}}$ deeply in strong inversion. However, this approach is eventually limited by the required headroom and/or the onset of velocity saturation effects. Moreover, reducing the flicker noise by increasing W and L leads to a large area consumption and large parasitics. As a possible route to further lowering the current noise, in this paper, we follow the idea of [4] and [5] of embedding the transistor $\mathrm{M_{CS}}$ into a feedback loop. However, in contrast to the prior art, the presented feedback loop, cf. Fig. 2b utilizes a TIA to reduce noise-induced fluctuations in the output current. Importantly, the TIA architecture greatly reduces the influence of the opamp noise on the overall current noise compared to previously presented noise reduction loops [4], [5]. The proposed feedback loop works as follows. Overall, the feedback loop regulates the source gate voltage v_sg of transistor $\mathrm{M_{CS}}$ with a high loop gain to reduce noise-induced fluctuations in the output current. The virtual short at the opamp input causes the source of transistor $\mathrm{M_{CS}}$ to be biased at VDD. The bias current flows through the TIA feedback resistor R_FB, producing a proportional voltage at the TIA output, which counteracts potential fluctuations in the output current. To allow for adjusting the DC bias current using the on-chip generated bias voltage $\mathrm{V_B}$, the TIA output is AC coupled to the gate of $\mathrm{M_{CS}}$, cf. Fig. 2b, effectively high pass filtering the TIA output with a very low cut-off frequency formed by capacitor $C_\mathrm{AC} = 20\,\mathrm{pF}$ and pseudo resistor $R_\mathrm{AC} = 10\,\mathrm{G\Omega}$. Additionally, a reset switch is added to the gate of the transistor $\mathrm{M_{CS}}$ to reset this high impedance node if necessary. The output current noise PSD of the proposed closed-loop scheme is then given by:

$$S_{\Delta I^2_{\mathrm{nD,CL}}} = \frac{S_{\Delta I^2_{\mathrm{nD,OL}}}}{(1+g_\mathrm{m}\,R_\mathrm{FB})^2} + \frac{4kT}{R_\mathrm{FB}} + V^2_{\mathrm{n,Opamp}} \cdot g^2_\mathrm{m} \cdot \underbrace{\left(\frac{R_\mathrm{FB}}{R_\mathrm{FB}+1/(\mathrm{s}\,C_\mathrm{IN})}\right)^2}_{\approx 0}, \quad (2)$$

where C_IN is the opamp input capacitance. Here, it is important to point out that any noise originating in the opamp of the TIA is greatly suppressed by the proposed feedback loop provided that $R_\mathrm{FB} \ll 1/(\mathrm{s}\,C_\mathrm{IN})$, cf. Fig. 2b and eq. (2). Intuitively, the TIA provides a voltage gain of unity from its input-referred voltage noise to the TIA output voltage, i.e. the gate voltage of transistor $\mathrm{M_{CS}}$. Moreover, the virtual short at the TIA input causes the source voltage of $\mathrm{M_{CS}}$ to also equal the TIA's input-referred voltage noise. Therefore, any TIA noise does not change the source-gate voltage of transistor $\mathrm{M_{CS}}$ and, therefore, does not increase the output

current noise. In this consideration, we have assumed that the AC coupling capacitor C_{AC} is much larger than the gate-source capacitance of $\mathrm{M_{CS}}$, C_{SG}, which has to be ensured by properly selecting the value of C_{AC}. Fig. 2c shows the simulated current noise PSD for an output current of 1 mA and using a TIA feedback resistor of $R_{\mathrm{FB}} = 4\,\mathrm{k\Omega}$. According to the figure, the open-loop current noise PSD of transistor $\mathrm{M_{CS}}$, $S_{\Delta I_{\mathrm{nD,OL}}}$, is reduced by the loop gain. The closed-loop noise floor is established by the current noise of the feedback resistor R_{FB}, cf. eq. (2), and given by $2\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ for the $4\,\mathrm{k\Omega}$ resistor used in the presented design. An important advantage of the proposed scheme is the possibility of working at moderately large inversion coefficients, while still being able to achieve very low noise floors. This allows significantly improving the voltage compliance level of the current source.

The implemented current source can provide currents up to 1 mA to maximize the TMR output signal. Since the utilized TMR sensor provides a base resistance of $\approx 1.4\,\mathrm{k\Omega}$, we use a larger feedback resistor in the TIA of the bias control loop of $R_{\mathrm{FB}} = 4\,\mathrm{k\Omega}$ to provide a noise floor below that of the TMR. To accommodate the maximum voltage drop of $\approx 4\,\mathrm{V}$ across R_{FB}, we have used a shifted power supply between $\mathrm{VSS_{bias}} = 1.8\,\mathrm{V}$ and $\mathrm{VDD_{bias}} = 3.6\,\mathrm{V}$ inside the biasing circuitry, as also shown in Fig. 3. This allowed us to implement the input stage of the TIA opamp using core 1.8 V devices, and only the opamp output stage has to use 5 V I/O devices supplied from a supply between $\mathrm{VSS_{bias}} = 1.8\,\mathrm{V}$ and $\mathrm{VDD_{biasH}} = 6.8\,\mathrm{V}$. Beside reducing the bias noise, the current flowing through the amplifier chain can be recycled from the bias circuitry of the sensor as shown in Fig. 3. Consequently, no additional biasing network is needed for the readout chain. It is worth mentioning that the proposed biasing scheme can also be supplied from a single supply when using smaller values of R_{FB} at the expense of increased noise floors.

B. Amplifier implementation

According to Fig. 2a, the low-noise bias current $\mathrm{I_{DAC}}$ flows through the TMR and produces a voltage signal that is subsequently amplified by a fully differential-difference amplifier (FDDA) with a gain of 40 followed by a programmable gain amplifier (PGA) with 4 different gain settings to accommodate different dynamic range requirements. The FDDA is implemented as a 2-stage Miller-compensated OTA. The input differential pair uses a current reuse scheme with stacked PMOS and NMOS differential pair to maximize the $g_{\mathrm{m}}/I_{\mathrm{D}}$ ratio and, thereby, the noise efficiency of the input stage [6]. Moreover, the FDDA includes chopping switches to suppress its offset and 1/f-noise.

III. Measurement Results

Fig. 4 shows a micrograph of the manufactured chip. The design occupies an active area of $1.7\,\mathrm{mm^2}$. The measured input-referred noise of the amplifier chain in the readout path with and without chopping ($f_{\mathrm{ch}} = 60\,\mathrm{kHz}$) and with nominally identical ohmic resistor connected to the input is shown in Fig. 5. In both cases, the measured noise floor is $4\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. With enabled chopping, the 1/f-noise corner frequency improves from 10 kHz to 400 Hz. The residual flicker noise after chopping originates from the unchopped PGA, cf. Fig. 2a.

To demonstrate the effectiveness of the proposed biasing scheme, Fig. 6 compares the measured closed-loop output noise of transistor $\mathrm{M_{CS}}$ against the situation when the reset switch in Fig. 2b is closed (OL noise from $\mathrm{M_{CS}}$ and the opamp are present) for a bias current of 1 mA. The measured noise floor with activated control loop is $2.2\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$, which presents a 5x improvement compared to the state-of-the-art [4], [5]. We measured the linearity of the readout chain by a single-tone test at a frequency of 10 kHz and an amplitude of $2.5\,\mathrm{mV_{pp}}$ while setting the PGA gain to 10, corresponding to an output amplitude of $1.0\,\mathrm{V_{pp}}$. The corresponding voltage spectrum at the chip output is shown in Fig. 7. The measured spurious-free dynamic range (SFDR) is 69 dB. The linearity is mainly limited by the open-loop structure of the input differential pair of the FDDA.

We then characterized the overall system performance as a TMR sensor system by replacing one of the two ohmic resistors by the TMR sensor presented in [7], which has a nominal resistance of $1.4\,\mathrm{k\Omega}$. As a first test, we ran the autocalibration routine to compensate the offset at the input of the readout chain. Then, we measured a sensitivity of 110 V/A/mT for

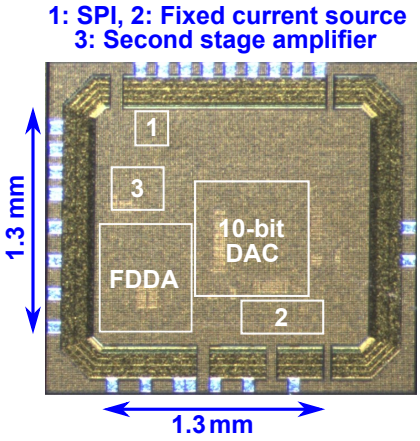

Fig. 4: Annotated chip micrograph.

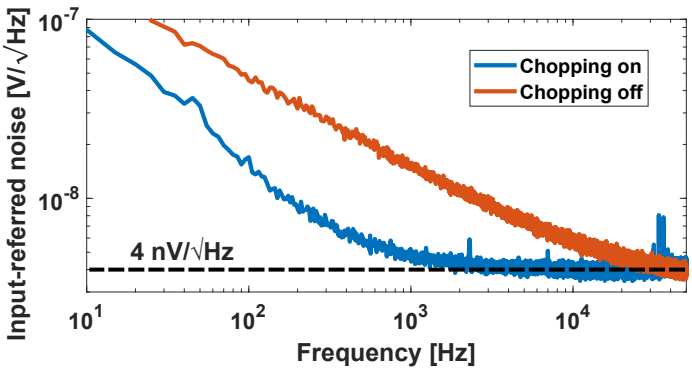

Fig. 5: Measured input referred voltage noise PSD of the amplifier chain with and without chopping.

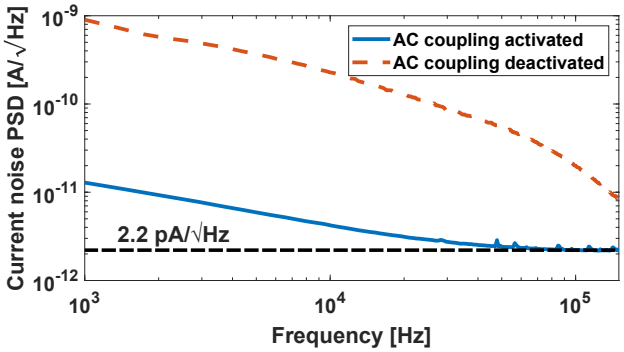

Fig. 6: Measured current noise PSD of the sensor bias.

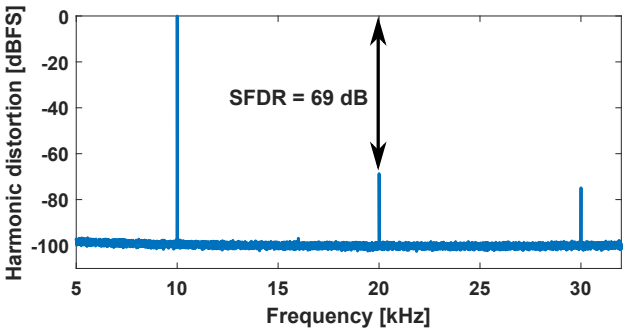

Fig. 7: Measured chip output distortion for an input signal with an amplitude of 2.5 $\mathrm{mV_{pp}}$ and a frequency of 10 kHz.

the TMR sensor for a bias current of 700 µA. For the same bias current, we measured the input-referred magnetic field noise PSD shown in Fig. 8a. The measured magnetic noise floor is 120 $\mathrm{pT}/\sqrt{\mathrm{Hz}}$ with a 1/f-noise corner frequency of $f_{\mathrm{fl}} = 1.5\,\mathrm{kHz}$. Fig. 8b shows the spectrum at the output of the sensor system when applying a magnetic field at a frequency of 5 kHz with an amplitude of 1.5 $\mathrm{nT_{rms}}$. The measured SNR is 22 dB, from which a limit of detection (LOD) of 120 $\mathrm{pT}/\sqrt{\mathrm{Hz}}$ has been calculated, which is compatible with the measured magnetic field noise in the absence of a signal, verifying the absence of nonlinear noise folding effects. Table I compares this work to the state-of-the-art in MR frontends employing current biasing.

IV. Conclusion

In this paper, we have presented a readout chip for a TMR sensing system, including an on-chip current bias. The system provides a state-of-the-art magnetic field LOD of 120 $\mathrm{pT}/\sqrt{\mathrm{Hz}}$. This is achieved by incorporating an ultra-low-noise current bias scheme for the MR sensor displaying a 5x improvement in the noise floor compared to previous designs. Moreover, the presented chip can provide a large range of bias currents up to 1 mA to accommodate the high process variations of TMR sensors. The included programmable readout chain including chopping displays a low noise floor of 4 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ together with a low 1/f-noise corner of 400 Hz, rendering the overall MR frontend a very versatile and high-performance platform for next-generation TMR sensing systems.

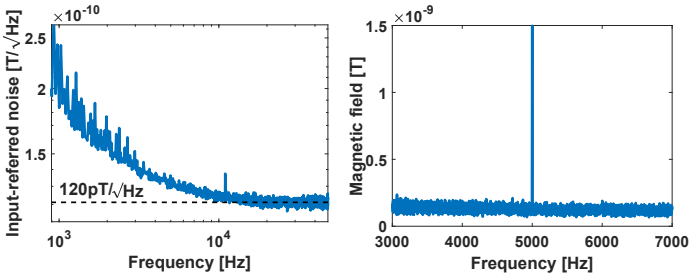

Fig. 8: a) Input-referred magnetic noise PSD of the TMR system. b) Measured spectrum with an input magnetic field of 1.5 $\mathrm{nT_{rms}}$.

TABLE I: Comparison against the state-of-the-art.

	Zhou [1]	Costa [4]	Zhou [5]	**This work**
Sensor	GMR	GMR	GMR	**TMR**
Resistance [Ω]	150	850	1300	**1400**
Sensor bias	–	0.5 mA	–	**up to 1 mA**
Bias noise [$\mathrm{pA}/\sqrt{\mathrm{Hz}}$]	–	10	≈10$^{\gamma}$	**2.2**
Input-referred noise [$\mathrm{nT}/\sqrt{\mathrm{Hz}}$]	46.4	11.5	8.2$^{\gamma}$	**0.12**
Power [mW]	0.43*	4.9*	2.5*	**10.4*§/38**
Area [mm^2]	0.249	3.17	1.92	**1.7**
Process [µm]	0.18	0.35	0.18	**0.18**

*Power excludes the current bias. $^{\gamma}$Calculated from figures and text.
§Power measured while switching off the sensor bias.
A FoM such as noise efficiency factor (NEF) can not be provided since the signal bandwidth has not been included in the reference designs.

Acknowledgment

This work has been supported by the German Research Foundation (DFG) under contract no. AN 984/12-1.

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