Draft version, pre-submission version.
Currently accepted for presentation at the IEEE 48th European Solid-State Circuits Conference, 19-22 September 2022, Milan (Italy). DOI not yet available.

A 150 mV, Sub-1 nW, 0.75%-Full-Scale INL Delta-Sigma ADC for Power-Autonomous Sensor Nodes

A. Catania[1*], A. Ria[2], G. Manfredini[1], M.Dei[1], M. Piotto[1], and P. Bruschi[1]
[1]*Department of Information Engineering, University of Pisa, Italy*
[2] *IEIIT Istitute of Italian National Research Council (CNR), Pisa, Italy*
*alessandro.catania@unipi.it

***Abstract*— Measured performances of a Delta Sigma ADC prototype operating down to 150 mV supply show 600 pW consumption while being able to convert dc signals with INL<0.75% of input full scale. The modulator shows an SNDR of 59.3 dB over a bandwidth of 0.3 Hz and 17 Hz at a supply voltage of 0.15 V and 0.3 V, respectively. Dc characterizations over a set of 5 samples between 0.18 V and 0.3 V supply range show consistent and repeatable offset (<0.51% of full scale) and integral non-linearity (<1.45% of full scale). Such performances candidate the proposed ADC for its use in ultra-low voltage, low sampling rate, power-autonomous sensor nodes.**

Keywords— ***Ultra-low voltage, Ultra-low power, Delta-Sigma ADC, Inverter-Like, Energy-harvester powered***

I. Introduction

An increasing number of emerging applications is requiring the development of extremely miniaturized sensor nodes, capable of monitoring critical physical and chemical quantities relying only on the power provided by energy harvesters. Among the latter, great interest is received by enzymatic biofuel-cells [1,2], especially for wearable and implantable devices. These sources pose great challenges to the designers, due to their low output voltages, often of the order of only a few hundred mV. Use of boost dc-dc converters is made difficult by their low efficiency when applied to Ultra-Low Voltage (ULV) and Ultra-Low Power (ULP) harvesters. Then, it is desired to develop complete sensor systems capable of operating with an as small as possible supply voltage. Prototypes of CMOS digital standard-cells capable of operating with sub-100 mV supply voltage have been demonstrated [3], while analog circuits are lagging behind, with only a few examples capable of overcoming the 200 mV barrier. To fill this gap, the development of ULV CMOS analog cells is therefore of paramount importance.

A key block that is required in most sensor systems is the Analog to Digital Converter (ADC). Interestingly, data logging of biometric parameters (e.g. temperature, humidity, concentration of analytes in body fluids) involves very slow conversion rates, often below one sample per second. In these cases, the usual trade-offs between bandwidth, resolution and power consumptions are less relevant and the actual challenge is obtaining an adequate dc accuracy even with extremely low supply voltages and power consumptions [4]. Several examples of ULV ADCs have been presented in the last decade. The functionality of SAR ADCs for supply voltages equal [5] or even lower [6] than 200 mV have been demonstrated. For the quoted relaxed sampling rate constraints, single-bit Discrete Time (DT) Delta Sigma (ΔΣ) ADCs represent a viable alternative to SAR ADCs, offering advantages in terms of area occupation due to their intrinsic insensitivity to device mismatch. Examples of DT-ΔΣ ADCs compatible with supply voltages from 300 mV to 250 mV have been proposed [7-10]. Lower supply-voltage limits have been reported for ΔΣ ADCs where the integrator function is accomplished in the phase-domain by a Voltage Controlled Oscillator (VCO) [11, 12]. A major drawback of open-loop VCO-based ADCs is low control over gain and offset errors, which strongly depend on the accuracy of the VCO voltage-to-frequency conversion law. Considering classical DT-ΔΣ architectures, reduction of the supply voltage (V_{dd}) impacts on the amplifier's gain-bandwidth product and output range. Inverter-like amplifiers become the mandatory solution when V_{dd} gets lower than the MOSFET's threshold voltage [10]. Notice that for supply-voltages lower than nearly 200 mV, the interval of output voltages where both devices of the inverters operate in saturation region vanishes, leading to available voltage gains in the order of a few units. In addition, stabilization of the output common mode voltage of Fully-Differential (FD) amplifiers formed only by standard CMOS inverters is problematic. The popular Nauta's six-inverter solution [13] was found to be highly inefficient in terms of output range [14].

In this work we propose a second-order FD DT ΔΣ ADC, based on switched capacitor (SC) integrators that exploits recently introduced solutions for mitigation of the aforementioned problems occurring at extremely low dc voltages. A 9-inverter topology [15], which, differently from the Nauta's solution, does not degrade the original inverter output swing, is used for the fully differential amplifiers. Acceptable dc performances are maintained even at supply voltages below 200 mV thanks to the adoption of a two-stage SC integrator [16] that boosts the dc gain of the amplifiers, while reducing the offset of the latter through Correlated Double Sampling (CDS). The proposed ADC architecture was originally proposed in [17], where the potentiality of application in ULV conditions was supported by simulations. This work describes for the first time the results of measurements performed on a prototype designed using the UMC 0.18 µm CMOS process.

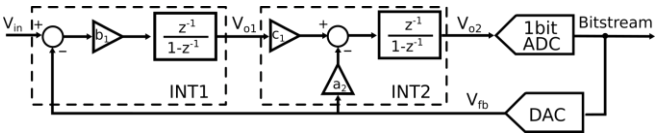

Fig. 1. Block diagram of a 2nd order, single-bit quantizer, Discrete-Time ΔΣ modulator.

II. Circuit Description

The topology chosen for the proposed ULV ΔΣ modulator is a DT 2nd order Cascade of Integrator FeedBack (CIFB) with a single-bit quantizer (Fig.1). This standard topology was adopted for its good compromise between resolution, linearity and design complexity. Moreover, a fully-differential architecture was preferred due to its intrinsic robustness to common-mode disturbs and its doubled signal range. The schematic view of the whole ΔΣ modulator is represented in Fig.2, including the time diagram of the clock phases.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under the Marie Skłodowska-Curie grant agreement No. 893544.

The first integrator INT1 represents the most critical block in terms of noise, offset and dc gain requirements, as it was extensively analysed in [17]. For this reason, the switched-capacitor integrator presented in [16] was employed. The coefficient b_1 (Fig.1) is realized by the capacitive ratio C_S/C_F, while the other capacitors C_T and C_H are needed to reach the low dc-gain sensitivity and the dynamic offset cancellation technique, which are peculiar of this integrator topology. These characteristics are essential when we are working with ultra-low supply voltages and inverter-like amplifiers, characterized by intrinsic low dc gain and large sensitivity to device mismatch. The fully-differential amplifiers A_1 and A_2 are implemented exploiting the completely inverter-like topology presented in [15] and depicted in Fig.3-a. Differently from other fully-differential inverter-like amplifiers as [13], it maximizes the differential output range, reaching at the same time a good common-mode stabilization. Thanks to the Common-Mode Stabilization Loop made by $Inv_{3\text{-}9}$, the amplifier shows a common-mode gain lower than one, which allows stabilization of the common-mode signals of the integrator. Inverters $Inv_{1\text{-}9}$, employed in the fully-differential amplifier, are depicted in Fig.3-b. The body terminal of the pMOS is connected to a potential close to ground in order to lower its threshold voltage and improve the inverter speed. The body terminal is connected to the nMOS M_d (shared by all the inverters in the modulator) to limit the current flowing through the forward-biased body-source and body-drain junctions of the pMOS. However, at ultra-low supply voltages (e.g. lower than 0.5 V), the current flowing through the two junctions is negligible and the pMOS body terminal is biased with a potential very close to ground.

The performance of the second integrator INT2 is not as critical as the first one, as discussed in [17]. For this reason, we did not choose the same topology of INT1 but we opted for a standard parasitic-insensitive switched-capacitor topology, which employs only one fully-differential amplifier. Capacitive ratios C_{S2A}/C_{F2} and C_{S2B}/C_{F2} implement modulator coefficients c_1 and a_2, respectively. The fully-differential amplifier A_3 is identical to A_1 and A_2. The constant bias voltage V_{inv} used in INT1 and INT2 is generated by a single input-output connected inverter (Inv_0 in Fig.2).

The 1-bit ADC is a latched comparator, whose schematic view is shown in Fig.4. It works on the two clock phases, pre-amplifying the input signal during phase 2 ($Inv_{10\text{-}11}$) and deciding during the following phase 1 ($Inv_{12\text{-}13}$). Each clocked inverter is formed by a CMOS inverter and two switches to disable it during the off-phase. The 1-bit DAC provides the differential feedback signal to INT1 and INT2. The reference voltage corresponds to the supply voltage V_{dd}, thus the DAC simply consists of two cascaded inverters used to buffer the output differential signal of the comparator and its schematic view is omitted for simplicity.

Proper non-overlapped control signals, whose timing is depicted in Fig.2, drive all modulator switches. Excluding the switches in the 1-bit ADC, which are implemented as pass-transistors, the rest of the switches are complementary pass-gates. The high and low voltage levels of the control signals are shifted to $2V_{dd}$ and $-V_{dd}$, respectively, by means of a clock-boosting circuit [9], reducing the on-resistance of both the pMOS and the nMOS switches, which is particularly critical in ULV design.

III. Experimental Results

The proposed ΔΣ modulator was fabricated with the 0.18 µm UMC CMOS process, using the 1.8 V MOSFET core devices. Sizing of all the inverters employed in the fully-differential amplifiers A_1, A_2 and A_3 (which are nominally identical), as well as sizing of the inverters in the ADC and in the DAC and of all the pass-gates, is reported in Table I. Values of the capacitors employed in INT1 and INT2 are also shown in Table I. Fig.5 shows a composition of an optical micrograph of the ΔΣ modulator and its superimposed layout in order to display devices and interconnections otherwise hidden below the planarization dummies. The geometrical dimensions of the clock boosting circuit and the ΔΣ modulator are indicated in the picture; the overall area occupation is 0.088 mm^2.

The oversampling clock signal was generated by a digital finite state machine, starting from the on-chip oscillator frequency and successively divided by means of programmable counters, which allow fine tuning of the oversampling frequency. The clock signal was level-shifted from the digital supply level (1.8 V) to the supply voltage V_{dd} of the ΔΣ modulator. At the output of the modulator, the bitstream was level-shifted from V_{dd} to 1.8 V. Both the clock and the bitstream waveforms were acquired by means of a Rohde & Schwarz RTB2004 oscilloscope and transferred to a personal computer, where the produced bit sequence was recovered and processed by programs written with the Python language. The software was used to estimate the bitstream spectra and implement a 3rd order CIC filter with a decimation factor (=OSR) of 64. The dc input differential signals were provided by a two-channel Source Measure Unit (SMU) Keysight B20902B. Sinusoidal and step stimuli were provided with an Agilent 33220A Arbitrary Waveform Generator.

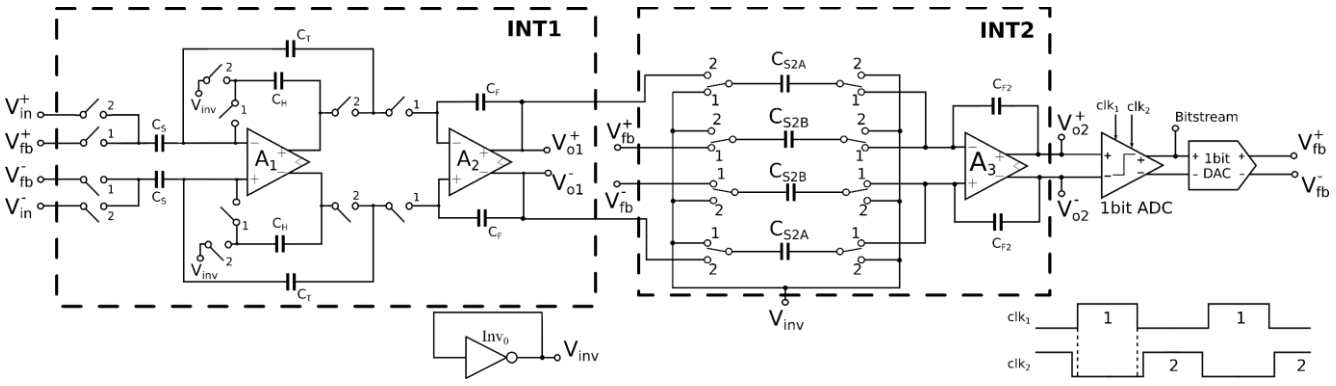

Fig. 2. Schematic view of the 2nd order, single-bit quantizer, fully-differential ΔΣ modulator.

Draft version, pre-submission version.
Currently accepted for presentation at the IEEE 48th European Solid-State Circuits Conference, 19-22 September 2022, Milan (Italy). DOI not yet available. Copyright IEEE.

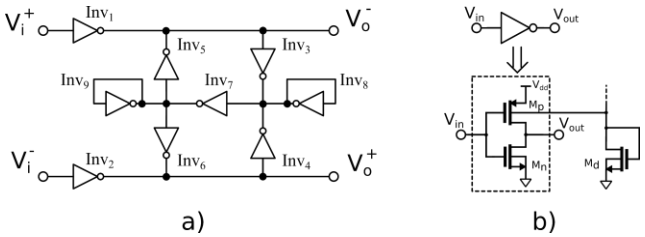

Fig. 3. Schematic view of the fully-differential inverter-based amplifier (a) and of the CMOS inverter with body-bias of Mp (b).

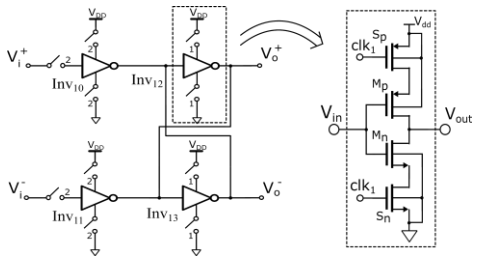

Fig. 4. Schematic view of the inverter-like 1-bit ADC, with the detail of the clocked inverter.

TABLE I
SIZES OF MOSFETS AND CAPACITORS

	L_{nMOS}	W_{nMOS}	L_{pMOS}	W_{pMOS}
Inv0	1 µm	5 µm	1 µm	5 µm
Inv1,2	1 µm	10 µm	1 µm	10 µm
Inv3,4	1 µm	2 µm	1 µm	2 µm
Inv5,6	1 µm	5 µm	1 µm	5 µm
Inv7,8,9	1 µm	500 nm	1 µm	500 nm
Inv10,11,12,13 (ADC 1-bit)	180 nm	2 µm	180 nm	6 µm
DAC inverters	180 nm	12.5 µm	180 nm	12.5 µm
Pass Gates	180 nm	960 nm	180 nm	1.92 um
C_S	**C_T,C_H,C_{F2}**	**C_F**	**C_{S2A}**	**C_{S2B}**
500 fF	1 pF	4 pF	490 fF	125 fF

Dc characterization was performed at different supply voltages, from 0.15 V to 0.3 V. The reference voltage of the ADC is V_{dd}, so the maximum input differential range is [-V_{dd}, V_{dd}]. All the results are normalized to the full-scale range of the ADC (FS=V_{dd}) to facilitate comparison of measurements performed at different supply voltages. Fig.6 shows the Integral Non-Linearity (INL) as a function of the differential dc input voltage for a fixed common mode dc input equal to V_{dd}/2, at different supply voltages (0.15 V, 0.18 V, 0.2 V and 0.3 V). The INL is lower than 1.5% of FS for a wide range of differential input voltages (from -90% to 90% of FS), for all the tested supply voltages. The current consumption I_{sup} and the oversampling frequency f_{ovs} at each supply voltage are listed in the inset of Fig.6. The dc operating point of the inverter-like amplifiers is sensitive to the supply voltage and their bias currents depend exponentially on the V_{dd} variations due to the weak inversion bias region. Thus, also the bandwidth of the amplifiers and, consequently, the maximum oversampling frequency of the ADC increase at higher supply voltages. It is worth noting the very low current consumption at V_{dd}=0.15 V resulting in a power consumption of only 600 pW.

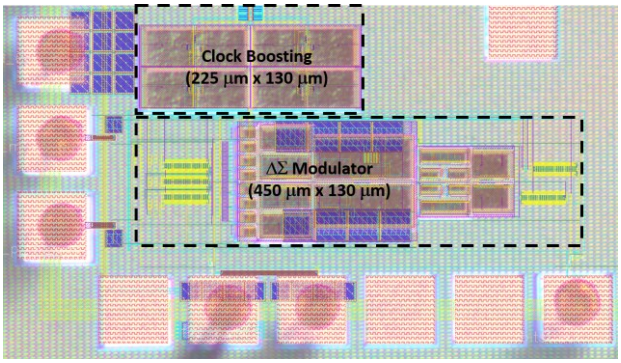

Fig. 5. Optical micrograph (plus superimposed layout) of the ΔΣ modulator and the clock boosting circuit.

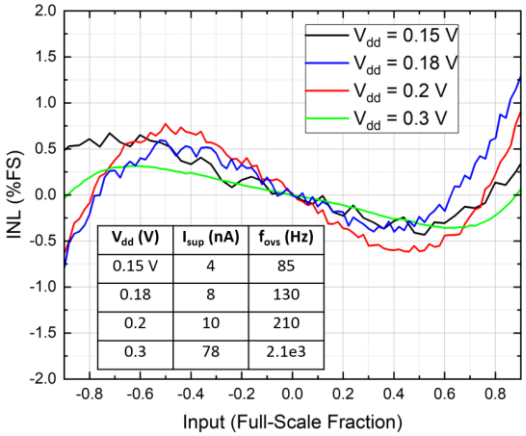

Fig. 6. INL vs differential input voltage at different supply voltages. The table in the inset shows the current consumption and the oversampling frequency for each V_{dd}.

Fig. 7 shows the step response of the ΔΣ modulator at the output of the software CIC filter, with a supply voltage of 0.15 V, an input common mode of V_{dd}/2 and an oversampling frequency of 85 Hz. Comparing the input differential square waveform and the output data, a significant offset can be recognized. This is mainly due to the low dc gain of the inverter-like amplifiers at this extremely low supply voltage, which causes a degradation of the effectiveness of the CDS technique [16]. It is worth noting also the settling time of the output waveform, which coincides with the typical three decimated data settling time of the employed 3rd order CIC filter. Finally, the inset shows repeated acquisitions after the settling time, from which an rms equivalent noise of 354 ppm of FS was estimated.

Fig.8 shows the spectrum of the modulator bitstream for two different supply voltages, 0.15 V and 0.3 V. Different oversampling and stimulus frequencies were set in the two testing conditions, as well as different oversampling ratios (128 at V_{dd}=0.15 V, 64 at V_{dd}=0.3 V) and different amplitudes. The ratio between the input tone amplitude and the converter full-scale was kept constant. In both operating conditions, the modulator shows a Signal to Noise And Distortion ratio (SINAD) of 59.3 dB, while the Total Harmonic Distortion (THD) is close to -60 dB or lower, which represent a promising result of these preliminary analysis.

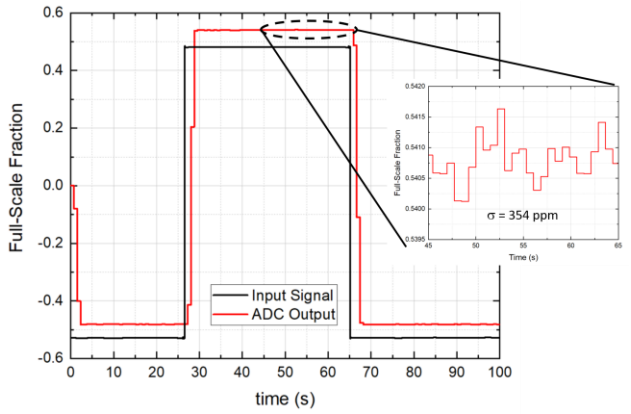

Fig. 7. Step response of the ΔΣ modulator supplied at V_{dd}=0.15 V (FS=0.15 V). The output bitstream was processed by means of Python 3rd order CIC filter with a decimation factor of 64.

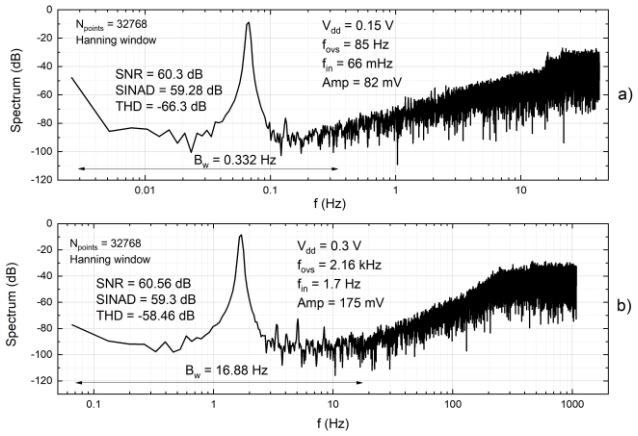

Fig. 8. Spectra of the output bitstream at V_{dd} = 0.15 V a) and V_{dd} = 0.3 V b).

Dc characterizations over a set of 5 samples at three different supply voltages (0.18 V, 0.2 V and 0.3 V) were performed and the average value μ and the standard deviation σ are reported in Table II. The standard deviation of the modulator offset is similar at 0.18 V and 0.2 V, while it significantly decreases at the highest supply voltage, due to the intrinsic increase of the amplifier dc gain. A similar trend can be recognized also in the maximum INL (measured over a differential input range from -90% to +90% of FS).

TABLE II
DC MEASUREMENTS ON 5 SAMPLES AT DIFFERENT VDD VALUES

V_{dd} (V)	I_{sup} (nA)		Offset (%FS)		INL-MAX (%FS)	
	μ	σ	μ	σ	μ	σ
0.18	9.9	1.2	-0.51	0.7	1.4	0.4
0.2	14.2	2.36	-0.06	0.83	1.45	0.55
0.3	108.6	17	-0.16	0.19	0.43	0.13

CONCLUSIONS

The proposed ΔΣ modulator is capable of working with supply voltage as low as 150 mV and a power consumption of only 600 pW. These performances are made possible by means of the high-gain, offset-free, switched-capacitor integrator and the high output swing, fully-differential, inverter-like amplifier. It shows a maximum INL of 0.75% of full-scale at V_{dd}=0.15 V and a SINAD = 59.3 dB over a bandwidth of 0.3 Hz. Despite of the very low conversion rate, the proposed ADC is perfectly suitable for data logging in power-autonomous sensor nodes (as wearable and implantable devices), where the signal bandwidth of several biometric parameters is typically below 1 Hz.

REFERENCES

[1] A.F. Yeknami, X. Wang, I. Jeerapan, S. Imani, A. Nikoofard, J. Wang, P. Mercier, "A 0.3-V CMOS Biofuel-Cell-Powered Wireless Glucose/Lactate Biosensing System", IEEE J. Solid State Circuits, vol. 53, pp. 3126-3139, November 2018.

[2] C. Gozales-Solino, M. Di Lorenzo, "Enzymatic Fuel Cells: Towards Self-Powered Implantable and Wearable Diagnostics", Biosensors, vol. 8, pp. 1-18, January 2018.

[3] N. Lotze and Y. Manoli, , "Ultra-Sub-Threshold Operation of Always-On Digital Circuits for IoT Applications by Use of Schmitt Trigger Gates", IEEE Trans. Circ. Sys. I, vol. 64, pp. 2920-2933, Nov.ember2017.

[4] M. Dei, J. Aymerich, M. Piotto, P. Bruschi, F. del Campo, and F. Serra-Graells, "CMOS Interfaces for Internet-of-Wearables Electrochemical Sensors: Trends and Challenges," MDPI Electronics, vol. 8, no. 2, p. 150, Jan. 2019.

[5] A. Petrie, W.Kinnison, Y. Song, K. Layton, S.W. Chiang, "A 0.2-V 10-bit 5-kHz SAR ADC with Dynamic Bulk Biasing and Ultra-Low-Supply-Voltage Comparator", proc. of IEEE CICC conference, Boston, MA, 22-25 March 2020.

[6] X. Zhou, Q. Li, "A 160mV 670nW 8-bit SAR ADC in 0.13μm CMOS", proc. of IEEE CICC, San Jose, CA, USA 9-12 September 2012.

[7] L. Lv, X. Zhou, Z. Quiao, Q. Li, "Inverter-Based Subthreshold Amplifier Techniques and Their Application in 0.3-V ΔΣ-Modulators", IEEE J. Solid State Circuits, vol. 54, pp. 1436-1445, May 2019.

[8] F. Michel and M. S. J. Steyaert, "A 250 mV 7.5 μW 61dB SNDR SC ΔΣ modulator using near threshold votage biased inverter amplfiers in 130 nm CMOS", IEEE J. Solid-State Circuits, vol. 47, no. 3,pp. 709–721, Mar. 2012

[9] A. Catania, L. Benvenuti, A. Ria, G. Manfredini, M.Piotto, P. Bruschi, "A 2 nW 0.25 V 140 dB-FOM Inverter-Based First Order ΔΣ Modulator, IEEE Trans. Circ. Sys. II, vol. 7, pp. 1514-1518, Sept. 2020.

[10] L. Lv, X. Zhou, Z. Qiao and Q. Li, "Inverter-Based Subthreshold Amplifier Techniques and Their Application in 0.3-V ΔΣ-Modulators," IEEE J. Solid State Circuits, vol. 54, no. 5, pp. 1436-1445, May 2019.

[11] U. Wismar, D. Wisland and P. Andreani, "A 0.2V, 7.5 μW, 20 kHz ΣΔ modulator with 69 dB SNR in 90 nm CMOS", in proc. of ESSCIRC 2007, Munich, Germany, 11-13 September 2007.

[12] V. Nguyen, F. Schembari and R. B. Staszewski, "A Deep-Subthreshold Variation-Aware 0.2-V Open-Loop VCO-Based ADC," IEEE J. Solid State Circuits, *Early Access*, Oct. 2021

[13] B. Nauta, "A CMOS transconductance-C filter technique for very high frequencies," IEEE J. Solid State Circuits, vol. 27, no. 2, pp. 142-153, Feb. 1992.

[14] L. H. Rodovalho, C. R. Rodrigues and O. Aiello, "CMOS inverter linearization technique with active source degeneration", in proc. of 2021 IEEE Nordic Circuits and Systems Conference (NorCAS), Oslo, Norway, 26-27 October 2021.

[15] G. Manfredini, A. Catania, L. Benvenuti, M. Cicalini, M. Piotto, and P. Bruschi, "Ultra-Low-Voltage Inverter-Based Amplifier with Novel Common-Mode Stabilization Loop," MDPI Electronics, vol. 9, no. 6, p. 1019, Jun. 2020.

[16] P. Bruschi, A. Catania, S. Del Cesta and M. Piotto, "A Two-Stage Switched-Capacitor Integrator for High Gain Inverter-Like Architectures," IEEE Trans. Circ. Sys II, vol. 67, no. 2, pp. 210-214, Feb. 2020.

[17] L. Benvenuti, A. Catania, G. Manfredini, A. Ria, M. Piotto, and P. Bruschi, "Design Strategies and Architectures for Ultra-Low-Voltage Delta-Sigma ADCs," MDPI Electronics, vol. 10, no. 10, p. 1156, May 2021.