A cryogenic SRAM based arbitrary waveform generator in 14 nm for spin qubit control

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Abstract—Realization of qubit gate sequences require coherent microwave control pulses with programmable amplitude, duration, spacing and phase. We propose an SRAM based arbitrary waveform generator for cryogenic control of spin qubits. We demonstrate in this work, the cryogenic operation of a fully programmable radio frequency arbitrary waveform generator in 14 nm FinFET technology. The waveform sequence from a control processor can be stored in an SRAM memory array, which can be programmed in real time. The waveform pattern is converted to microwave pulses by a source-series-terminated digital to analog converter. The chip is operational at 4 K, capable of generating an arbitrary envelope shape at the desired carrier frequency. Total power consumption of the AWG is 40-140 mW at 4K, depending upon the baud rate. A wide signal band of 1-17 GHz is measured at 4K, while multiple qubit control can be achieved using frequency division multiplexing at an average spurious free dynamic range of 40 dB. This work paves the way to optimal qubit control and closed loop feedback control, which is necessary to achieve low latency error mitigation and correction in future quantum computing systems.

Index Terms—Quantum control electronics, cryogenic CMOS, quantum computing, arbitrary waveform generator, SRAM, spin qubit systems, 14 nm bulk FinFET technology

I. INTRODUCTION

A continuous trend in the scaling of qubit numbers in quantum systems has been established over the past few years. Realization of large scale error corrected qubit systems would demand the miniaturization and integration of different components inside the cryostat. The scaling bottleneck of quantum control systems has motivated the cryo-CMOS community to explore the prospects of cryogenic circuit design at 4K and below. The major challenge is to meet the reliability and performance requirements put forth by the future quantum computing systems, while consuming the least amount of power, limited by the available cooling power in the cryostat. Short and optimized control pulses are the key to realize fast gubit gates with improved gate fidelity. Fast gates suffer from leakage effects and additional unitary errors caused by the large bandwidth of the short control pulses [1]. Adopting techniques to increase the fidelity of short duration single qubit gates using optimized control pulses in a closed-loop fashion is crucial to build low error quantum systems [2].

Spin systems have an advantage of being able to operate at higher temperatures. CMOS compatible FinFET spin qubits operating at 1-4 K have been demonstrated by [3]. Scaling of quantum computing systems beyond 1000 qubits, irrespective

of their qubit technology, puts forth an inevitable need for intelligent sub-systems operating at proximity to the qubits. These include cryogenic control and readout circuitry with maximum affordable signal processing capabilities to ensure low-latency error correction and reduced data rate for links to room temperature, as shown in Fig. 1a. We propose an SRAM based arbitrary waveform generator, that paves the way to such systems. Advanced CMOS technology such as 14 nm bulk FinFET offers high interconnect density to support digitally assisted designs that are scalable. Control and readout circuitry implemented in advanced CMOS process nodes like 14 nm and below could be potentially co-packaged with spin qubit arrays, a well-known advantage of spin systems over other platforms. A radio frequency (RF) digital to analog converter (DAC) with wide bandwidth and sufficient spurious free dynamic range (SFDR) could be used to control multiple qubits using frequency division multiple access (FDMA). Apart from simplifying the wiring bottleneck in the cryostat, the merits of using FDMA over 1:1 qubit to control DAC ratio for large scale error corrected systems need to be evaluated.

The source series terminated (SST) transmitter proposed in [4] and its improved version [5] have a proven track of record in high speed I/O links applications. The advantages of SST concept are low power operation, high content of digital circuitry that supports scaling, and comparatively large signal swing. These concepts found their application in quantum control electronics owing to their scalability and overlapping specifications with high speed IO links, with design enhancements to achieve low power. The transmitter used in this work was designed by C. Menolfi et al., as a single ended adaptation of [4]. The main difference in architecture compared to the SST transmitter from [4], is the digital part with an SRAM based pattern generator. SRAM based architectures offer high versatility with the ability to store multiple gate sequences for qubit control. Moreover, they allow the control signals to be pre-distorted, in order to compensate the non-linearities and drifts caused by cabling. It helps to mitigate the effect of intersymbol interference (ISI) caused by cabling via feed forward equalization (FFE) at no added power cost.

II. CHIP ARCHITECTURE

The RF DAC architecture shown in Fig. 1b is an 8-bit SRAM-based single-ended SST transmitter. Four dedicated SRAM instances, each 512×16 B provide a total 32 KB onchip memory. There is a 8×32 b wide interface between

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Fig. 1: Figure showing the SRAM based RF AWG architecture, together with the envisioned cryogenic qubit control system co-packed with hot spin qubits at 1-4 K. The proposed AWG can be integrated into a closed-loop feedback control system

SRAM and DAC TX. A 1/32-rate clock, C32, is used for the data capture at the DAC TX input as well as with opposite phase for the clocking of the SRAM. Because the most significant bit (MSB) is thermometer encoded to improve the linearity and also reduce the fanout spread between MSB and least-significant bit (LSB) weights in the DAC output stages, the 8 b resolution is implemented with nine 32:4 serializers that multiplex the input data to 9×4 b data streams at quarter-rate. Each quarter-rate data stream drives a specific DAC weight consisting of 4:1 multiplexer, pre-driver and SST output stage. The DAC weights are segmented into 6b binary weights between LSB and MSB-2 while the MSB and MSB-1 define the thermometer-encoded weights. The inclusion of the 4:1 multiplexer into each DAC segment increases the overall clock load but enables identical loading at the full data rate amongst all DAC weights, leading to superior timing jitter performance.

The clock path operates on an incoming half-rate clock, C2, that first goes into a duty-cycle correction (DCC) block followed by a frequency divider (DIV2) to produce quadrature clocks. Hence the DCC block in front of the DIV2 allows a quadrature-error correction (QEC). It is implemented as an AC-coupled trip-point-biased inverter with programmable bleeding current. Each quadrature clock is followed by a separate DCC block to adjust the duty cycle of the pertinent quadrature phase pairs. The quarter-rate quadrature signals C4I and C4Q are fed to the 4:1 multiplexers of the DAC segments as well as to the 32:4 serializers together with the sub-rate clocks C8, C16 and C32 that are derived from C4I via frequency division in the clock path.

The digital part consists of a pattern generator and a bidirectional serial interface as shown in Fig. 2a. The pattern generator is responsible for generating a 256 b input pattern to the RF DAC. It consists of a controller state machine, 32 KB

SRAM, data path logic with byte rotational capability and a digital serializer. The design is implemented in a 14 nm bulk CMOS FinFET technology and has an active area of 0.095 mm², including T-coil, ESD and SRAM.

III. CRYOGENIC MEASUREMENTS

The experiments described in this work were conducted at room temperature, liquid N₂ and He (300 K, 77 K, 4 K) on a dip stick set up. The chip was packaged in a miniature PCB mounted in a cryogenic dip stick shown in Fig. 2b. The bandwidth of interest is identified as 4-8 GHz, that matches both transmons and the spin qubits in general. The experiments target the control requirements of the spin system described in [3]. Fig. 2c shows measured sub-5 ns pulse sequences at 4 K, showing granular control over their amplitude, pulse duration and spacing. At 4K the measured signal shows larger signal amplitude when compared to the same measurement at room temperature and 77 K (not shown in the figure). The effect could be attributed to a combined effect of increase in the device drain saturation current for a given applied potential [6] and reduced cable losses in the dip stick. To perform linearity measurements, the DAC was programmed to output all 256 codes, creating a DC ramp in steps at the output. 1000's of samples were averaged for each DAC input code to calculate the output voltage. The measured INL at 4K is < 2 LSB and DNL is < 1 LSB. The ratio between MOS resistance and metal resistance does not appreciably vary over temperature, which makes the SST driver topology in this technology exceptionally linear over such broad temperature range, compared to the current steering DAC in [8].

Fig. 2d and 2e show a two tone raised cosine pulse of width 200 ns in time domain and frequency domain respectively. A power of -33 dBc IM3 at -43 dBm is calculated from Fig. 2e,



Fig. 2: (a) Simplified block level representation of the pattern generator (b) Chip Micrograph (bottom), dip stick setup (top) (c) Measured Gaussian sequences with programmable amplitude, pulse duration and spacing at 4 K (d) Time domain dual-tone raise cosine signal (e) Frequency domain shows the 3rd order intermodulation products at 4 K for 5.1 and 5.3 GHz. The magnitude is normalized to the largest amplitude corresponding to clock feedthrough at 7 GHz (f) Measured frequency response

measured at 4 K for a dual tone output of 5.1 GHz and 5.3 GHz. The tones are spaced 200 MHz apart to match the qubit spacing in [3]. A 40 dB average spurious free dynamic range is achieved over a wide bandwidth of 1 to 17 GHz, which is in accordance with the current state of the art. The total harmonic distortion is less than 2%. The operational frequency range allows the control of multiple spin qubits with different Larmor frequencies, based on the assumption that a large multiplexing ratio will be supported by the error corrected spin systems in future.

Jitter measurements were performed to analyze the drift on the control signal. Optimal linear equalizer coefficients for the cryogenic set up were calculated for a known pattern such as PRBS7. A 35% reduction in deterministic jitter is observed after feed forward equivalization (FFE) Fig. 3d. A square wave output at 5 GHz, with FFE, shows < 2 ps deterministic jitter at 4 K as shown in Table I. One of the advantages of SRAM based AWG architecture lies in its ability to adapt the FFE coefficients to equalize the changes in cryostat cabling over time. Since it is done through input data pattern, no extra power is required. Moreover, it facilitates real time calibration.

Fig. 3b shows the power measurements at 4 K. The SRAM is programmable throughout supply and frequency range shown in Fig. 3b. The power consumption could be further minimized

by dynamically lowering the power supply of the SRAM, while the data is held safe. Although the digital part of the design operates at a fraction of the reference clock, the total power consumption increases with the sampling frequency $(2 \times \text{reference clock})$, as shown in Fig. 3b. On the other hand, high frequency operation of RF up conversion architectures [7]- [9] would demand high frequency LO and mixer, adding up to their total power consumption. The digital blocks consume only 20% of the total power, where as the power consumption of [8]- [9] is largely dominated by the digital part as shown in Table II. The total power consumption is often reported as power per qubit for a given number of frequency multiplexed qubits per controller. This ratio may vary depending upon the DAC bits, linearity, target SFDR, qubit frequency spacing, etc. A total power of 2-4 mW/qubit can be estimated for the proposed controller, with a multiplexing ratio of 1:20 (drive:qubit) in our target qubit platform [3], with the qubit frequency spacing of 200 MHz within 4-8 GHz band.

TABLE I: Jitter measurements for square wave at 5 GHz

Temperature	Total jitter ^a	Random ^a	Deterministic ^a
300 K	4.80 ps	0.237 ps	1.56 ps
77 K	5.91 ps	0.239 ps	2.64 ps
4 K	4.98 ps	0.221 ps	1.95 ps

^aMeasurements were done using precision timebase scope.

CONCLUSIONS

A study on the cryogenic operation of an SRAM based AWG with an RF DAC in 14 nm FinFET technology is reported. The proposed AWG can generate RF control pulses of any envelope shape with programmable amplitude, carrier frequency, pulse spacing and duration. Furthermore, it enables real time feed forward equalization to compensate drift due to changes in the cryostat cabling, at no added power cost. The SRAM is fully functional and programmable at 4K, within the given voltage and frequency range. The proposed digitally dominated architecture eliminates the need of local oscillators and mixers, reaping the benefits of scaling in advanced CMOS nodes, such as 14 nm or below. The measured wide signal band of 1 GHz to 17 GHz at 4 K is in accordance with the specifications of transmons and spin qubits developed thus far. Mutiple qubit control can be acheived via frequency multplexing with a target average spurious free dynamic range of 40 dB. The proposed AWG architecture supports system level integration of a cryogenic signal processor, leading to fully integrated, feedback based qubit control systems at 4K.

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TABLE II: Comparison with current state of the art

[Features	This work	[9]	[8]	[7]
	Qubit Platforms	spin	spin	transmons, spin	transmons
	Functionality	RF control	Gate pulsing, RF control, Readout	RF control	RF control
ĺ	Chip area	0.5 mm ²	16 mm ²	$4 \mathrm{mm^2}$	1.6 mm ²
	Technology	14 nm FinFET	22 nm FinFET	22 nm FinFET	28 nm bulk
	Power consumption	Total power: 40-140 mW Analog: 32-54 mW Digital: 8-16 mW	Total drive power ^b : 93-223 mW Analog: 83 mW or 5.2 mW/qubit Digital: 10- 140 mW	Total power ^b : 384.4 mW Analog: 54.4 mW or 1.7 mW/qubit Digital: 330 mW	2 mW/qubit
	Frequency multiplex- ing	yes	yes	yes	no
	Drive to qubit ratio	N/A	1:16	1:32	N/A
	Frequency range	1-17 GHz	11-17 GHz	2-20 GHz	4-8 GHz
	IM3	−33 dBc at −43 dBm	$-50 \mathrm{dBc}$ at $-17 \mathrm{dBm}$	$-50 \mathrm{dBc}$ at $-18 \mathrm{dBm}$	N/A
	On-chip storage	32 KB SRAM	RAM, digital memory	SRAM	Digital memory
	Waveform storage	32 K points AWG	16 K points AWG	40 K points AWG	Fixed 22 points
ļ	DAC bits	8	10	10	11

^b Calculated by multplying the reported power/qubit by the reported number of qubits per controller for the given system

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Fig. 3: (a) SFDR plots with unaccounted cable losses at 4K (b) Power vs Sampling clock and Supply voltage at 4K. The SRAM is programmable throughout the range. (c) Power breakdown chart at 14 GHz and 0.8 V, (d) PRBS7 eye diagram at 20 GS/s at 4K shows that the deterministic jitter due to cabling improves by 35% by applying feed forward equalization