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Characterization and Modeling of BTI in SiC MOSFETs

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***Abstract*—SiC power MOSFETs have been investigated by performing two different kinds of measurements, the hysteresis between two adjecent sweeps and the positive bias temperature instability, at different temperatures. The threshold hysteresis is a measure of the switching dynamics of the interface traps, while measurements at long stress times can reveal the role of an additional interface degradation. In order to fully understand the role played by the latter mechanisms, TCAD simulations have been calibrated in order to reproduce the experimental results.**

1. Introduction

Compared to Si, SiC has superior characteristics such as thermal conductivity, wide bandgap and critical electric field which make it an ideal material for the fabrication of power MOSFETs. The benefits provided by SiC include operating at higher temperature and at higher frequency, but they still suffer for reliability issues significantly more than their Si counterparts [1]. More specifically, the threshold voltage shift (ΔV_{th}) in SiC-MOSFETs under positive and negative gate biases are significantly higher, though recovering faster, than the ones observed in Si-MOSFETs [2]. The latter is due to the presence of a high density of electrically active defects at the SiC/SiO$_2$ interface, with at least two orders of magnitude higher concentrations compared to the Si/SiO$_2$ systems [3][4]. The improvement of the SiC/SiO$_2$ interface is of vital importance for MOS applications, because charged interface traps directly affect not only the threshold voltage but also the channel mobility. In addition to this, the origin and energetic distribution of defects in SiC/SiO$_2$ systems is still unclear and needs further investigation. To this purpose, TCAD modeling and simulation can be used to effectively study and analyze reliability issues in semiconductor devices, as it has been demonstrated to be a comprehensive tool [5]. In particular, the reaction-diffusion model implemented in the Synopsys TCAD solver has been proven to emphasize the physical aspects of the interface degradation and recovery under BTI phenomena [6] [7] [8]. In this work, an experimental study based on measurements of hysteresis and positive bias temperature instability (PBTI) of a commercial SiC MOSFET carried out at different ambient temperatures is reported along with a TCAD simulation setup calibrated in order to qualitatively explain the anomalous temperature dependence of the V_{th} shift.

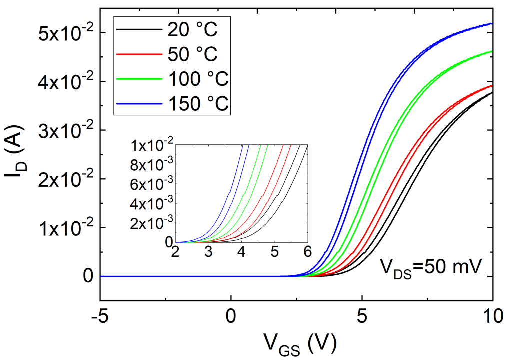

Figure 1. I_D-V_{GS} hysteresis measured at different temperatures in SiC MOSFET. Inset highlights that the amplitude of the hysteresis loop at a fixed current level decreases by increasing the temperature.

2. Experiments

Hysteresis and PBTI measurements were performed on packaged commercial SiC power MOSFETs by using the parameter analyzer Keithley 4200-SCS. The hysteresis measurements have been obtained by sweeping the V_{GS} from -5 V to 10 V and vice versa, at V_{DS} = 50 mV. The minimum voltage was fixed at -5 V, in order to reset the device characteristics. As shown in Fig. 1, the current increases with temperature due a significant decrease of the threshold voltage. It is worth noting that the hysteresis amplitude at a fixed current level decreases with temperature (see inset of Fig. 1). PBTI stress measurements were performed at different temperatures and stress voltages with V_{DS} = 50 mV (Fig.2). The measurement procedure consisted of four steps: i) the device was biased with a negative gate voltage of - 5 V for 10 s, with the purpose of reaching a reproducible reference state; ii) the reference I_D-V_{GS} curve was measured by sweeping V_{GS} from -5 V to 5 V; iii) the device was biased again with a negative gate voltage

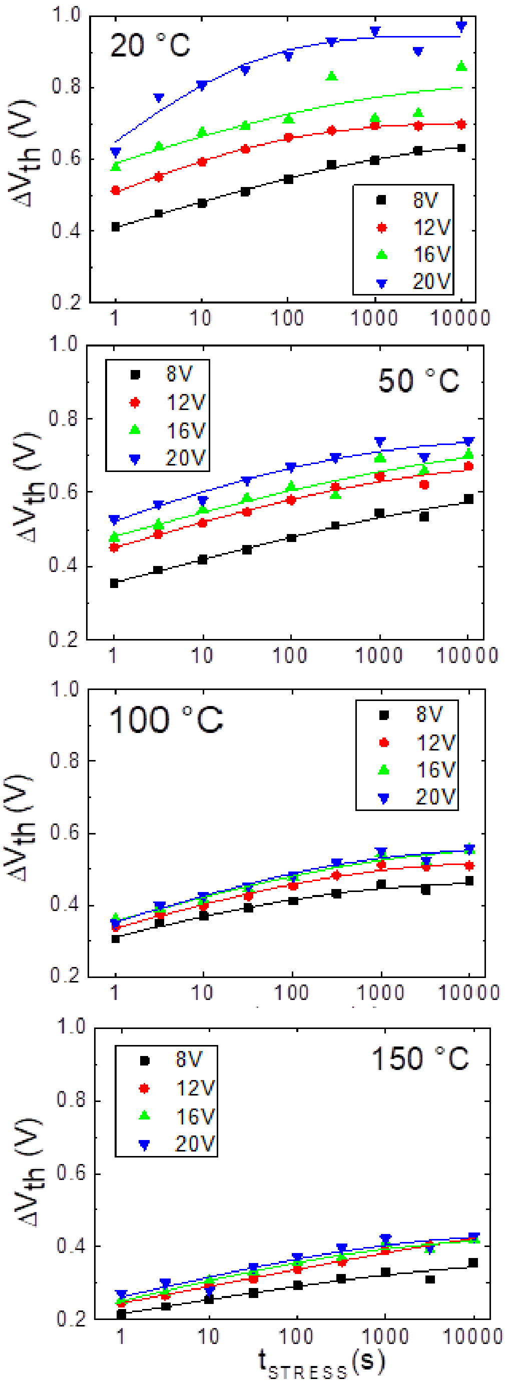

Figure 2. PBTI-induced ΔV_{th} evolution for different temperatures and stress voltages. At long stress times, ΔV_{th} tends to saturate. PBTI degradation exhibits an anomalous decrease with temperature.

of - 5 V for 10 s; iv) PBTI degradation was monitored by applying a high gate voltage (between 8 V and 20 V) and by interrupting the stress at fixed time intervals in order to sense I_D at low gate voltage (V_{GS} = 3 V). By using the reference I_D-V_{GS} curve, the measured I_D at low gate voltage was converted into the threshold voltage shift ΔV_{th}.

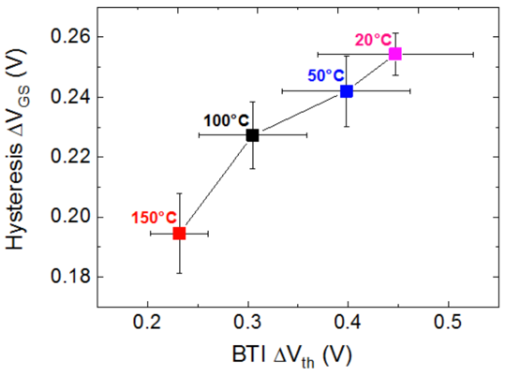

Figure 3. Mean value of the hysteresis amplitude evaluated at I_D = 5 mA versus mean value of ΔV_{th} induced by a PBTI stress (V_{stress} = 20 V and t_{stress} = 1 s) measured in 8 samples at different temperatures. A clear correlation between hysteresis and PBTI is observed.

This characterization technique allows to reduce the recovery mechanisms occurring when the gate stress voltage is completely removed [9]. Two main messages can be drawn from the data reported in Fig. 2. First, PBTI degradation tends to saturate at high stress times (more than 1000 s) for all investigated temperatures and stress voltages. Second, ΔV_{th} exhibits an anomalous decrease with temperature, opposite to the behavior observed in Si MOSFETs [2]. In order to evaluate the correlation between hysteresis and PBTI, we performed measurements on a set of 8 samples at different temperatures. Fig. 3 shows the mean value of the hysteresis amplitude evaluated at a fixed current level (I_D = 5 mA) versus the mean value of ΔV_{th} induced by a PBTI stress (V_{stress} = 20 V and t_{stress} = 1 s). The two phenomena exhibit similar temperature dependence and are strongly correlated, suggesting that the same physical mechanism is the main factor responsible for hysteresis and PBTI.

3. TCAD setup calibration

Due to the lack of information on the specific technology of the measured SiC power MOSFETs, we used published data on a similar device to calibrate the physical models in the TCAD setup. More specifically, a 4H-SiC power MOSFET with a p-body retrograde profile with a blocking voltage of 1.3 kV has been used as reference [11]. The TCAD deck has been realized using the device geometrical description and channel doping given in the paper. The schematic view is shown in Fig. 4. Material-specific models for the incomplete ionization and the channel mobility, accounting for the role of Coulomb scattering, surface roughness and interface charge, have been adopted in the TCAD setup to investigate the device characteristics. The physical models have been used with default parameters. The interface trap profile ($D_{it}(E)$) has been extracted by directly comparing the simulated and measured transfer characteristics at two different drain-source voltages as far as the trap density in the upper half of the SiC band-gap is concerned (Fig. 5). These traps have been specified as acceptor-like, thus

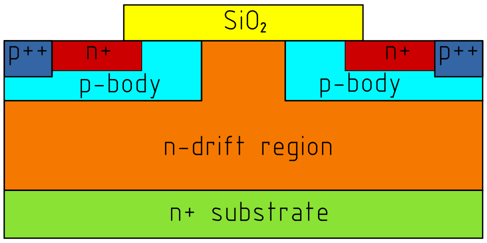

Figure 4. Schematic view of the SiC-MOSFET structure.

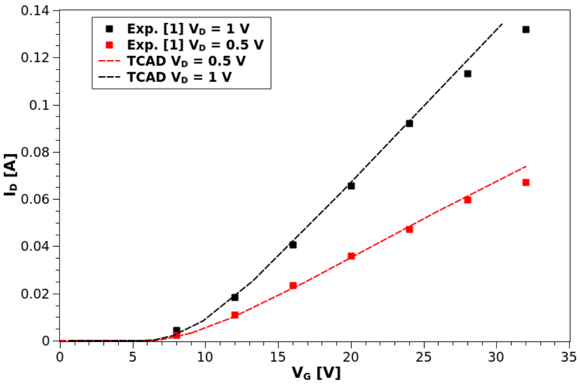

Figure 5. Turn-on characteristics of the MOSFET at different drain voltages. Solid lines: TCAD simulations. Symbols: experiments [11].

the filled traps are negatively charged and would degrade the channel mobility. The extracted $D_{it}(E)$ shows an exponential tail close to the conduction band edge, and it is in agreement with other sets extracted from SiC devices [3], [10] (Fig. 6).

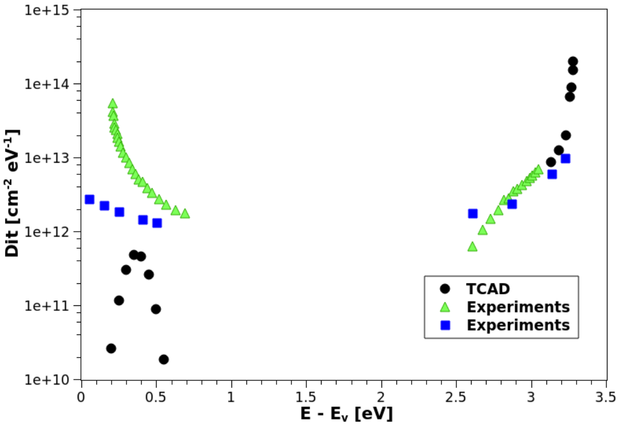

Figure 6. Interface state density as a function of energy from the top of the SiC valence band to the bottom of the conduction band. Green triangles and blue squares are the extractions reported in [3] and [10], respectively. Black circles correspond to the acceptor trap distribution used in this work.

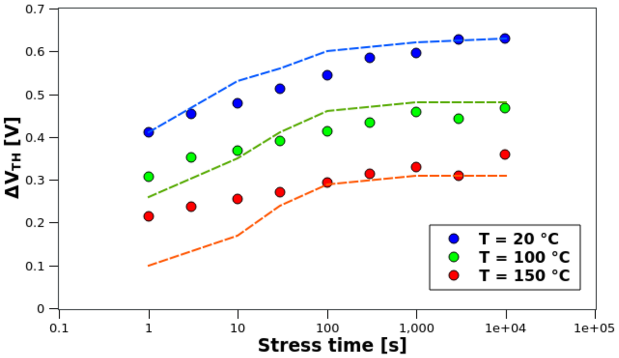

Figure 7. Threshold voltage shift as a function of stress time at different tempertures. TCAD simulations (dashed lines) are in a nice agreement with experiments at $V_{\rm stress} = 8$ V (filled circles).

4. Simulation of the V_{th} instability

The experimental investigations reported in Figs. 1 and 2 show that the V_{th} instability consists in a drain-current hysteresis resulting from signals varying at relatively fast times ($0.1 - 1$ s), and of an additional degradation mechanism resulting from the application of a positive gate voltage for long stress times. The first effect has been modeled in the TCAD setup by means of an additional Gaussian distribution of acceptor-like traps at the SiC/SiO$_2$ interface with a peak density of 6×10^{11} cm^{-2}eV^{-1} at 0.42 eV from the valence band, as shown in Fig. 6. The presence of such a defect is in agreement with the extracted data in [3] and [10], while the trap cross-section has been calibrated in order to obtain trapping/detrapping effects for stress ramps in the range between $0.1 - 1$ s as provided during turn-on measurements. We carried out TCAD simulations of the PBTI stress by following the experimental approach, starting with a negative gate voltage at -5 V for 10 s before the application of $V_{\rm stress}$. Simulations have been carried out at different temperatures, and we found a nice agreement against experimental ΔV_{th} up to 150 °C (Fig. 7). The added Gaussian distribution of traps would lead to a complete saturation of the ΔV_{th} for stress times longer than 1 s and independent of $V_{\rm stress}$, while experiments clearly show a field-driven increase of ΔV_{th} which can be referred to a positive bias temperature instability (PBTI). In the last years, several methods have been proposed to describe such kind of phenomena in the TCAD framework [7], [8], [12], [13], [14]. Among them, the reaction-diffusion model by Alam [7] has been demonstrated to be an effective physically-based approach which nicely predicts NBTI reliability data [5]. Here, we adopted the reaction-diffusion degradation equations to investigate the PBTI curves for stress times up to 10^4 s and different temperatures. This model accounts for the generation of defects at SiC/SiO$_2$ interface caused by the breaking of the passivated Si-H bonds. The released hydrogen diffuses away from the interface into the oxide layer and might recombine during recovery. Thus, a counteracting effect is expected also during the degradation, when the increase of ΔV_{th} is measured. At long stress times, the model nicely predicts the ΔV_{th} saturation when all the Si-H bonds are broken. In addition to this, the anomalous temperature dependence observed in the experimental curves is reproduced by the proposed

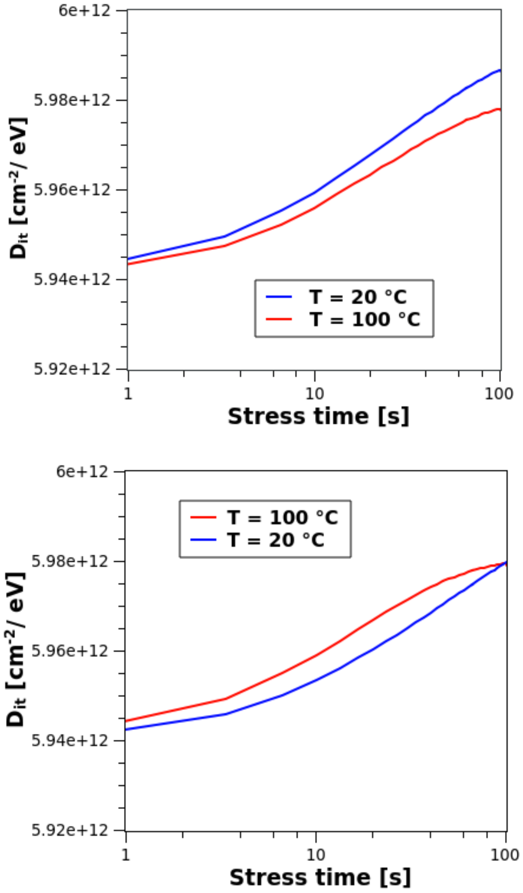

Figure 8. Simulated interface trap density as a function of the stress time obtained for two different activation energies of the diffusion coefficient in the reaction-diffusion model. Top: a faster recovery takes place when a large activation energy is assumed, the generated trap concentration is consistent with a reduced degradation at higher temperatures. Bottom: the opposite behavior is obtained assuming a lower activation energy.

approach. The latter can be ascribed to the temperature-enhanced recovery which reduces also the saturation level of ΔV_{th} (Fig. 7).The physical explanation for such a behaviour was given in [2] as due to a significant unbalance between the thermal activation of charge capture during the electrical stress and that of the recoverable components. We consistently tuned this effect in the reaction-diffusion model by changing the activation energy in the exponential temperature dependence of the hydrogen diffusion coefficient (E_A). As shown in Fig. 8, a change in E_A can unbalance the recovery with respect to the degradation giving both a reduction (top) or an increase (bottom) of trap generation with temperature.

5. Conclusion

The threshold voltage instability of SiC power MOSFETs has been measured at different ambient temperatures. In order to fully understand the role played by the degradation mechanisms, TCAD simulations have been carried out by assuming a specific distribution of interface traps and the reaction-diffusion degradation model. The temperature dependences of the experimental results are nicely explained by the proposed TCAD approach, suggesting that a combination of both effects is observed and that a different activation energy in the diffusion of hydrogen is experienced in SiC MOSFETs with respect to Si ones.

Acknowledgments

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