Back-end-of-line CMOS-compatible diode fabrication with pure boron deposition down to 50 °C

Tihomir Knežević, Tomislav Suligoj
University of Zagreb, Faculty of Electrical Engineering and Computing, MINEL, Zagreb, Croatia
tihomir.knezevic@fer.hr

Xingyu Liu, Lis K. Nanver
University of Twente, Faculty of Electrical Engineering Mathematics & Computer Science, Enschede, The Netherlands

Ahmed Elsayed, Jan F. Dick, Joerg Schulze
University of Stuttgart, Institute for Semiconductor Engineering, Stuttgart, Germany

Abstract— **Pure boron deposited on silicon for the formation of p^+n-like junctions was studied for deposition temperatures down to 50 °C. The commonly used chemical-vapor deposition method was compared to molecular beam epitaxy with respect to the electrical characteristics and the boron-layer compactness as evaluated by etch tests, ellipsometry and atomic force microscopy. Electrically, the important parameters are minority carrier electron injection into the p-type region and the sheet resistance along the boron-to-silicon interface which appear to be independent of deposition method for temperatures down to 300 °C. Only with molecular beam epitaxy did we succeed in producing substantial layers for the lower temperatures down to 50 °C. Also, at this very low temperature, p^+n-like diodes were formed, but the suppression of electron injection was less efficient than at the higher temperatures. From simulations, assuming that the attractive electrical behavior is due to a monolayer of fixed negative charge at the interface, the concentration of holes needed to explain the *I-V* characteristics is estimated to be 1.4×10^{11} cm^{-2} for 50 °C deposition and 1.1×10^{13} cm^{-2} for 400 °C.**

Keywords— chemical vapor deposition (CVD), electron injection, fixed interface charge, molecular beam epitaxy (MBE), pure antimony, pure boron, silicon diodes, ultra-shallow junctions

I. INTRODUCTION

Junction formation by pure boron (PureB) deposition is a fabrication technique that can break physical and technical limitations imposed by conventional doping techniques used to form p^+n junctions with ultra-shallow, high concentration doping profiles. With chemical-vapor deposition (CVD), electrically active PureB layers have been deposited on silicon (Si) from 700 °C down to temperatures as low as 250 °C [1] making this a back-end-of-line (BEOL) complementary metal-oxide-semiconductor (CMOS) compatible way of fabrication p^+n-like diodes. At temperatures below 400 °C, drive-in of deposited B atoms into Si is not expected. Nevertheless, attractive properties of the high-temperature depositions are preserved such as saturation/ leakage currents that are decades lower than in comparable Schottky diodes. It has been proposed that these low current levels are a result of negative fixed charge at the PureB-Si interface which attracts holes and provides a high electrical field gradient up to the interface for suppressing the injection of electrons from the n-substrate. The resulting low reverse currents, together with an exceptional robustness of the PureB interface to the Si as well as the bulk boron layer itself, has been pivotal for the application to photodiodes for high-dose beams with low-penetration depths in Si, such as vacuum-ultraviolet light and low-energy electrons [2], [3].

Besides the applications to ultrashallow photodiodes, PureB has also displayed a high resistance to the standard Si etchants tetramethyl ammonium hydroxide (TMAH) and potassium hydroxide (KOH). Nanometer-thin CVD PureB layers have been shown to form efficient masking layers for etching cavities and for forming B membranes for deposition temperatures down to 400 °C [4]. As the temperature is lowered, the B-layer becomes less compact and surface roughness is increased. For micro-electro-mechanical system (MEMS) applications this can improve the stress situation while the etch selectivity remains high [4]. However, for the electrical application this means that the layer must be made thicker to avoid the formation of weak spots through which the metallization can approach the Si surface and give Schottky-like leakage currents [5]. In the literature, other techniques such as molecular beam epitaxy (MBE) and electron-cyclotron-resonance (ECR) argon plasma-enhanced CVD for depositing B layers were also reported, but with the goal of capping monolayer-thin B layers with a thin layer of crystalline Si to promote hole activation [6], [7]. For photodiode applications, this configuration did not offer good stability and robustness found for PureB photodiodes.

A first device application of 650 °C MBE PureB was reported in [8] where the layer was implemented as the collector of an insulted-gate bipolar transistor. In the present paper, we give a first detailed investigation of MBE PureB layers deposited from 50 °C to 400 °C and used to fabricate BEOL CMOS-compatible diodes. The compactness of the layers was evaluated by performing etch tests, ellipsometry and atomic force microscopy (AFM) measurements. Electrical characteristics of MBE-grown PureB devices such as minority carrier electron injection and sheet resistance were measured and compared to characteristics of CVD-deposited PureB devices. Both, compactness and electrical characteristics were seen to degrade as the substrate temperature was reduced but still the B formed p^+n-like diode *I-V* characteristics even at 50 °C. It was also possible to deposit the pure n-type dopant antimony (PureSb) on p-type

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Si by using MBE. Reports in the literature about material analysis experiments suggest that a positive charge-layer density > 10^{13} cm^{-2} can be formed when thin Sb layers capped by Si are deposited on Si substrates [9], [10]. A first attempt to make n^+p diodes in this way is presented in the last section.

II. Material Analysis

A. Deposition procedure

The compactness of the PureB layers was analyzed on blanket deposited samples. The substrate was a (100) p-type Si wafer with resistivity 10-20 Ω-cm. Prior to MBE deposition, native oxide was removed with a dip in diluted hydrofluoric acid (HF) followed by an *in-situ* thermal desorption under ultra-high vacuum (UHV) conditions at a substrate temperature, T_{sub}, of 700 °C to remove the H coverage built up on the surface during the HF-dip. The PureB layer is deposited from a Knudsen effusion cell of elemental B. The base pressure in the MBE was 10^{-11} mbar. The deposition was first made on Si samples without heating the substrate which resulted in heating of the sample to 50 °C due to radiation emission from the B effusion cell. For the subsequent depositions, T_{sub} was 200 °C, 300 °C or 400 °C.

B. AFM analysis

The PureB surface topography at different deposition temperatures was analyzed by AFM with a scanning area of 1 μm^2. The results are shown in Fig. 1. The root-mean-square (RMS) height of surface roughness is similar for all deposition temperatures, about 3.5 nm. There is a clear difference in surface textures which can be explained by a reduction in mobility of the B atoms along the surface as the substrate temperature decreases [11]. At substrate temperatures below 400 °C, the mobility of B atoms is low, so after they are adsorbed on the surface, clustering is limited, and the coverage is homogenous. At T_{sub} = 400 °C, a finer grain structure appears, indicating that a higher mobility allows the B atoms to move along the surface and cluster together. From CVD experiments it has also been found that at 400 °C the B atoms are more easily adsorbed to other B atoms rather than Si [12] which encourages a more peaked clustering.

The quality of MBE PureB layers was evaluated by monitoring the rate of PureB removal in Al etchant at room temperature. The thickness and roughness was extracted from ellipsometry measurements using the Bruggeman effective medium approximation [13] assuming a stack of compact B and 50% compact B. For the present layers it is not expected that they are 100% compact at any point, but the extracted values still give useful information on the relative layer

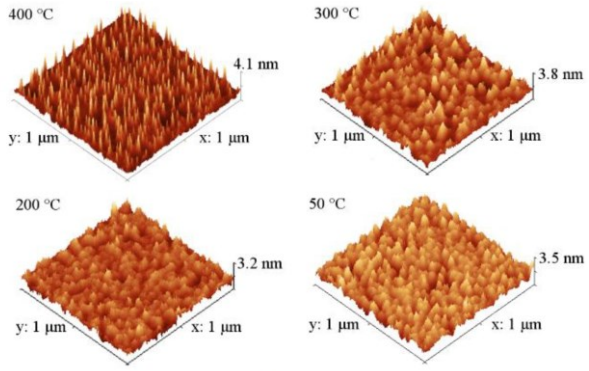

Fig. 1. AFM images of the surface topography of MBE PureB layers deposited at T_{sub} = 400 °C, 300 °C, 200 °C, and 50 °C.

TABLE I. Thickness and roughness extracted from ellipsometry measurements for MBE PureB samples etched in Al etchant at room temperature for different etch times.

Al etching	Thickness + roughness (nm)			
	T_{sub} = 50 °C	T_{sub} = 200 °C	T_{sub} = 300 °C	T_{sub} = 400 °C
as-deposited	1.54+2.31	1.58+2.12	1.56+1.83	1.62+1.64
30 sec	1.31+2.17	1.35+1.95	1.43+1.54	1.50+1.51
2 min	1.16+2.18	1.18+2.05	1.28+1.71	1.40+1.62
5 min	1.03+2.21	1.04+2.10	1.13+1.95	1.28+1.88
15 min	0.88+1.90	0.92+1.98	1.00+2.07	1.15+2.22

composition. The results as a function of etch time are listed in Table I. The initial thicknesses of the PureB layers were ~ 1.5 nm with a surface roughness of > 1.5 nm. The etch rate was slowest for T_{sub} = 400 °C indicating that this layer had the highest compactness.

More information on the integrity of the layers was obtained by immersing the samples in TMAH at 85 °C. CVD PureB layers have proven to be a very efficient barrier for TMAH etching [4], and TMAH etch tests can reveal weak spots in the layers. For the MBE samples, after 20 min exposure to TMAH, inspection with an optical microscope revealed no pinholes. However, after 2 hours, an extensive coverage of pinholes was observed on the samples deposited at T_{sub} = 50 °C as shown in Fig. 2. The coverage decreased as T_{sub} was increased and at 400 °C the only pinholes observed are related to mechanical damage of the sample surface. This suggests that the thermal energy supplied at higher temperatures enhances the strength and/or number of B-to-B bonds.

III. Electrical Characterisation

A. Electrical test structure fabrication

To extract electrical characteristics, PureB layers were deposited either by MBE or CVD in sheet resistance test structures that allow monitoring of the as-deposited layers by contacting the PureB-Si interface via B-implanted p^+-regions [14]. The structure, schematically shown in Fig. 3, is used to determine the sheet resistance along the B-Si interface, R_{SH}, and diode current-voltage (I-V) characteristics including the electron current component, I_e. The (100) Si substrate was n-type Si wafer with resistivity 1-10 Ω-cm. Probing pads and guard rings around the deposition regions were created by B^+ implant/ anneal to achieve a surface doping of 10^{19} cm^{-3} and a junction depth of 0.5 µm. The PureB was deposited in silicon dioxide (SiO_2) windows wet-etched to the Si. Directly before deposition, the wafer was dip-etched in diluted HF to remove

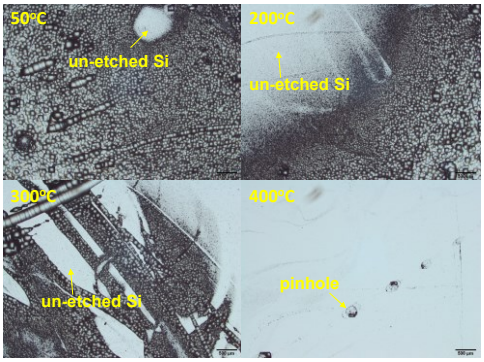

Fig. 2. Optical microscope images of MBE PureB deposited on Si at T_{sub} = 50 °C, 200 °C, 300 °C and 400 °C after TMAH etching at 85 °C for 2 hr.

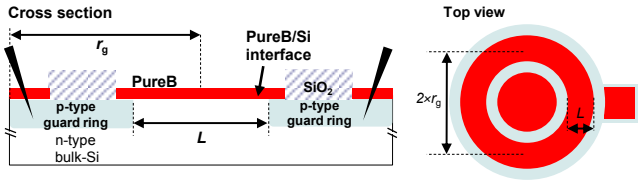

Fig. 3. Schematic cross section and top view of the basic ring-shaped devices that have PureB rings of varying width L and a radius r_g.

native oxide. The PureB CVD depositions were performed with diborane (B_2H_6) precursors in the temperature range from 250 °C to 400 °C in a commercial PicoSun atomic layer deposition (ALD) system [1] and from 400 °C to 700 °C in an ASM Epsilon 2000 reactor [2]. MBE depositions were performed as described in Section II.A.

B. Low temperature PureB depositions

The *I-V* characteristics of the MBE PureB diodes are shown in Fig. 4. They are all close to the characteristics of implanted p^+n diodes for which the current is dominated by hole injection into the substrate [15]. All characteristics displayed a small non-ideality that was similar for all devices including the implanted ones. Such leakage was not observed for the samples processed with CVD PureB. In the MBE case a slightly different pre-deposition processing could have caused excessive thinning of the SiO_2 and in addition, unlike with CVD, the MBE PureB is non-selectively deposited over the whole substrate.

In Fig. 5, the I_e at 0.2 V forward bias is plotted for the MBE samples and for the CVD samples reported in [1] and [14] for deposition temperatures from 250 °C to 700 °C. For all these devices the PureB layer was thicker than 2 nm. For the 600 ºC and 700 ºC devices, the B bulk Si doping gives a small additional reduction of the I_e. Below 450 ºC the I_e appears to saturate at ~ 45 pA for the CVD samples, which corresponds to a saturation current density of 9.6×10^{-20} A/µm^2. Devices with MBE PureB deposited at T_{sub} = 300 °C and 400 °C follow the same trend and almost the same suppression of electron injection is achieved. However, decreasing the deposition temperature down to 200 °C and 50 °C increases electron current to 330 pA and 2.45 nA which correspond to saturation current densities of 7×10^{-19} A/µm^2 and 5.2×10^{-18} A/µm^2, respectively. The large increase in electron injection at 50 °C suggests that the interface bonding between the B and Si that leads to hole accumulation at the interface is still taking place albeit not very effectively. From simulations of a simplified layer stack as presented in [1] an estimate of the hole

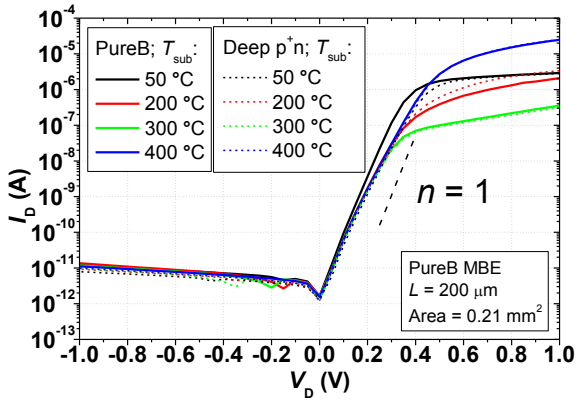

Fig. 4. Measured *I-V* characteristics of a non-metallized ring-shaped diodes with L = 200 µm fabricated using MBE deposited PureB layer at T_{sub} = 50 °C, 200 °C, 300 °C and 400 °C, compared to an implanted p^+n diodes.

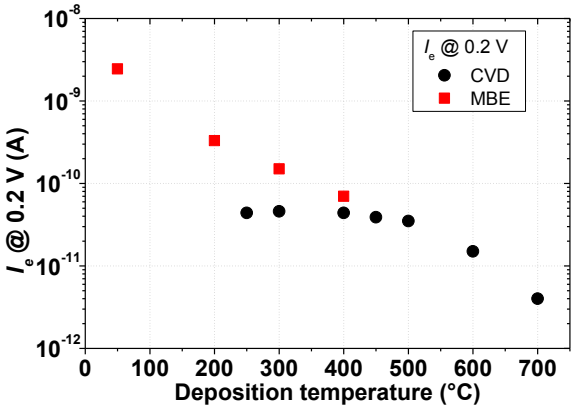

Fig. 5. Electron current as a function of deposition temperature for devices with MBE and CVD PureB layers.

concentration at the interface needed for achieving these saturation currents can be made. In the 400 °C case a hole concentration of 1.1×10^{13} cm^{-2} is found if the electron mass is assumed to be $m_e = 0.1\times m_0$, where m_0 is the electron rest mass. This decreases to 8×10^{11} cm^{-2} and 1.4×10^{11} cm^{-2} for the I_e values found at 200 °C and 50 °C, respectively. We speculate that the low temperature deposition does not provide enough energy to form and sustain a high concentration of negative fixed charge at the PureB-Si interface.

The same conclusion could be made from the sheet resistance measured along the PureB-Si interface on the same samples and plotted in Fig. 6. In contrast to the I_e that has a more or less constant value from 400 °C to 250 °C, the R_{SH} continues to increase as the deposition temperature is decreased. It becomes, just like the I_e, extremely high for the 200 °C and 50 °C depositions. These high values could also indicate that, besides a lower hole concentration, a higher density of interface defects could also be playing a role for degrading the R_{SH}.

IV. MBE PureSb Depositions – First Tests

It is suspected that the group III dopant nature of the B in Si plays a role in the formation of the fixed negative charge interface layer at the interface with Si. It could even be feasible, but difficult to determine experimentally, that the chemical rearrangement of the surface allows actual B doping in the top atom layers of the Si even at very low temperature. With this thought it becomes interesting to attempt an n^+p-like diode fabrication by depositing an n-type dopant on Si. Unfortunately, this has not been successful by CVD with standard n-dopants, As and P. They segregate on the surface

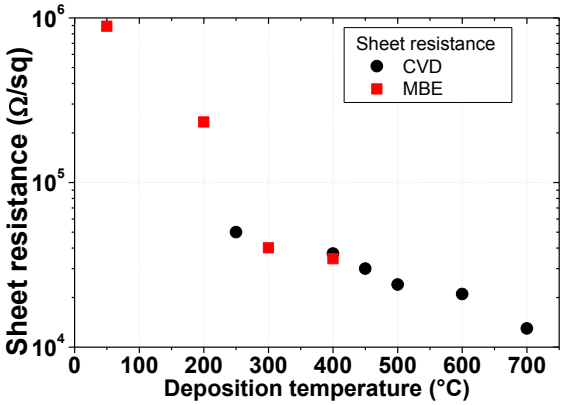

Fig. 6. Sheet resistance as a function of deposition temperature for devices with MBE and CVD PureB layers.

but do not readily build up substantial layers [16]. With MBE we were able to try an antimony (Sb) deposition. Our experiments were however not successful in monitoring any electrical activity that could be accorded to the formation of a n^+p-like junction.

For the PureSb deposition, we used test structures and fabrication equivalent to those used for PureB electrical characterization as described in more detail in [17] and schematically shown in Fig. 7a. The PureSb depositions were performed with T_{sub} = 400 °C, 500 °C or 600 °C. None of the samples showed any clear n-type diode characteristics that could be accorded to the PureSb-to-Si interface. The *I-V* characteristics for a 600 °C deposition are shown in Fig. 7b. The current levels increased with the perimeter of the regions where the implanted areas overlapped the PureSb-deposited areas, and they display no dependence on the area of the bare PureSb-to-Si ring areas. To avoid the effect of Sb oxidation in air, samples where the PureSb was capped *in-situ* with 20 nm Si were also fabricated. This only resulted in increased leakage currents that could be correlated to the above mentioned perimeter regions. Lowering of the deposition temperature also led to an increase in this leakage current.

V. Conclusions

Little more than 1.5-nm-thick PureB layers deposited by MBE at Si substrate temperatures from 400 °C down to 50 °C were shown to form p^+n-like diodes due to an effective suppression of electron injection from the n-substrate. The efficiency decreases with substrate temperature, and for 50 °C it is about a factor of 50 lower than for T_{sub} = 400 °C and the R_{SH} increased by decades. This was shown to be correlated to a less compact nature of the deposited PureB material, which was observed as an increase in roughness compared to CVD depositions, a higher etch rate of the layer in Al-etchant, and degradation of the masking of Si etching in TMAH. At T_{sub} = 400 °C the MBE-deposited PureB diodes display the same low I_e and R_{SH} as CVD-deposited PureB diodes, which suggests that the reaction at the Si surface responsible for the attractive electrical behavior is predominantly determined by the activation energy supplied by the surface temperature. Although results from the literature suggest that similar electrical behavior could be expected for PureSb deposition on p-type Si to form n^+p-like diodes, the first experiments with PureSb did not show any electrical behavior that could point in this direction. This underlines how versatile PureB is in having a deposition window from 50 °C to 700 °C for ultra-shallow p^+n-like diode formation.

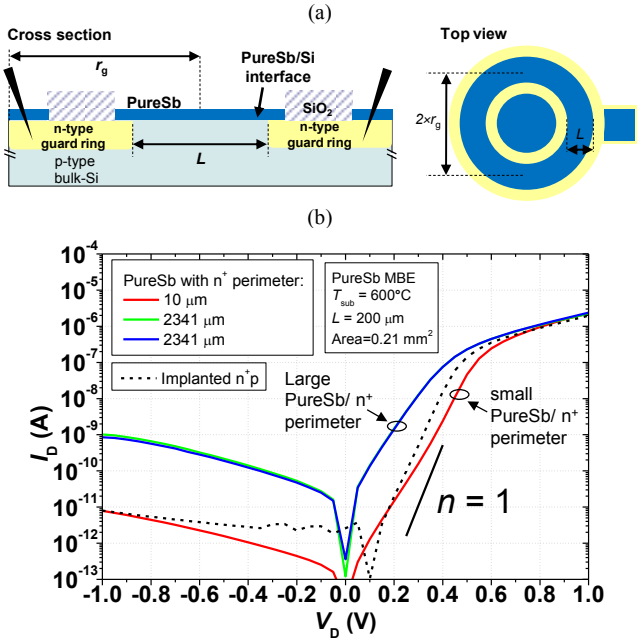

Fig. 7. (a) Schematic cross section and top view of the ring-shaped devices that have Sb deposited rings of varying width *L* and a radius r_g. (b) Measured *I-V* characteristics of a non-metallized ring-shaped diodes with *L* = 200 µm fabricated using PureSb MBE layer at T_{sub} = 600 °C, compared to an implanted n^+p diode.

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