Electrothermal modeling of junctionless vertical Si nanowire transistors for 3D logic circuit design

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Abstract*— *This work presents a comprehensive analysis of electro-thermal effects in emerging 3D vertical junctionless nanowire transistors (VNWFETs) using on-wafer measurements under a wide range of temperature and validated against numerical and compact model simulations. Experimental observations indicate an increase of the drain current with the temperature, conforming to the behavior of junctionless FETs. Multiphysics simulations reveal formation of temperature hot-spots that adversely affect thermal conductivity in smaller geometries. The VNWFET compact model was then modified to account for the underlying electro-thermal effects as well as dynamic self-heating. Model simulations and the experimental results at different measurement temperatures for different transistor geometries show good agreement. The developed SPICE-compatible compact model was then used for studying the impact of electrothermal effects on the performances of basic 3D logic circuits.

Keywords—***electrothermal effects, self-heating, compact model, vertical junctionless nanowire transistors, 3D logic circuit***

I. Introduction

The increasing use of "deep learning" in various areas of computer systems, such as natural language processing, image classification, and speech recognition, has led to an increasing demand for data processing and functionality [1]. New computing paradigms such as neural networks (NN) and in-memory computing have the potential to overcome the bottlenecks of CPU and storage performance differences of traditional von Neumann architectures, but have high hardware requirements in terms of computational efficiency and energy consumption [2]. To develop low-power, low-latency 3D NN compute cubes, beyond-CMOS technologies such as junctionless vertical nanowire transistors (VNWFET) are being considered as a solution. Its 3D vertical structure achieves a breakthrough in integration by vertically stacking several nanowires, thus increasing the number of devices accommodated per unit area. The transistor fabrication process is simplified due to the uniformly high doping in the junctionless channel, and gate-all-around (GAA) architecture (Fig. 1) offers better immunity against short channel effects (SCE) and improved gate control [3].

In order to exploit the full potential of this state-of-the-art, inherently 3D technology, logic circuit design efforts must leverage physics-based, accurate and efficient compact models for realizing innovative 3D circuit architectures through Design-Technology Co-optimization (DTCO) [4]. In particular, the many advantages of compact models in the context of design includes compatibility with design tools and computational efficiency through the use of analytical equations to describe carrier transport in transistors for all possible operating regimes. However, thermal management remains a critical issue for this technology especially due to a lack of understanding of nano-scale heat transport. Moreover, considering the non-classical behavior of junctionless transistors under temperature, it is crucial to take electrothermal effects into account for modeling and design efforts especially to study the impact of these effects on performance metrics such as energy consumption and delay.

In this work, we present a modified VNWFET compact model with integrated electro-thermal and dynamic self-heating effects. Multiphysics simulations are used to investigate the underlying thermal phenomena and identify physical device parameters (such as threshold voltage) that are impacted by these effects. The compact model is then modified to incorporate the temperature dependence of these parameters and is validated against experimental data and numerical simulation. The impact of electrothermal effects on the performance of logic circuits is then predicted through circuit simulations of basic logic cells. The rest of this paper is structured as follows: section II details the compact model improvements, and in section III, validation of the compact model is presented followed by a circuit level analysis to study the impact of electrothermal effects on the basis of the improved VNWFETs compact model.

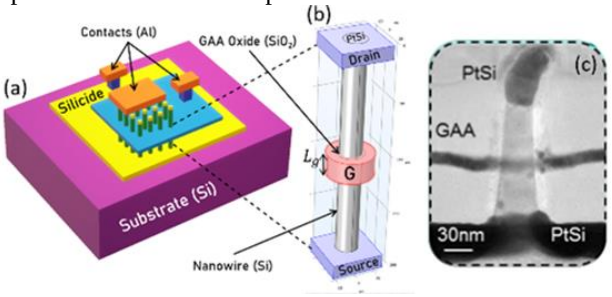

Figure. 1 Schematic representation of (a) Vertical array of GAA nanowires. (b) A single nanowire. (c) SEM image of a fabricated nanowire [3].

II. Electrothermal Modeling

The VNWFET compact model is developed based on a unified charge-based control model (UCCM) formulation for junctionless devices while accounting for short-channel effects (SCE), gate-induced drain leakage (GIDL), drain-induced barrier lowering (DIBL), as well as access resistors and Schottky contacts at the source and drain sides [5]. The compact model has been extensively validated against experimental data from the fabricated VNWFETs from LAAS [3] for a wide range of geometries at room temperature. The characteristics of the VNWFETs are strongly impacted by temperature variation, but unlike conventional transistors, the drain current shows a constant increase with increasing temperature. It is understood that in junctionless devices, carrier mobility is quite low due to the high channel doping [6]. Moreover, the variation of mobility

with temperature is also quite weak due to a combination of phonon and impurity scattering [7] and can be thus considered negligible from the electrothermal modeling point of view. The steady increase in the current in junctionless devices is widely attributed to a shift in the threshold voltage [6] and with no significant mobility degradation to counter this effect, the device characteristics exhibit a contrasting temperature dependence with respect to classical FETs. Aided by the understanding of nanoscale thermal transport in VNWFETs through Multiphysics simulations, we analyzed DC temperature measurements to extract thermal parameters such as the temperature coefficients of physical parameters (threshold voltage etc.) and leveraged low-frequency S-parameter measurements [8] to extract the equivalent electrothermal network of the device (consisting of thermal resistance and capacitances) for model development considering (1) temperature dependence of relevant model parameters and (2) dynamic self-heating effect.

A. Temperature dependence of threshold voltage

From the experimental observations, it was evident that increasing the temperature leads to a monotonically increasing drain current (Fig. 2(a)) conforming to prior observations in junctionless transistors [6]. To understand the nanoscale heat-transport in the VNWFETs at different temperatures, we investigated them through multiphyiscs simulations using COMSOL [9]. The COMSOL simulations were performed based on the GKE formulation [10] by solving the non-Fourier heat equation and coupling thermal and electrical transport equations. Simulation results showed good agreement with experimental data (Fig. 2(a)). Next, the thermal conductivity between the source and drain of a single nanowire at different temperatures was extracted from the numerical model as shown in Fig. 2(b). The gate-all-around (GAA) architecture of the VNWFET with a SiO_2 layer wrapped around the silicon nanowires makes it challenging to dissipate heat from the device [11]. A significant increase in the device temperature, reflected by an equivalent reduction in the thermal conductivity on the drain side, could be observed that indicated hot-spot formation and subsequent self-heating, even though the temperature rapidly falls off beyond the peak towards the drain contact, which may explain an efficient heat-evacuation through the nanowire. In addition to these observations, expectedly COMSOL simulations indicated a weak mobility variation and a strong variation of the threshold voltage with temperature, affirming that compact model formulation needs to translate these effects in terms of the electrical parameters of the device.

Next, to extract the temperature coefficients for the compact model, we leveraged on-wafer DC I_D-V_G measurements (Fig. 3) performed in the 15 °C-100 °C range and extracted the threshold voltage of the VNWFETs as a function of the temperature which showed a linear dependence (Fig. 4). The g_m/I_D-V_G method [12] was used for this extraction over the commonly used transconductance method, which is more sensitive to V_D variation. The g_m/I_D-V_G method, on the other hand, is expected to provide more accurate results and is particularly more reliable for junctionless transistors than other methods that may introduce additional uncertainty in threshold voltage extraction at different temperatures.

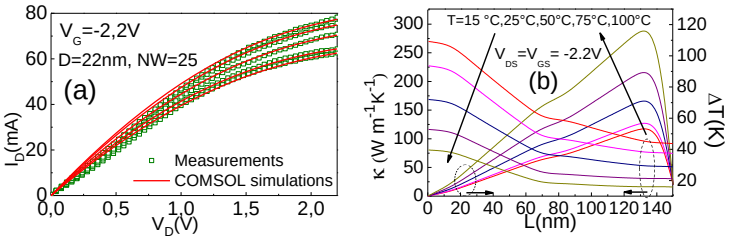

Fig. 2 (a) I_D-V_D of a p-type VNWFET comparing COMSOL simulations with DC temperature measurements. (b) Thermal conductivity and internal device temperature under different temperature condition.

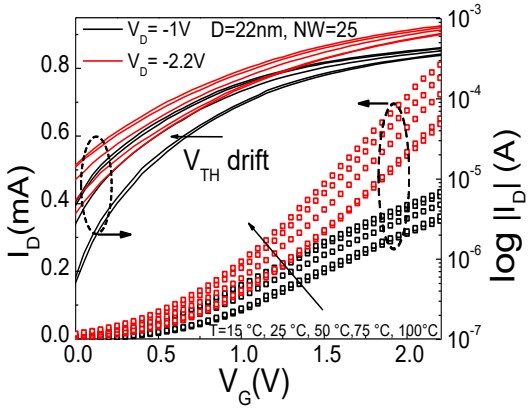

Fig. 3. I_D-V_G measurements at V_D= -1V and -2.2V at different temperatures.

From the linear dependence of threshold voltage on the measurement temperatures for different device geometries (different nanowires in parallel), an analytical model equation is obtained for the shift of threshold voltage:

$$\Delta V_{TH} = zetaVT \times (T_{dev} - T_{nom}) \qquad (1)$$

where $zetaVT$ is the slope of the curves in (Fig. 4), T_{dev} is the internal device temperature, which is different from the measurement temperature and T_{nom} is the nominal temperature, in this case 300K, the reference measurement temperature. This analytical equation of ΔV_{TH} is then embedded in the VNWFET compact model as an additional contribution to the threshold voltage expression.

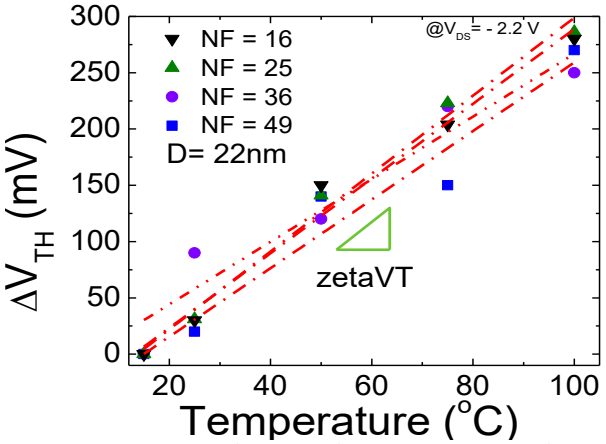

Fig. 4. Threshold voltage shift extracted from measurements as a function of temperature.

Additional to this, temperature-induced variation in both access resistances and Schottky barrier height (SBH) [13] of drain and source are considered to be linear with temperature. The temperature coefficients ($zetaR, zetaPhi$) for these parameters are then introduced in the compact model in a similar manner and are integrated into the existing analytical equations for source-drain resistances ($R_{S/D}$) and Schottky barrier heights ($PhiSB_{S/D}$) as follows:

$$\Delta R_{S/D} = zetaR \times (T_{dev} - T_{nom}) \quad (2)$$

$$\Delta PhiSB_{S/D} = zetaPhi \times (T_{dev} - T_{nom}) \quad (3)$$

These new model parameters ($zetaR, zetaPhi$) are then extracted from the compact model calibration against the DC measurement data for temperature-dependent drain current.

B. Self-heating effects

In addition to the drift of certain parameter values with temperature, the increase of internal device temperature during device operation is influenced by the self-heating phenomenon. Under dynamic operating conditions, device thermal impedance plays an important role in governing the device temperature and eventually the performances at device and circuit levels. To investigate the self-heating of the VNWFETs, the COMSOL multiphysics model [14] is further exploited to extract the thermal resistance from the heat flux and the device temperature rise observed under high bias conditions [15]. The thermal resistance (R_{TH}) can be simply represented by the following equation,

$$R_{TH} = \frac{\Delta T}{P_{ssi}} \quad (4)$$

Here, P_{ssi} is the dissipated electrical power in Watt, typically calculated by the product of drain voltage and current ($V_D \times I_D$), and ΔT is the increase of device temperature. Apart from DC conditions, dynamic self-heating can be modeled by considering the thermal impedance of the transistor. In [8], we extracted the thermal resistance (R_{TH}) and thermal capacitance (C_{TH}) of the VNWFET using low-frequency S-parameter measurements [15], which were then used to construct the equivalent RC filter-like circuit representing the electro-thermal network [16] to account for dynamic self-heating (Fig. 5). This required implementation of an additional fictitious node in the Verilog-A compact model that can be activated through a FLAG parameter when performing transient analysis of VNWFET logic circuits with electrothermal effects.

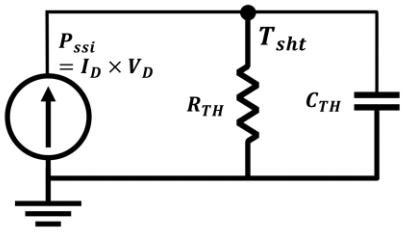

Fig. 5. RC filter-like electrical equivalent circuit for the implementation of self-heating effects.

Here, T_{sht} is the device temperature due to self-heating which is dynamically calculated from the voltage of the fictitious node (Fig. 5), through the following relation between its branch currents as implemented in the model,

$$Pssi = \frac{T_{sht}}{R_{TH}} + C_{TH}\frac{dT_{sht}}{d_t} \quad (5)$$

As indicated from Multiphysics simulations, the self-heating is more pronounced under higher temperature and bias conditions, which is why the extraction of thermal resistance and capacitances were performed at V_G, V_D = -2.2 V to reduce extraction errors. The T_{sht} contribution was then calculated directly using the extracted values of R_{TH} (validated using COMSOL) and C_{TH}. The new device temperature is thus represented by

$$T_{dev} = T_{amb} + T_{sht} \quad (6)$$

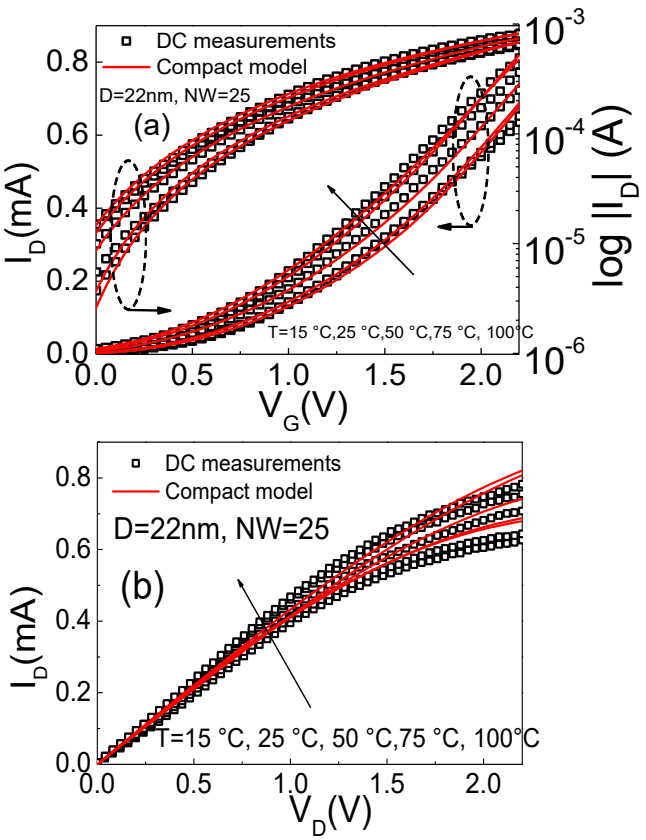

Fig. 6. (a) I_D-V_G and (b) I_D-V_D DC measurements at different temperatures compared with compact model simulations.

Finally, the modified compact model with the additional temperature-related and self-heating parameters was simulated under different measurement conditions (T_{amb}) which demonstrated good model accuracy, consistent with experimental results, as shown in Fig. 6.

III. Logic Circuit Simulations

Based on the improved VNWFET compact model and model parameter set calibrated against measurements, we investigated the influence of temperature variation on standard logic circuits composed of VNWFETs. Firstly, a classical CMOS inverter (inset of Fig. 7(a)) consisting of two VNWFETs, a p-type and an n-type, with the same geometrical characteristics, is studied. Fig. 7(a) a shows the static transfer curves of the inverter for different temperatures, whereas Fig 7(b) shows the input (V_{IN}) and output (V_{OUT}) transient waveforms. From the results it can be observed that the output shows a symmetrical behavior with respect to the input with a balanced switching transition roughly around $0.5V_{DD}$. Moreover, as temperature increases, we observed a degradation in the logic levels and an increase in the delay time. This can be explained by the drift of threshold voltage caused by electrothermal effects, with which the off-state current (I_{OFF}) increases significantly and the increase in the on current (I_{ON}) is not sufficient to compensate for the effect of the temperature-induced degradation in the I_{ON}/I_{OFF} ratio, which in turn affects the switching characteristics of the logic cell.

In more complex circuits, such as the XOR logic circuit consisting of eight VNWFETs (along with four additional transistors for the inverters) as shown in Fig. 8(a), the influence of electrothermal effects are visibly more

pronounced. The logic cell output in Fig. 8(b) indicates a classical XOR operation, but the output logic level degradation becomes more significant at higher temperatures.

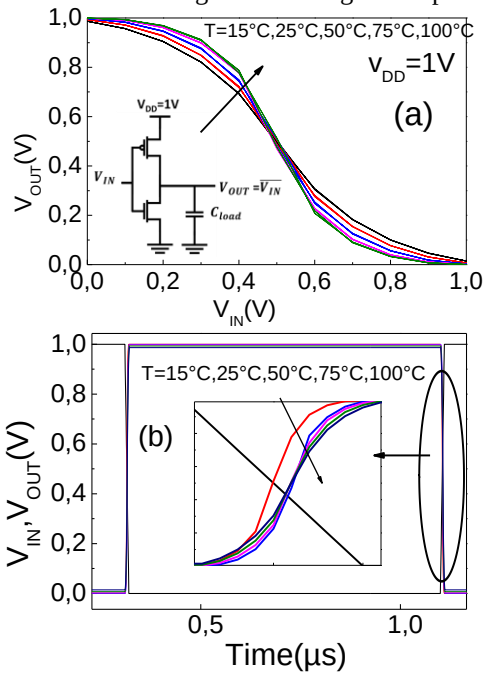

Fig. 7 (a) Inverter logic circuit (inset) and transfer characteristics, (b) input (V_{IN}) and output (V_{OUT}) transient waveforms at different temperatures.

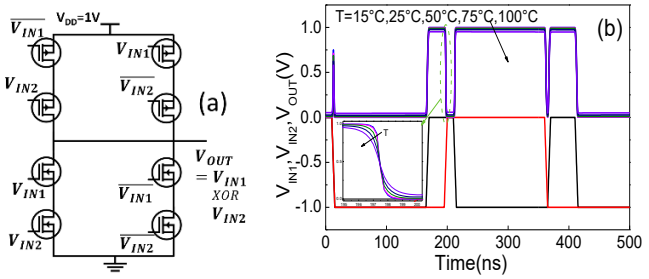

Fig. 8. (a) XOR logic circuit, (b) inputs (V_{IN1}, V_{IN2}) and output (V_{OUT}) transient waveforms; inset: Output degradation with temperature.

IV. Conclusion

In this work, we present, for the first time, a comprehensive physics-based compact modeling of electrothermal effects in vertical GAA junctionless nanowire transistors VNWFET. The compact model accounts for underlying electrothermal phenomena aided by in-depth analysis of experimental data and understanding of nano-scale heat transport studied through Multiphysics simulation. The developed model is validated against experimental results showing good agreement between simulation and measurements results at different temperature conditions for different VNWFET geometries. The calibrated compact model is then used for studying standard logic circuits that indicate performance degradation at high temperatures, mainly in terms of delay and a reduction of the output voltage swing, especially for complex logic circuits. As available on/off current ratio continues to decrease at higher temperatures, maintaining circuit functionality and meaningful performance can become critical with the current state of the technology. Hence special attention should be given when designing complex logic circuits using this technology generation and providing feedback to the fabrication process engineers through DTCO loop remains a crucial aspect in the value chain of 3D VNWFET-based 3D computational neuromorphic hardware design.

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