Re-using Chip Level DFT at Board Level

Gu, Xinli; Rearick, Jeff; Eklow, Bill; Qian, Jun; Jutman, Artur; Chakrabarty, Krishnendu; Larsson, Erik

Re-using Chip Level DFT at Board Level

Xinli Gu[1], Jeff Rearick[2], Bill Eklow[3], Martin Keim[4], Jun Qian[2], Artur Jutman[5], Krishnendu Chakrabarty[6], Erik Larsson[7]
[1] Huawei, [2] AMD, [3] Cisco, [4] Mentor Graphics, [5] Testonica, [6] Duke University, [7] Lund University

Abstract—As chips are getting increasingly complex, there is no surprise to find more and more built-in DFX. This built-in DFT is obviously beneficial for chip/silicon DFX engineers; however, board/system level DFX engineers often have limited access to the build in DFX features. There is currently an increasing demand from board/system level DFX engineers to reuse chip/silicon DFX at board/system level. This special session will discuss: What chip access is needed for board-level for test and diagnosis? How to accomplish the access? Will IEEE P1687 and IEEE 1149.1 solve these problems?

Keywords-Board test, board diagnosis, chip access, IEEE P1687, IEEE 1149.1

The statements from board-level, EDA tool vendor, and chip-level panelists are collected below:

I. BOARD-LEVEL

A. Jeff Rearick

On-chip instrumentation is becoming pervasive, and the access to those instruments is becoming available to downstream users via soon-to-be-balloted standards like IEEE P1687 and the latest update to IEEE 1149.1. There are several use models for these standards which add distinct value to the board and system test community, including validation of intra-chip functionality, performance testing of inter-chip connectivity, and debug of system operation, all of which we can expect to be supported by vendor tools in the near future.

B. Bill Eklow

More Moore and More than Moore technology scaling means one thing for board and system level functional test: unmanageable complexity. Already functional specs are reaching thousands of pages for a single component. There is significant concern that component yields will decrease as technology scales. It could easily be inferred that test escapes to the CM could grow proportionately to shrinking yields. What we end up with is more problems that are more difficult to find on the board or in the system. While "localizing" failures to the correct component is becoming increasingly difficult, isolating to the defect (in system) will be nearly impossible. Yet, this critical information is exactly what is needed by the component supplier to prevent shipping more defective parts. We need disruptive methods to solve this problem before it becomes Moore than we can handle.

II. EDA TOOL VENDOR

A. Martin Keim

Engineers could always make system and board level test of embedded IP work, independently how deep the IP was in the die. BIST is one preferred way enabling system level test of an embedded IP; IEEE 1149.1 or one or another type of a bus interface are access mechanisms. To make this access and operation of the IP somewhat more robust and safe to use, many companies defined preferred methodologies together with their IP providers, developed in-house solutions and proprietary tools. Some solutions are very sophisticated, other are more ad-hoc, some provide debug access, for others this is very difficult. Common to all is that these are isolated, stand-alone solutions between a few partners. The emerging standard of IEEE P1687 provides a way out of these myriad of distinct techniques of solving the same problem. We will show how one standard can achieve this, and at the same time is an attractive standard for an EDA provider to support.

III. CHIP-LEVEL

A. Jun Qian

Many DFX test features aimed for board/system level test and debug are built in complex SOC. Those features are proven to be very useful and beneficial at board/system level. However, pre-silicon validation are very challenging and nowhere to be complete; post-silicon usage requires time and effort consuming bring up process. Establishment of standards and common practices and tools will help a great deal.

IV. CONTACT DETAILS

Contact details to the panelists:
Jeff Rearick, AMD, USA, email: Jeff.Rearick@amd.com
Bill Eklow, Cisco, USA, email: beklow@cisco.com
Martin Keim, Mentor Graphics, USA, email: Martin_Keim@mentorg.com
Jun Qian, AMD, USA email: Jun.Qian@amd.com
Contact details to the moderator:
Artur Jutman, Testonica, Estonia,
email: artur@testonica.com
Contact details to the panel organizers:
Xinli Gu, Huawei, USA, email: Xinli.Gu@huawei.com
Krishnendu Chakrabarty, Duke University, USA, email: krish@ee.duke.edu
Erik Larsson, Lund University, Sweden, email: erik.larsson@eit.lth.se

IEEE computer society