

# New Scan-Based Test Strategy for a Dependable Many-Core Processor Using a NoC as a Test Access Mechanism

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Recent advances in the semiconductor industry enable the integration of many processing units on a single die and new processors are often included into large many-core SoCs. The dependability of such a many-core processor is essential for many mission-critical applications. Ideas such as the Know-Good-Tile concept [1] or majority-voting among tiles [2] have been proposed to explore the possibility to enhance the dependability of a many-core processor.

Given a many-core processor with many identical processing cores (tiles), the same test responses are expected from identical fault-free tiles when one applies the same test stimuli to each of these tiles. Assuming that only one tile becomes faulty at a time, one is able to identify this faulty tile by comparing its test responses with the responses of other fault-free tiles. Previous researches have shown the design of an infrastructural IP (IIP) [3]-[4] within the many-core processor to perform a periodic structural scan-based test on the idle ones of an array of Xentium tile processors (from Recore Systems [5]).

This work presents the unaddressed link between the IIP and the processing tiles under test: the Test Access Mechanism (TAM). Network-on-chip (NoC) has been proven to be an efficient and flexible on-chip communication method for SoCs. It is possible to reuse the NoC as a TAM to test the few idle tiles in the many-core processor while leaving other tiles carry on with their normal task. This can be considered as a hybrid form of on-line and off-line test.

Obviously, the overall NoC bandwidth will have to be shared between the normal applications running on the many-core processor and the testing task. It is preferred to give the normal applications precedence over the testing task when the NoC bandwidth is allocated. This means the IIP should be able to adapt to the very flexible NoC bandwidth availability or even to suspend the testing when too little or no bandwidth is available.

Performing scan-based test using the NoC may not be as

straight-forward as it appears. As a packet-switched NoC is used, the test stimuli and responses are transported over the NoC in the form of 32-bit “data flits”. The loading of primary input stimuli does not necessarily take the same number of clock cycles as the unloading of the primary output results. Global timing constraints are necessary to match the “loading test stimuli” and “unloading test results” operations. Meeting these constraints becomes even more difficult considering the fluctuating availability of NoC bandwidth. Therefore, it has been decided that the test stimuli application and test response collection processes will be decoupled to simplify the top-level control of the scan-based test.

Additionally, it is required to be able to pause and resume the scan-based test depending on the amount of NoC traffic. This can be achieved by adding a pause/resume function to the test stimuli generator and test response evaluator in the IIP. This is particularly useful if one needs to match the test responses from multiple tiles which do not always arrive at the IIP at the same pace.

A special wrapper IP has also been designed for the Xentium tiles. This wrapper can switch among “Functional”, “Manufacture Test” and “Dependability Test” modes to ensure the incoming data arriving at the correct data port of the processing tile. Silicon of the system is expected in 2010.

## REFERENCES

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