Analysis of Resistive-Bridging Defects in SRAM Core-Cells: a Comparative Study from 90nm down to 40nm Technology Nodes

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Analysis of Resistive-Bridging Defects in SRAM Core-Cells: a Comparative Study from 90nm down to 40nm Technology Nodes*

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***Abstract*—In this paper, we present a comparative study on the effects of resistive-bridging defects in the SRAM core-cells, considering different technology nodes. In particular, we analyze industrial designs of SRAM core-cell at the following technology nodes: 90nm, 65nm and 40nm. We have performed an extensive number of simulations, varying the resistive value of defects, the power supply voltage, the memory size and the temperature. Experimental results show malfunctions not only within the defective core-cell, but also in other core-cells (defect-free) of the memory array.**

***Keywords*—SRAM, core-cell, resistive-bridge, fault modeling.**

I. INTRODUCTION

Nowadays, embedded memories are made with the fastest technologies and are among the most important components in complex systems. The major trend of System-on-a-Chip (SoC) design allows to embed in a single chip all components and functions that historically were placed on a hardware board. Within SoCs, embedded memories are the densest components, accounting for up to 90% of the chip area [1]. Thus, it is common to find on a single chip several memories of different types, sizes, access protocol and timing. The high density of SRAM core-cells makes them extremely vulnerable to physical defects. Due to the complex nature of the SRAM internal behavior, the generation of fault models and efficient tests is a non-trivial task.

In order to minimize the test development effort and produce more efficient and dedicated memory tests, we can rely on information provided by electrical analysis. In this context, the analysis of the memory layout allows to determine realistic defect sites within memory elements and, in particular, the core-cell. Then, electrical simulations of defects allow determining those that may lead to a faulty behavior of the SRAM. The next step is the modeling of the faulty behavior of the memory and the generation of effective test algorithms.

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Most of the work proposed so far and using the above approach is dedicated to the test of resistive-open defects [2][3][4]. More recently, the study of parasitic capacitances within a memory core-cell was also considered during test development [5]. All these studies determine a sub-set of fault models and lead to very effective test solutions in terms of test time.

The work presented in [6] analyzes the impact of resistive-bridging defects but only between (not inside) memory core-cells. In [7], resistive-bridging defects are injected in an industrial SRAM designed with a 250nm technology. In this paper, we present a study on the effects of resistive-bridging defects injected in industrial SRAM designs of three different recent technology nodes: 90nm, 65nm and 40nm. The position of the resistive-bridges has been chosen taking into account the actual industrial core-cell layout. Each defect has been explored in a wide range of resistance values and different conditions of supply voltage, memory size and temperature.

The main results presented in this paper are that simulated defects do not only show malfunctions within the defective core-cell (*i.e.* the core-cell where we actually inject the defect), but they also influence the behavior of other (defect free) core-cells in the memory array.

The paper is structured as follows. Section 2 details the experimental conditions used to perform simulations. Section 3 summarized the experimental results. Section 4 provides detailed analysis of some relevant case studies, while Section 5 summarizes the main contribution of this paper.

II. EXPERIMENTAL SETUP

In this section, we present experimental conditions for SPICE simulations that allow revealing faulty behaviors of SRAMs induced by resistive-bridging defects. We assume the presence of only one defect for each analysis, as the occurrence of multiple defects has a low probability to occur.

As shown in Figure 1, five resistive-bridging defects (Df1 to Df5) have been placed in different locations of the core-cell. As mentioned in the introduction, these defect locations have been extracted from the layout view of an industrial core-cell, by looking at adjacent lines of the same metal layer or between metal layers. Note that, we do not

consider all possible locations because of the symmetry of the core-cell structure. In particular, Df2 to Df5 have symmetrical resistive-bridges. Df1 is a defect between the internal nodes (*S* and *SB*) of the core-cell and has no possible symmetrical defect.

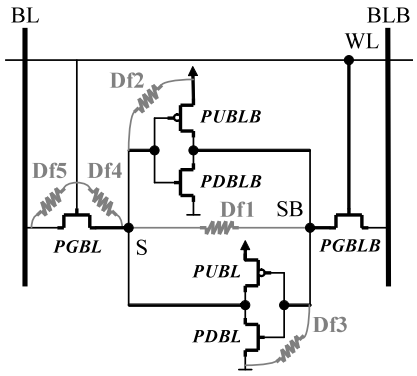

Figure 1: Resistive-bridging defects in the SRAM core-cell

The five resistive-bridging defects that we consider can be classified into two groups:

- *Group_1:* This group includes defects that may affect the behavior of the core-cell when read and/or write operations are performed on it. According to the taxonomy presented in [8], Group_1 defects involve single-cell faulty behaviors. Group_1 includes Df1, Df2 and Df3, as these defects may impact electric nodes within the core-cell only.
- *Group_2:* This group includes defects affecting the behavior of the defective core-cell and of other non-defective core-cells of the array. According to the taxonomy presented in [8], defects in Group_2 may involve double-cell faulty behaviors. Group_2 includes Df4 and Df5 as these defects may impact BL and WL nodes

The considered simulation scheme includes the whole SRAM array and not only the single defective core-cell. It is shown in Figure 2. In order to speed-up simulations, most of core-cells are replaced by current sources, thus modeling leakage effects.

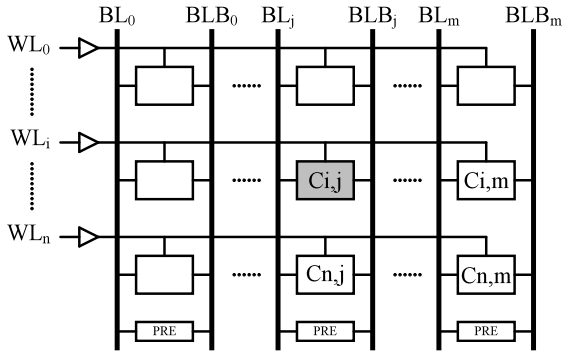

Figure 2: Simulation model of the core-cell array

This memory array is composed of n×m core-cells (n rows and m columns) and Ci,j is the defective core-cell (*i.e.* the core-cell affected by one of the resistive-bridging defects). For the analysis of defects in Group_1, only Ci,j is accessed for read/write operations. Otherwise, defects in Group_2 are studied by applying read/write operations on other core-cells of the array:

- on Ci,m that shares the same word line than Ci,j.
- on Cn,j that shares the same bit line than Ci,j.
- on Cn,m that does not share the same word line and bit line than Ci,j.

Using this simulation scheme, the whole operating environment range has been examined with the aim of determining test conditions that maximize the probability of malfunction and the fault detection. Hence, simulations have been performed on the three technology nodes by applying an exhaustive number of test patterns and by varying the following parameters: power supply voltage, memory size and temperature.

For each technology node, we considered low, nominal and high voltages. The values of the applied voltages are listed in Table I.

TABLE I. POWER SUPPLY VOLTAGE VALUES

	Low	Nominal	High
90nm	1.0	1.1	1.2
65nm	0.9	1.0	1.1
40nm	0.8	0.9	1.0

We also considered low, nominal and high values for the temperature. They are: -40°C, 25°C, 125°C.

The memory size is relative to each technology node, as more advanced technologies allow more core-cells in a column. In Table II, we list the number of core-cells per column, also known as memory height.

TABLE II. NUMBER OF CORE-CELLS PER COLUMN

	Low	Nominal	High
90nm	128	512	1024
65nm	2048	4096	8192
40nm	4096	8192	16384

We considered defect values in a range from 0Ω up to several MΩ. A summary of electrical simulations is provided in the next section.

III. SIMULATION RESULTS

Table III presents a summary of fault models identified for each injected resistive-bridging defect. Worst-case conditions were defined to maximize the resistance range in which the corresponding fault occurs. The worst-case conditions for each fault are described in Table IV.

In Table III, the first column gives the defect location. The second column presents resulting fault models. Remaining columns report the maximum defect value (in kohm) that implies the observation of the fault model for each technology node. Thus, the corresponding range of defect values in which failure occurs is from zero up to the value presented in Table III.

The definitions of fault models reported in Table III are the following:

- *Stuck-at Fault* (SAF) [2]: A core-cell is said to have a SAF when it stores always the same value. It is called SAF0 when the value is always '0' and SAF1 when the value is always '1'.
- *Transition Fault* (TF) [2]: A core-cell is said to have a TF if it fails to produce a transition ($0 \rightarrow 1$ or $1 \rightarrow 0$) when it is written.
- *No Store Fault* (NSF): A core-cell is said to have a NSF if it is not able to retain any logic information in their nodes S and SB.
- *Weak Read Fault* (WRF): A core-cell is said to have a WRF when, during the access for the read operation, the voltage difference between BL and BLB (ΔBL) is lower to the safety limit (about 10% of VDD) that allows the sense amplifier to produce the correct logic output.
- *Read Destructive Fault* (RDF) [10]: A core-cell is said to have a RDF if a read operation performed on this core-cell changes its content and returns an incorrect value on the output.
- *Incorrect Read Fault* (IRF) [2]: A core-cell is said to have an IRF if a read operation performed on the core-cell returns an incorrect logic value, although the correct value is still stored in the core-cell.
- *Disturb Coupling Fault* (CFds) [8]: Two core-cells are said to have a CFds if an operation (write or read) performed on the aggressor forces the victim into a given logic state.

TABLE III. MAXIMUM DEFECT VALUE THAT INDUCES FAILURE IN EACH TECNOLOGY NODE

Dfi	Fault Model		Defect values (kohms)		
			40nm	65nm	90 nm
Df1	NSF		611.2	379	27
	RDF		1210	413	27
	WR		2010	1180	45
Df2	SAF1		82	47	7.6
	RDF		110	33	8.2
	WRF		582	96	12.1
Df3	SAF0		160	137	22
	RDF		612	415	31
	WRF		1248	1290	67
Df4	SAF0		156	120	24
	IRF		54	21	10.4
	WRF		582	96	12
Df5	C(i,j)	TF	2.52	0.82	0.31
		IRF	2.52	0.82	0.31
		WRF	21	9	1.5
	Array	RDF alter	77	44	16.7
		CFds*	1.34	1.07	1.04
		WRF alter	1020	255	39
		IRF alter	150	56	13.7

Note that the '*' symbol indicates that the aggressor and victim core-cells share the same word line. The term 'alter' in the fault modeling related to Df5 (RDF alter, IRF alter and WRF alter) indicates that the core-cell in which the faulty behavior is observed is not the defective core-cell.

From Table III, we observe that more advanced technologies are more susceptible to fail due to resistive-bridging defects, because higher values of resistances are sufficient to lead to a faulty behavior.

TABLE IV. CONDITIONS USED TO SIMULATE EACH FAULT

Dfi	Fault Model		Temp.	VDD	Memory height
Df1	NSF		low	low	-
	RDF		low	low	high
	WRF		low	low	high
Df2	SAF1		low	low	-
	RDF		low	low	-
	WRF		low	low	high
Df3	SAF0		low	low	-
	RDF		low	low	-
	WRF		low	low	high
Df4	SAF0		nominal	low	-
	IRF		nominal	low	low
	WRF		low	low	high
Df5	C(i,j)	TF	low	low	-
		IRF	low	low	-
		WRF	low	low	-
	Array	RDF alter	high	low	low
		CFds*	high	low	-
		WRF alter	low	low	high
		IRF alter	low	low	low

Defect values in Table III were extracted from worst-case conditions simulations. Conditions that maximize the defect value are described in Table IV. In order to make a fair comparison between different technology nodes, we do not change the conditions between the technology nodes for the same fault model and defect. In Table IV, the worst case conditions listed are the worst case conditions for the technology node 40nm.

Table IV shows that a low supply voltage maximizes the defect value that induces failure for every fault model. For some fault models, the memory height has none or very little influence. It is surprising that, in some cases, the temperature that maximizes the failure range is 25°C. It suggests that the simulation method of corner analysis may fail to capture the worst-case conditions when analyzing this technology node.

For test and diagnosis developments, Table III indicates the predominance of WRF. In order to detect WRFs, the sense amplifier should be stressed by reading alternately '0' and '1' logic values.

In Table V, we show conditions that maximize the failure range in each technology node. For each defect, we selected the condition that induces the highest defect resistance range that causes a failure among the concerned fault models.

Table V shows that, in technology nodes 40nm and 65nm, conditions that maximizes the failure occurrence, if a

defect is present, is low temperature, low supply voltage and high memory height.

TABLE V. WORST CASE COMPARISON BETWEEN TECHNOLOGY NODES

Dfi	Parameter	40nm	65nm	90 nm
Df1	Temp.	low	low	low
	VDD	low	low	low
	M. Height	high	high	high
Df2	Temp.	low	low	low
	VDD	low	low	high
	M. Height	high	high	high
Df3	Temp.	low	low	low
	VDD	low	low	high
	M. Height	high	high	high
Df4	Temp.	low	low	high
	VDD	low	low	low
	M. Height	high	high	high
Df5	Temp.	low	low	high
	VDD	low	low	low
	M. Height	high	high	high

The technology node 90nm presents a different behavior with respect to technology nodes 40nm and 65nm. Moreover, it presents different worst case conditions for different defects. This may be explained by the fact that more than one fault model can be the worst case for each defect in 90nm. Whereas, in 40nm and 65nm, the fault model WRF always has the greatest defect resistance range. Thus, the worst case for the fault model WRF is always the same.

In 90nm, different fault models may appear with the same defect resistance range. Thus, one fault model or another becomes the dominant depending on environmental conditions.

IV. SOME CASE STUDIES

In this section, we analyze in detail two resistive-bridging defects (Df1 and Df5). Defect Df1 causes failure only in the defective core-cell, whereas defect Df5 has an impact on the array functioning.

A. Impact of Df1 on the core-cell functioning

When analyzing the symmetric defect Df1, we observe hat the determinism of electrical simulations may hide some faults. For example, in order to find the range of defect values in which RDF occurs, we performed a read operation in transient simulations varying the defect value of Df1. Figure 3 shows voltage levels at the internal S and SB nodes.

The arrows indicate the resistive values of the defect. Thus the external curves (indicated by the number ①) correspond to very high defect values that tend to an open-circuit, denoting a non-defective core-cell.

In the following, we observe two couples of curves (indicated by the number ②), which indicate that the core-cell nodes are initially in different states. At time 5ns, when the read operation starts, the voltages of nodes S and SB become equals. After the end of the read operation, the voltage values at these nodes remain at the same value, characterizing a lost of information. It is not a usual RDF, because the core-cell does not store any value. The core-cell is set in a third state, which corresponds neither to '1' nor to'0'. Thus, the next read operation made on this core-cell would return a random value. In electrical simulations, if we only observe the output of the sense amplifier, this fact may not be noticed.

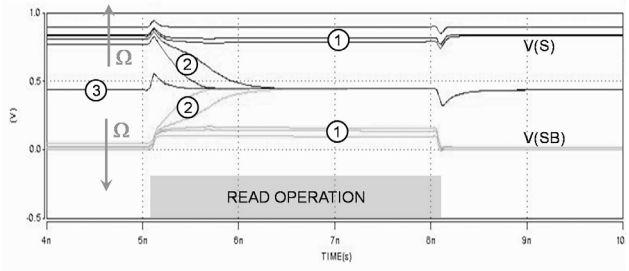

Figure 3: Voltages at nodes S and SB during a read operation, considering several defect values.

A third behaviour is observed for very low defect values, which is observed in middle curves (indicated by number ③ in Figure 3). The core-cell is not able to store any value even before a read operation, which corresponds to a NSF fault.

In order to have a better insight of the impact of Df1 on the core-cell functioning, we analyzed the well-known butterfly plot, used to compute the Static Noise Margin (SNM). In butterfly plots, we can observe the three behaviours described above. Butterfly plots are DC analysis of S and SB nodes. In each plot, one curve is the voltage measured at SB in function of the voltage applied at S and the other curve is the voltage measured at S in function of the voltage applied at SB. The points where one curve cross the other one are stable or meta-stable points. Butterfly plots can be made in retention mode, with the WL voltage equal to zero, or in read mode, with the WL voltage equals to VDD. The retention mode plot gives origin to the SNM [11] measure, while the read mode plot gives origin to the Read Noise Margin (RNM) [11].

Figure 4 shows butterfly plots of a non-defective core-cell in read and retention modes. The diagonal of the inserted squares correspond to SNM and RNM of this core-cell.

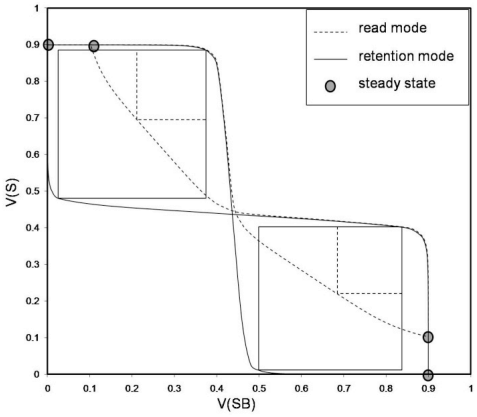

Figure 4: Butterfly plot of a non-defective core-cell in retention mode and in read mode

We observe that stable points are different in read and retention mode. Nevertheless, in both modes we clearly see that two distinct stable states exist. There is a meta-stable point in each point. If S and SB nodes are somehow brought to this point, they will soon diverge towards one stable point or another. Finally, we observe that the RNM is smaller than the SNM.

When we inject defect Df1, butterfly plots of the core-cell are altered. Figure 5 shows the butterfly plot of a core-cell affected by defect Df1 of 850kΩ. For this resistance value, no failure was observed in transient simulations.

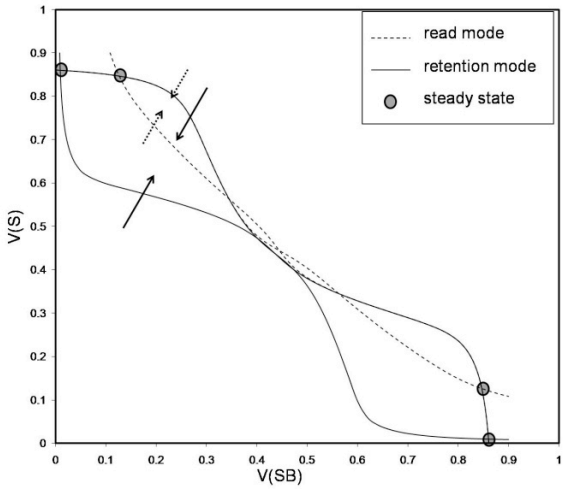

Figure 5: Butterfly plot of a core-cell in retention mode and read mode with Df1 = 850KΩ

Comparing curves in Figure 5 with those in Figure 4, we observe the reduction of SNM and RNM, but the steady states are still visible in retention mode and in read mode. This means that the core-cell is still able to retain data and, when selected for read operation, it still keeps its data.

As we decrease the resistive value of the defect, the butterfly plots lose their original form. For a resistive bridge of 400kΩ, we obtain the curves shown in Figure 6.

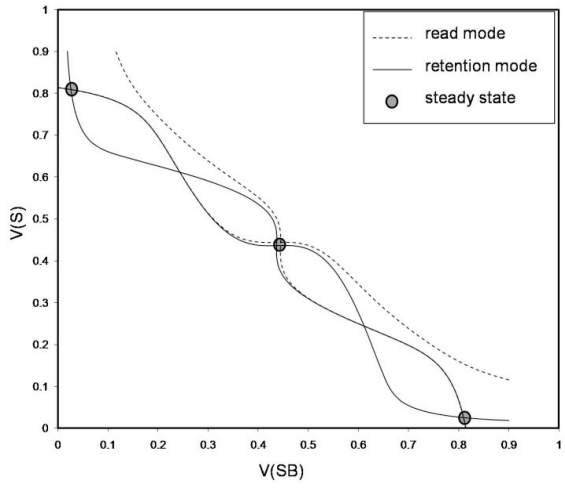

Figure 6: Butterfly plot of a core-cell in retention mode and read mode with Df1 = 400KΩ

Firstly, we observe in Figure 6 that, in read mode, there is only one stable point. Consequently, the core-cell does not preserve its value during a read operation, indicating read destructive fault. Secondly, we observe that the retention mode presents five crossing points. From these five points, we verified that three are stable points.

Figure 6 corresponds exactly to the second behaviour identified in Figure 3. In this case, the core-cell initially stores a given value using two different voltage values for S and SB nodes. During a read operation, both nodes converge to the same voltage value. After the end of the read operation, when the core-cell enters in retention mode, both nodes are in the middle stable point, as shown in Figure 6.

Finally, we observe the third behaviour identified in Figure 3, in which the core-cell present NSF. For a defect value of 150kΩ, the core-cell has the same steady state in read mode and in retention mode, as shown in Figure 7.

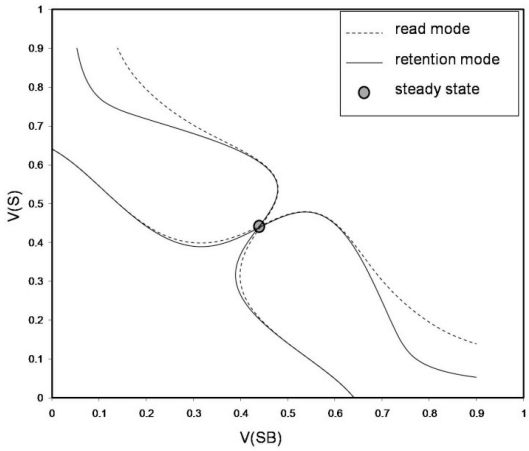

Figure 7: Butterfly plot of a core-cell in retention mode and read mode, with Df1 =150KΩ injected.

Effects observed in transient simulations were confirmed by the analysis of butterfly plots. An interesting behaviour was highlighted in Figure 6, where the butterfly plot indicates three stable points in a core-cell affected by defect Df1.

B. Impact of Df5 on the array functioning

We have seen in Section III that Df5 may cause faults in the defective core-cell and also in the neighbour core-cells. In this subsection, we analyze what kind of fault models Df5 causes in the memory array. Firstly, we analyze the WRF/IRF that occurs in the defective core-cell Ci,j. Then, we analyze faults that Df5 causes on core-cells of the same column. Finally, we analyze the case of CFds.

The first case is illustrated in Figure 8. The voltage difference between BL and BLB, known as ΔBL, is plotted for different defect values of Df5. The defective core-cell Ci,j initially stores a logic '0' and is accessed for a read operation. During the read access, a non-defective core-cell produces a negative ΔBL, like the curve indicated by number ① in Figure 8. Conversely, for low values of resistance (see number ③ in Figure 8), word line WLi that is selected (WLi at VDD) pulls-up bit line BL. The read operation in Ci,j

returns a logic '1' instead of a logic '0'. At the end of the read operation, the word line is turned off (passes to 0), driving BL, and consequently ΔBL, down. Moreover, for many defect values of Df5 (number ② in Figure 8), there is a weak read and the core-cell may return a random value.

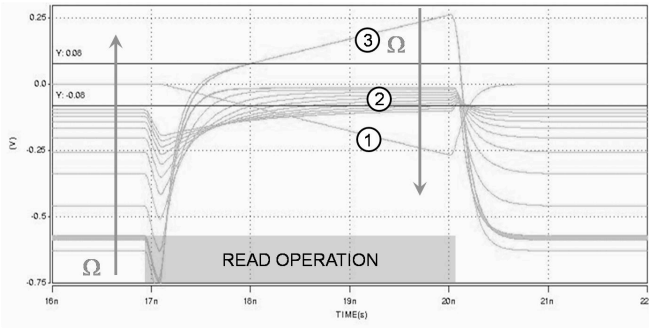

Figure 8: ΔBL at r0 access of defective core-cell with Df5

Figure 9 shows the occurrence of WR/IRF in a non-defective core-cell Cn,j placed in the same column than the defective core-cell Ci,j. When core-cell Cn,j, storing a logic '1', is accessed for reading, ΔBL is positive if Ci,j is non-defective (number ① in Figure 9). Conversely, for low defect values of Df5 (number ③ in Figure 9), the word line WLi (at a logic '0', because it is not selected), drives bit line BL to a logic '0'. The read operation in Cn,j returns a logic '0' instead of a logic '1'. Besides, for many defect values of Df5 (number ② in Figure 9), there is a weak read and the non-defective core-cell Cn,j may return a random value.

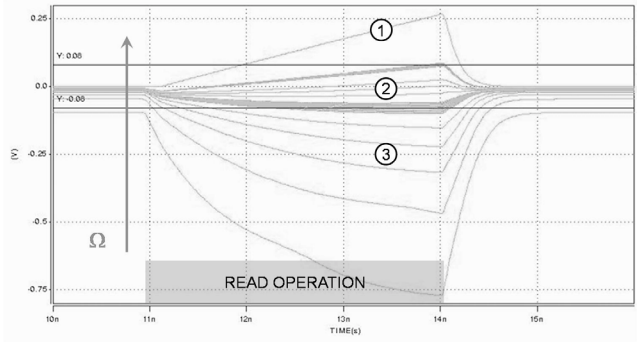

Figure 9: ΔBL at r1 access of non-defective core-cell with defective cell in the same column with Df5.

Finally, the CFds appears when an operation is applied on the core-cell Cn,m (see Figure 2), activating the word line WLn. This operation disturbs a core-cell that is in the column of the defective core-cell and in the row of the accessed core-cell. Since the bit line of the victim is connected to the word line of the defective core-cell, this bit line is pulled down. This may cause the loss of the data stored in the core-cell Cn,j, if the voltage at the bit line of defective core-cell is low enough.

In summary, defect Df5 causes many failures in the column of the defective core-cell and this will be easily detected using known March tests. If a repair strategy is applied, the whole column of the defective core-cell (with Df5) must be replaced with a spare column. Moreover, the word line in which Df5 occurs should also be replaced, because it is connected to a bit line through a defective resistance. This may lead to non-catastrophic faults in this word line since the word line driver was not conceived to drive this extra capacitance.

V. CONCLUSIONS

In this paper, we made a comparative study on effects of resistive-bridging defects in SRAM core-cells in different technology nodes. We identified that the core-cell is more sensible to resistive-bridging in more advanced technologies. Although the resistive-bridges are placed inside the core-cell, we have found an impact on other defect-free core-cells of the memory array. Moreover, it is interesting to note that we have diagnosed coupling faults CFds*, with aggressor and victim core-cells that are both different form the defective core-cell.

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