Towards Power Efficient 6G Sub-THz Transmission

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***Abstract*—Extreme high rate demands for 6G can be addressed by communication technologies in the millimeter wave and Terahertz bands. In these high carrier frequencies, power consumption can become a key limiting factor and thus has to be assessed thoroughly. This paper considers the power consumption of the RF frontend of a transceiver for the use in a hot spot scenario. A power consumption model for the main functional blocks has been derived for different frequencies and array architectures, both at transmit and receive side. The impact of the EIRP reduction over the frequency range from 90 GHz up to 230 GHz due to increased path loss and reduced output power of the power amplifiers has been assessed and the related power consumption has been evaluated. Further, the impact of analog-to-digital converters on the overall power consumption of the receive part have been carved out. Key dominating components have been identified indicating the number of antenna elements needed for different architectures and the related power consumption.**

Keywords—power consumption, sub-THz devices, power efficiency, spectral efficiency, waveforms, antenna array, ADC resolution, PAPR, achievable data rate

I. INTRODUCTION

Five generations of celluar systems are already deployed. There are numerous visions how the sixth generation (6G) should look like [1][2][3]. The demand for increasing data rates is ever-growing and thus addressing it with technologies for supporting new spectrum in the upper millimeter wave (mmW) and Terahertz (THz) bands is a clear direction to be considered for 6G. Driver for extreme high-rate services can be e.g. multi-modal mixed reality telepresence or mixed reality co-design. Furthermore, the large bandwidths available at high carrier frequencies also provide a good basis for sensing technologies, being embedded into the communication system.

The design of new communication systems envisaged for 6G in the sub-THz range (100–300 GHz) provide additional challenges on the physical layer (PHY). The higher path loss in the frequency bands above 100 GHz and the targeted higher bandwidths up to several tens of GHz lead to increased transmit power requirements, measured as equivalent isotropic radiated power (EIRP). While a larger number of antenna elements can compensate that to a certain extent by exploiting the beam gain, there are physical limitations e.g. on the power amplifier (PA) devices. The PA efficiency and the achievable output power level are technologically limited and decrease with increasing carrier frequency. Increasing the number of RF chains, which contain one PA each, will in combination with the reduced PA efficiency, significantly increase the power consumption of the transmitter. A further important point is the impact of the selected waveform to be transmitted. OFDM signals as standardized in current 5G NR [14] have a high peak-to-average power ratio (PAPR). The PAs are selected to transmit the maximum output power level meeting the linearity requirements. This means that the average power to be transmitted is reduced by the PAPR, which further decreases the power efficiency [15].

On the receive side, the analog-to-digital converter (ADC) is considered as the most power consuming part. Its power consumption increases with the resolution in number of bits and with the sampling rate. Further, the baseband processing of the signals with the targeted high bandwidth must be capable to handle the higher data rates associated with the high sampling rates. All these impacts make it a challenge to provide sub-THz communication systems with reasonably low power consumption and even improved energy efficiency compared to legacy 4G and 5G systems.

Various system architectures characterized by different antenna array configurations, numbers of transmit and receive chains for spatial multiplexing with multiple-input-multiple-output (MIMO) schemes, and different transmit power classes reflecting the various services and deployment scenarios can be considered. Performance requirements need to be addressed by proper selection of channel coding, waveforms, ADC resolution and user multiplexing. So the overall power consumption depends on the number and design of many different functional blocks, as well as on the requirements of the use case. The various architecture options make it difficult to identify the most dominating contributors to the overall power consumption, and to find suitable strategies to keep power consumption low and energy efficiency high.

Therefore this paper intends to investigate and review different system architectures with respect to power consumption for the expected upcoming use cases under the related physical and technological constraints of 6G systems operating in the sub-THz band. In [4] a similar analysis has been provided for frequency bands up to 60 GHz. There the spectral efficiency of different architectures and ADC resolutions has been compared to the related energy efficiency, but with focus on the pico- and macro-cellular use cases envisaged for the 5G NR FR2 frequency band. This paper attempts to analyze power consumption based on a model derived for the functional blocks of a fully integrated system operating in the 90 GHz band [5], covering all important system components and allowing parametrization according to the different expected upcoming new use cases and architectural approaches up to 230 GHz.

The paper is organized as follows: Section II will explain the exemplary use case and derive the most important requirements, Section III introduces the power consumption model covering various system architectures, and revisits the power consumption data of PA, ADC, low noise amplifiers (LNA) and other considered devices. In Section IV the detailed power consumption analysis and energy efficiency of different architectures and the impact of waveforms are presented. Finally, Section V concludes and will give recommendations for 6G sub-THz system designs.

II. Use Case and Requirements

A. Use Case

We consider as an exemplary use case a hot spot scenario serving users in a 10 GHz bandwidth with a target total cell rate of 100 Gbit/s and a range of 100 – 200 m. These values are within the range of 6G KPIs introduced in [13]. To achieve this rate, we assume cross polarized transmission. The required spectral efficiency (SE) is 5 bit/s/Hz per polarization, which corresponds e.g. to a modulation with 64QAM and a FEC encoding rate of 0.83. Alternatively, we can consider 2 user equipment (UE) with 2 MIMO streams each and the same cell rate. With 16QAM and a FEC encoding rate of 0.625 the total of 4*2.5 bit/s/Hz = 10 bit/s/Hz can be achieved.

B. Requirements

To assess the power consumption we first assess the required total transmit power for the use case above, which then can be mapped to the different architectures. For the coarse assessment of the basic behaviour we use a simplified set of assumptions. We take into account line-of-sight (LOS) propagation and in the multi-user case a similar path loss for each user. In the link budget analysis, we take into account the carrier frequency, bandwidth, receiver noise figure, target rate and distance with some exemplary values. From the required minimum signal-to-noise-ratio (SNR) derived for a specific spectral efficiency (SE) with the Shannon formula

$$SNR[dB] = 10 \cdot \log(2^{SE} - 1) \quad (1)$$

and the free space path loss

$$PL = 20 \cdot log\left(\frac{4\pi \cdot d \cdot f}{c}\right) \quad (2)$$

with distance d, carrier frequency f and speed of light c we can calculate the total EIRP needed per polarization. The total required transmit (tx) output power based on an exemplary link budget for two UEs with two polarizations is shown in TABLE I.

TABLE I. Exemplary Link Budget for two UEs

Carrier frequency	120	120	GHz
2 Polarizations	4	4	MIMO streams
Bandwidth	10	10	GHz
Target rate	**100**	**10**	**Gbit/s**
Spectral efficiency	2.5	0.25	Bit/s/Hz
Required SNR lin. scale	4.66	0.19	
Required SNR in dB	6.68	-7.23	dB
Noise power	-74	-74	dBm
Noise figure	10	10	dB
Rx signal power	-57.32	-71.24	dBm
Distance	100	100	m
Free space path loss	114.03	114.03	dB
Tx EIRP per stream	56.71	42.79	dBm
Total EIRP	**62.73**	**48.82**	**dBm**

A total average EIRP of more than 60 dBm is needed to achieve the target cell rate of 100 Gbit/s at 100 m distance. This value will further increase with distance and carrier frequency. The required EIRP can be achieved with a combination of a PA with reasonable output power and a beamforming antenna array providing sufficient gain. Another interesting case is the required output power if the target data rate at cell edge of 100 m is relaxed to 10 Gbit/s. Using a similar analysis gives a total EIRP of 48.8 dBm. With that total EIRP the maximum achievable LOS distance for 100 Gbit/s would go down to below 20 m. At this point it becomes obvious that for the extreme data rates large number of PAs and array elements with related high power consumption is expected.

III. Power Consumption Model

A. Model description

Among the large variety of system architectures we have chosen one which is widely used for highly integrated system on chip (SoC) design at 90 GHz [5]. The transmitter part (Fig. 1) comprises a digital tx processing block, digital-to-analog (DAC) converters, local oscillator (LO) + synthesizer, analog baseband (BB) part, upconversion, a splitter, analog phase shifters and PAs located as close as possible to the antenna to minimize feeder losses. The receiver part (Fig. 2) is equipped with a low noise amplifier per antenna element, phase shifter and combiner, downconversion with LO and synthesizer, analog BB, ADC and digital receive (rx) procesing.

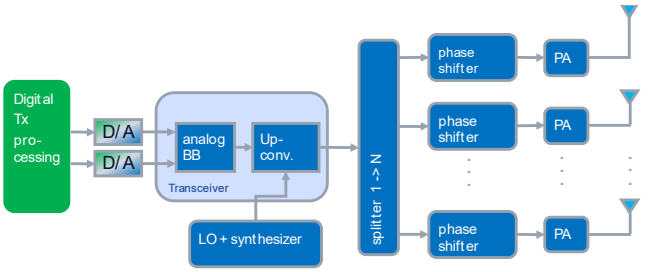

Fig. 1. Building blocks of power consumption model, transmitter part for analog BF

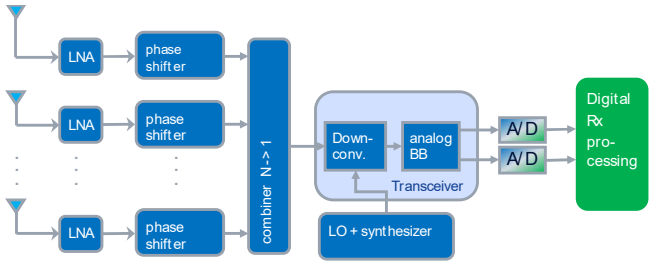

Fig. 2. Building blocks of power consumption model, receiver part for analog beamforming (BF)

This basic architecture represents an analog beamforming (BF) with N antenna elements. It can be easily extended towards hybrid and full digital architectures with N antenna elements by scaling the number of analog BB and conversion chains accordingly, as described e.g. in [6] and shown in TABLE II. For the hybrid architecture this results in M subpanels with N/M elements each. The number of DACs and ADCs is twice the number of analog BB and conversion chains since we assume complex I and Q signals, although in general also sampling of the bandpass signal at a low intermediate frequency (IF) with one converter would be possible and the I and Q demodulation then is shifted to the digital processing.

With this model we can formulate the power consumption of the base station transceiver as follows:

$$P_{tx} = N \cdot P_{PA} + k \cdot P_{uc,\,aBB} + P_{LO,\,synth} + 2 \cdot k \cdot P_{DAC} + P_{dBB,tx} \quad (3)$$

$$P_{rx} = N \cdot P_{LNA} + k \cdot P_{dc,aBB} + P_{LO,synth} + 2 \cdot k \cdot P_{ADC} + P_{dBB,rx} \quad (4)$$

$$P_{tot} = P_{tx} + P_{rx} \quad (5)$$

With $k = 1$ for analog BF, $k=M$ for hybrid and $k=N$ for digital BF, P_{PA}, P_{LNA}, $P_{uc,aBB}$ and $P_{dc,\,aBB}$, $P_{LO,\,synth}$, P_{DAC} and P_{ADC}, $P_{dBB,tx}$, $P_{dBB,rx}$ meaning the power consumption of PA, LNA,

upconversion, downconversion with analog BB, LO and synthesizer, DAC and ADC, and digital baseband processing of tx and rx side, respectively. Since the digital baseband processing depends not only on sampling rate and carrier frequency, but is also impacted by the used algorithms and targeted number of streams, it is omitted here for this analysis and will be treated in a separate work.

TABLE II. SCALING NUMBER OF BUILDING BLOCKS FOR DIFFERENT BEAMFORMING ARCHITECTURES

Building blocks	Scaling			Power consumption @ 90 GHz [mW]
	Analog BF	*Hybrid BF*	*Digital BF*	
Tx part				
PA, active phase shifter, splitter	N	N	N	275
Analog BB and upconverter	1	M	N	500
LO + synthesizer	1	1	1	100
DAC	2	2M	2N	750
Digital tx processing	1	1 … M	1 … N	n.a.
Rx part				
LNA, active phase shifter, combiner	N	N	N	225
Downconverter and analog BB	1	M	N	500
LO + synthesizer	1	1	1	100
ADC	2	2M	2N	40 - 200[a]
Digital rx processing	1	1 … M	1 … N	n.a.
Max. no. of MIMO streams	1	M	N	

[a.] depending on selected model: Walden FOM envelope or circuit theoretical approach

B. Power consumption data of devices and building blocks

For the 60 GHz frequency band and also up to 90 GHz there exists a variety of devices and even fully integrated systems, so that power consumption data for specific designs is available. But for the sub-THz range the data base is only small yet. To get suitable power consumption data to feed the model we start with published power consumption data of an exemplary analog frontend operating at 90 GHz [5] and apply trends towards higher frequencies derived from device surveys [9], [10], [11] and manufacturers informations. The data from [5], extended by data for DAC [8] and ADC [9], is also summarized in TABLE II.

The PA survey [10] provides a large data collection of PA devices operating at different frequency bands and realized with different technologies (CMOS, SiGe, InP and others). Since for CMOS and GaN technology the survey contains only few or no devices at the higher frequencies, we will focus our analysis on SiGe. Based on typical values of saturated output power Psat, power added efficiency PAE and gain values reasonable for devices operating at 90 GHz, 120 GHz and around 230 GHz we derive a more generic model covering the effect of reduced output power and decreasing PAE. The relation between Psat, PAE and gain is according to (6):

$$P_{DC} = \frac{Psat \cdot \left(1 - \frac{1}{gain}\right)}{PAE\,[\%]} \cdot 100 \qquad (6)$$

We derive a scaling factor indicating the increase in DC power when going to higher frequencies, and apply this to the known values given for the system at 90 GHz (TABLE II. TABLE III. shows parameters taken from [10] and the derived scaling factors Q_{PA} for the DC power consumption per PA and related Q_{mW} for DC power consumption per mW output power. Despite of the increase in power consumption it should be noted that the output power reduces by 3 and 6 dB for 120 and 230 GHz, respectively. This needs to be taken into account in the model if total output power or coverage has to be maintained.

TABLE III. EXEMPLARY PA DATA FROM [10] FOR DIFFERENT CARRIER FREQUENCIES

f [GHz]	Psat [dBm]	PAE [%]	Gain [dB]	P_{DC} [mW]	Q_{PA}	Q_{mW} [mW]
90	18	15	15	407	1	6.45
120	15	6	15	510	1.25	16.13
230	12	2	15	767	1.88	48.39

For the LNA on rx side a similar survey [11] provides device data. A closer analysis revealed that the power consumption across different technologies and in the frequency range between 60 GHz and 300 GHz does not vary much. Almost all reported power consumption values are in the range of 24 mW … 63 mW. Since these values are significantly less than e.g. the PA values it seems justified to use a constant frequency-independent value in the power consumption model. The power consumption of the analog BB and up- and downconverters, as well as DAC, are assumed to be affected mainly by the signal bandwidth rather than the carrier frequency. Since we do not change this parameter we keep these values for the further analysis unchanged. For LO and synthesizer also only a negligible variation over the targeted frequency range is assumed.

The ADC power consumption depends on sampling rate and number of bits, and can be calculated using e.g. the Walden figure of merit (FOM), which is an empirical approach based on data of real existing ADC devices [9]. It gives the normalized energy in femto-Joule needed per conversion step versus the sampling rate in Hz. The envelope of the device data, denoting the lowest energy values of existing devices, gives a lower bound for the sampling rate dependent FOM

$$FOM_{envelope}(f_s) = 0.88\sqrt{\left(1 + \left(\frac{f_s}{371 \cdot 10^6}\right)^2\right)}\ \frac{\text{fJ}}{conv.-step} \qquad (7)$$

so that

$$FOM_{evelope}(f_s = 10GHz) = 23.7\ \text{fJ/conversion step}.$$

To reflect a more practical case we also calculated an average FOM from the data given in [9].

$$FOM_{avg}(f_s = 10GHz) = 342\ \text{fJ/conversion step}$$

The related power consumption can be calculated as (8):

$$P(f_s) = \text{FOM}(f_s) \cdot f_s \cdot 2^{ENOB}\ [\text{fW}] \qquad (8)$$

with f_s = sampling rate in Hz and ENOB = effective number of bits.

Alternatively, a circuit theoretical approach can be applied, as e.g. described in [7]. In TABLE II. we noted the value for eight bit resolution and a sampling rate of 10 GHz. The ADC power consumption vs ENOB for envelope and average Walden FOM and for the circuit theoretical model is shown in Fig. 3. To summarize the insights from the device survey analysis: On tx side the most dominating frequency dependent part is, as expected, the PA, whereas the other parts do not significantly depend on the carrier frequency and remain unchanged. So, we

apply the identified scaling factors from TABLE III. to the PA part. The other parts depend on bandwidth or are independent over the parameter variations. The ADC is dominating the power consumption on rx side, due to the significant impact of the resolution. Thus, we will take into account different quantization levels.

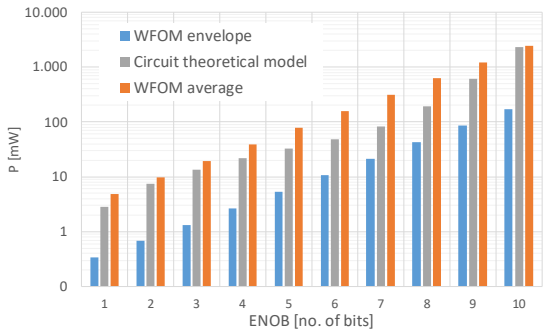

Fig. 3. Single ADC power consumption for $f_s = 10\text{Gsamples/s}$

IV. Energy Efficiency Analysis

A. Impact of PA

In this section we highlight the power consumption applying the model of section III to the different architectures and frequency bands. The main variation will be due to the PA, if bandwidth and ADC resolution are kept constant. The following analysis is for a bandwidth of 10 GHz, an ADC resolution of 8 bits and an array size of 64 elements. At 90 GHz the achievable distance is about 48 m. We now consider two cases. First, we keep the array size constant and assume a tx power reduction versus frequency as given in TABLE III. Then, we compensate for the tx power reduction and the path loss increase by increasing the array size to achieve the same coverage as for f_c=90 GHz. A simplified link budget is shown in TABLE IV. In the link budget we assume 5dBi element gain and a combined power and array gain of 20log$N$, N = number of antenna elements.

TABLE IV. Achievable distance for different frequencies and array sizes (simplified model)

f_c	**90**	**120**	**230**	**120**	**230**	**GHz**
Parallel streams	2	2	2	2	2	
Bandwidth	10	10	10	10	10	GHz
Target rate	100	100	100	100	100	Gb/s
SE per stream	5	5	5	5	5	b/s/Hz
Tx output power	18	15	12	15	12	dBm
Array element gain	5	5	5	5	5	dBm
No.of array elements	64	64	64	120	320	
Array + power gain	36.1	36.1	36.1	41.6	50.1	dB
Total tx EIRP	**59.1**	**56.1**	**53.1**	**61.6**	**67.1**	**dBm**
EIRP per stream	56.1	53.1	50.1	58.6	64.0	dBm
Required SNR	31	31	31	31	31	
Required SNR in dB	14.9	14.9	14.9	14.9	14.9	dB
Noise power	-74	-74	-74	-74	-74	dBm
Noise figure	10	10	10	10	10	dB
Min. Rx power per stream	-49.1	-49.1	-49.1	-49.1	-49.1	dBm
Allowed path loss (LOS)	105.2	102.2	99.2	107.7	113.2	dB
Distance	**48.3**	**25.7**	**9.5**	**48.1**	**47.4**	**m**

As expected, the achievable distance decreases significantly when increasing the carrier frequency without increasing the antenna gain. The first three columns keep the array size constant and indicate shrinking distance, the columns 4 and 5 increase the number of antenna elements and PAs to maintain the distance of about 48 m of the 90 GHz reference case.

Next we consider the RF frontend power consumption for the different frequencies, architectures and array sizes. The power consumption model of section III is applied, with N = 64 and K = 1, 4 and N for the analog, hybrid and digital case, respectively. Further, for 120 GHz and 230 GHz also N = 120 and 320, respectively, has been calculated. For the "PA, phase shifter and splitter" block we assume that the PA consumes about 80% of the power, so that for splitter and phase shifter $275mW \cdot 0.2 = 55\ mW$ remain. The fraction of PA power consumption is then scaled to the output power given in TABLE III. according to (6). Fig. 4 shows the resulting power consumption of the tx part of the RF frontend.

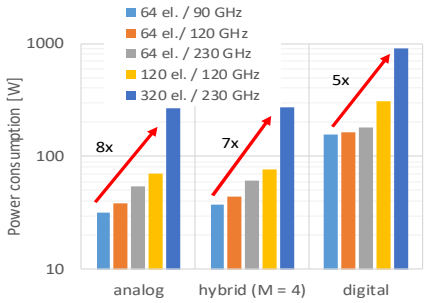

Fig. 4. Power consumption of tx part for analog, hybrid and digital architectures and frequencies of 90 GHz, 120 GHz and 230 GHz, no backoff

Whereas the increase for 120 GHz is still moderate with a factor around 2, the 230 GHz case with compensation of path loss and reduced possible PA output power requires up to 8 times the power of the reference case.

The assessments up to here are valid assuming Psat as total tx output power. Due to the non-linear behaviour of the PA in practice the total tx output power is reduced by the backoff (BO), usually given in dB. Given that the maximum PA output power is limited, this must be compensated by an array size increased by a factor $u = 10^{\left(\frac{BO}{20}\right)}$, as indicated in TABLE V. The EIRP per MIMO stream s then is calculated as

$$EIRP_{stream} = P_{Sat} - BO + gain_{element} + \cdots \\ +20 \cdot \log(N) + 20 \cdot \log(u) - 10 \cdot \log s \qquad (9)$$

TABLE V. No. of array elements N needed to compensate carrier frequency, path loss and backoff

f_c **[GHz]**	**90**			**120**			**230**		
Backoff [dB]	0	-3	-7	0	-3	-7	0	-3	-7
N (d ~48m)	64	90	144	120	168	268	320	452	716

The lower tx output power leads to less power consumption per PA, but at the same time the PAE is also reduced, so that the power consumption does not scale linearly with the output power. The PAE variation depends on the PA type. At microwave and mm-wave frequencies PAE values of up to 45% can be achieved, which go down to 50% or even less at a backoff of 7 dB [15], as usually applied for OFDM signals. In our case the maximum PAEs are already comparably small, so that the resulting DC power consumption will become very large.

The following analysis compares the power consumption of the previous setup with a backoff of 3 and 7 dB. The PAE for backoff 3 dB and 7 dB is assumed 80% and 56% of PAEmax, assuming a similar scaling as indicated in [15]. Applying the

model of section III and increasing the array size to compensate the EIRP leads to the results shown in Fig. 5. For the analog and hybrid architecture at 90 and 120 GHz there is almost no difference between 3 dB and 7 dB backoff. For the digital architecture the power consumption increases strongly. This is due to the very large arrays needed to achieve the target EIRP, and the resulting large number of chains. For analog and hybrid architectures the PA is the dominant power consuming device, and the increased number of PAs is widely compensated by the lower power consumption at lower output power, despite of the also lowered PAE. The digital architecture requires much more analog BB and conversion chains, so that also the DAC and upconversion power consumption scales with the number of array elements N needed for the target EIRP. Although the PAs need to be operated with a certain backoff, a lower backoff in a digital architecture helps to keep the number of PAs lower and therefore also the overall power consumption.

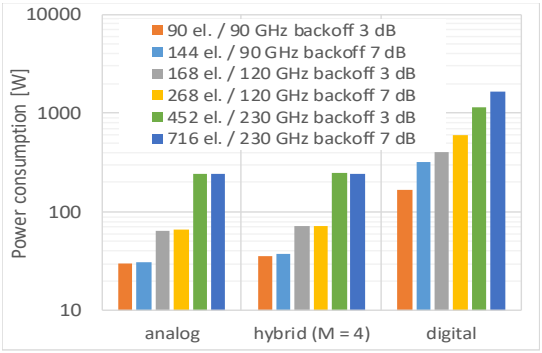

Fig. 5. Power consumption for different architectures and frequencies

B. *Impact of ADC resolution*

On receiver side the ADC consumes energy depending on both, sampling rate and resolution. The high impact of the number of bits suggests reducing ADC resolution to a reasonably small value to save energy. In [12] it is shown that using multiple antenna elements and ideal maximum ratio combining (MRC) leads to an improvement of the SNR at the detection point SNR_{MRC} which is proportional to the number of antenna elements N, compared to the SNR at each single antenna element SNR_{SE} (SNR in linear scale):

$$SNR_{MRC} = N \cdot SNR_{SE} \tag{10}$$

This is valid for the unquantized case. In case of quantization and in combination with channel estimation errors, the SNR at the detection point is further reduced, as derived in [12], (20) and (25). For ideal channel knowledge it is e.g.

$$\frac{SNR_{MRC}}{SNR_{SE}} \sim \frac{N}{1+\frac{1}{SQR}+\frac{a}{SQR+\frac{1}{\sigma_n^2}}} \tag{11}$$

with SQR = signal to quantization error ratio, σ_n^2 = noise variance at each element and a is a factor depending on the channel statistics. It should be noted that for $SQR \rightarrow \infty$ this results in (10). With channel estimation errors assumed the relation is even more complex.

TABLE VI. SNR REDUCTION IN DB DUE TO 2 AND 3 BIT QUANTIZATION

Channel estimantion	ideal		realistic	
SNR_{SE} [dB]	0	5	0	5
2 bits quantization	-0.8	-1.6	-3.2	-4.0
3 bits quantization	-0.6	-1.1	-2.0	-2.5

The SNR reduction at the decision point due to quantization with 2 and 3 bits compared to the unquantized case, for SNR_{SE} of 0 dB and 5 dB, taken from [12], is shown in TABLE VI. The realistic channel estimation increases the quantization impact, also an increased SNR_{SE} leads to higher losses for larger quantization, because quantization noise becomes more dominant then.Now, similarly as on the transmitter side we can increase the array size to compensate for the quantization losses and assessing the power consumption trade-off between smaller number of high resolution ADCs and a larger number of low resolution ADCs providing the same performance. From [12] it can be derived for the digital beamforming case that the factor for increase of N to maintain the performance of unquantized case at $SNR_{SE} = 5\ dB$ is about 2.6 and 1.7 for 2 bit and 3 bit quantization, respectively. At $SNR_{SE} = 0\ dB$ the corresponding values are 2.3 and 1.8, respectively (realistic channel estimation assumed). Hence there is only a moderate increase in number of RF chains and antenna elements needed to compensate the quantization effect. In Fig. 6 we see that the power consumption of the ADCs is significantly reduced, although the number of ADCs is increased for lower resolution. According to (8) the power consumption reduction per ADC is proportional to 2^3 for 3 bit and 2^4 for 2 bit resolution, compared to 6 bit reference.

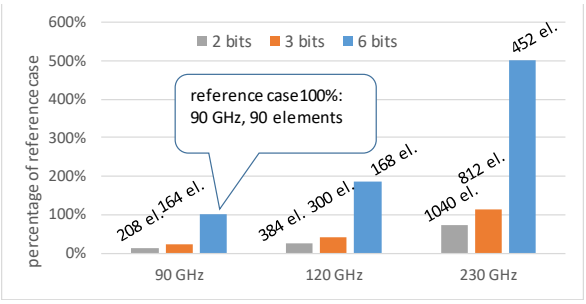

Fig. 6. Percentage of ADC power consumption relative to 90 GHz / 6 bit resolution case, digital architecture. No.of elements (el.) needed to maintain performance of 6 bit case.

C. *Overall power consumption analysis*

The following tables indicate the percentage of PA and ADC power consumption to the total power consumption. From TABLE VII. we see that the PA is dominating in the analog and hybrid case, whereas in the digital architecture also the analog baseband blocks contribute more due to their higher number.

TABLE VII. PA POWER CONSUMPTION CONTRIBUTION TO TOTAL TX POWER CONSUMPTION

Carrier frequency [GHz]	analog	hybrid	digital
90	93.0%	77.5%	16.5%
120	96.8%	88.6%	15.8%
230	99.1%	96.8%	21.1%

The ADC power consumption (TABLE VIII.) with the average FOM model is rather low. Although there are large variations between 2 and 8 bit resolution the contribution to the overall power consumption in the investigated scenario is not significant, except for the digital architecture. But since it is expected that the number of parallel MIMO streams at sub-THz frequencies will be low compared to the number of antenna elements, the ratio of ADC power consumption will rather decrease when array size increases. Fig. 7 compares the total power consumption of the analog frontend for the different frequencies. We take the values for the analog, hybrid and digital architecture for 3 dB backoff (90, 168 and 452 array elements for 90, 120 and 230 GHz, respectively), and show the

contribution of the tx and rx parts. The tx part is dominating the overall power consumption. The rx part consumes only about 25% of the power for analog and hybrid architectures. This is mainly due to the PA in combination with the high number of antenna elements, which is similar in all the architectures. In the digital case in addition also the baseband blocks scale with the number of antenna elements, so that the increase versus frequency is higher.

TABLE VIII. ADC POWER CONSUMPTION CONTRIBUTION TO TOTAL RX POWER CONSUMPTION (AVERAGE FOM ASSUMED)

f_c [GHz]	No. of bits	Analog	Hybrid	Digital
90	2	0.1%	0.3%	2.6%
	3	0.2%	0.7%	5.1%
	8	5.6%	18.2%	63.1%
120	2	0.1%	0.2%	2.6%
	3	0.1%	0.4%	5.1%
	8	3.1%	11.1%	63.1%
230	2	0.0%	0.1%	2.6%
	3	0.0%	0.1%	5.1%
	8	1.2%	4.6%	63.1%

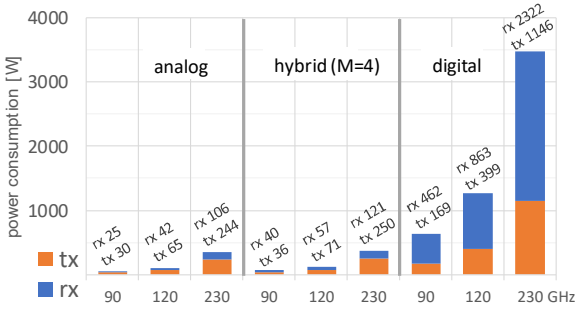

Fig. 7. Total power consumption of tx and rx part (analog, hybrid and digital architecture, 90 – 230 GHz carrier frequency with 90, 168 and 452 array elements, respectively). Labels indicating power consumption in W, 8 bit ADC resolution, average WFOM model

V. SUMMARY AND CONCLUSIONS

In this paper the power consumption of the different building blocks of the analog frontend of a wireless communication system has been analysed. For a target rate of 100 Gbit/s in a 10 GHz bandwidth the contribution of the individual functional blocks to the overall power consumption at frequencies of 90 GHz, 120 GHz and 230 GHz has been considered. The EIRP has been maintained at higher frequencies by compensating the reduced PA output power, path loss and backoff requirements by increasing the number of antenna elements. We investigated the impact of low resolution ADCs on power consumption when exploiting a tradeoff between ADC resolution and number of elements. The investigations show that to achieve at 230 GHz a similar coverage as at 90 GHz a factor of five increased number of antenna elements is needed, because PA output power and PAE decrease strongly. One remarkable aspect is the fact that the PAPR reduction of transmission signals does not notably affect the overall power consumption for a given communication distance. But e.g. a 3 dB improvement in PAPR would allow 3 dB higher average output power, which increases supported communication distance by a factor of ≈1.4. Digital architecture at 230 GHz leads to high power consumption driven by the scaling of the baseband functions with N. Analog architecture has the lowest power consumption, but does not allow for spatial multiplexing of multiple users. Realistically only few simultaneously served users can be expected, so that a hybrid approach with a number of M smaller than N (e.g. $M = 4$ or 8) seems the most reasonable approach. On rx side the contribution of ADCs, even with higher resolution, is rather small. Although low resolution would be feasible with the high number of antenna elements, it is questionable to which extent this is feasible with a hybrid approach with few analog BB and conversion chains only. A further open point is the power consumption of the digital baseband processing. This depends not on the carrier frequency, but on the bandwidth, the number of simultaneous MIMO streams and further on the used algorithms. These points will be subject to future work.

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