

FPGA-based CDMA Switch for Networks-on-Chip

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Abstract

This paper presents timing and area results for an FPGA implementation of a CDMA-based switch for networks-on-chip. The design was mapped onto the Xilinx Virtex4 XC4VLX200 device using Synplify Pro for a range of payload sizes. The synthesis results give the area and maximum frequency obtained. Simulation verifies the desired functionality and provides throughput and latency values as functions of payload size.

1. Introduction

Networks-on-Chip (NoC) have received a great deal of attention as a new type of on-chip communication to replace or augment traditional buses [1]. A bus is a shared resource which does not support concurrent transactions. In addition, buses do not scale well due to increasing capacitance and more difficult skew constraints as the lines get longer and clock rates become faster. A switched network model, however, can support parallel transfers and can be scaled up to support a large number of communicating resources. Moreover, a regular network topology can be constructed to have well-defined communication delays. In a previous paper [2] we described the high-level architecture of a code division multiple access (CDMA) switch for NoC applications. In this paper, we give detailed synthesis and simulation results for an FPGA implementation of this switch.

2. Architecture

The proposed CDMA-based switch is shown in Figure 1. Data is transferred in a packet format, which is divided into four fields: valid packet field (1-bit), source address field (3-bit), destination address field (3-bit) and payload field (2^N -bit). Using a set of 8, 8-bit Walsh codewords, we assigned seven of the codewords to correspond to the seven possible Intellectual Property (IP) blocks that may be attached to the switch. The remaining codeword, which is the

all-zero codeword, is reserved for use in specifying that a resource does not have any valid data to send. The switch is easily scalable to handle a larger number of IP blocks by using longer Walsh codewords.

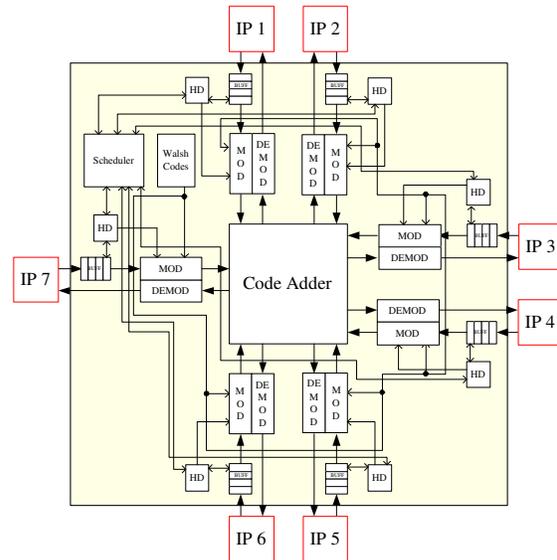


Figure 1. CDMA Switch Architecture

For a given packet, the codeword corresponding to the desired destination address is modulated with each bit of the packet and the modulated data is transmitted as a parallel word in order to obtain higher throughput. The modulation algorithm is described in Table 1.

Table 1. Modulation Algorithm

Data	Codeword Assignment
0	Codeword itself
1	Inverted codeword
No data	All-zero codeword

The demodulator recovers the original data from the summation value produced by the code adder. The sum-

mation range is variable depending on the number of codewords that are used. The demodulation algorithm is described in Table 2.

$$D[i] = \begin{cases} (2S[i] - L) & \text{if codeword}[i] \text{ is } 0 \\ (-2S[i] + L) & \text{if codeword}[i] \text{ is } 1 \end{cases} \quad (1)$$

$$\lambda = \sum_{i=0}^{L-1} \frac{D[i]}{N} \quad (2)$$

$D[i]$ is the decision variable derived from the $S[i]$, which is the summation of all modulated values. L is the codeword length and λ is the decision factor.

Table 2. Demodulation Algorithm

Decision Factor(λ)	Demodulated Data[bit]
+1	1
-1	0
0	No data sent

3. FPGA Synthesis and Simulation

The proposed architecture was described using VHDL and was synthesized onto the Xilinx Virtex4 XC4VLX200 device with the FF1513 package and the -10 speed grade using Synplify Pro 7.7. The number of 4-input LUTs and flip-flops were determined for each block in the switch as a function of payload size, and these values are listed in Table 3. As shown in the table, a 128-bit payload was the longest size that would fit within the target FPGA. However, for a system built with this particular device the most practical payload size to use would likely be either 8, 16 or 32 bits, as these would still leave most of the FPGA resources available for the implementation of the attached IP blocks.

Table 4 presents the optimal estimated frequency and the total path delay for various payload sizes. The total path delay information indicates that the delay was nearly evenly balanced between logic and routing.

The functionality of the CDMA switch architecture was verified using ModelSim simulations. The clock frequency used in the simulation was derived from the optimal estimated frequency values of Table 4 that avoid negative slack. For payload sizes from 8 bits to 64 we used a 14 ns clock period (71.4 MHz), while an 18 ns clock period (55.5 MHz) was used for the case of 128-bit payloads. With these values, the maximum aggregate throughput values, in bits per second, can be computed for each payload size by forming the following product: (7 IP resources)*(number of payload bits)*(clock frequency). (Note that we assume that the interconnections between the IP resources and the switch are parallel paths whose width is equal to the total packet

length.) Therefore, we arrive at throughput values of 3.9 Gbps for the case of an 8-bit payload up to 49.7 Gbps for the case of a 128-bit payload. In addition, simulation results for average latency range from 90.0 ns to 115.7 ns for the five different payload sizes considered.

Table 3. Area Report

Xilinx Virtex4 XC4VLX200 (AREA)										
Components	Payload Size									
	8 bits		16 bits		32 bits		64 bits		128 bits	
	4-input LUTs	Flip Flops	4-input LUTs	Flip Flops						
MOD	1769	0	2835	0	5009	0	7839	0	14534	0
BUFF	1239	1920	1984	2870	3507	4774	5487	8686	10174	16202
HD	0	42	0	42	0	42	0	42	0	42
SCHE	49	7	46	7	48	7	49	7	48	7
CA	3033	0	4736	0	7826	0	17336	0	25016	0
DEM0D	4822	105	7289	161	12757	273	20224	497	111900	945
Total	10912 out of 178156	2074 out of 178156	16890 out of 178156	3080 out of 178156	29147 out of 178156	5096 out of 178156	50935 out of 178156	9232 out of 178156	161672 out of 178156	17196 out of 178156
Utilization	6.1 %	1.2 %	9.5 %	1.7 %	16.4 %	2.9 %	28.6 %	5.2 %	90.7 %	9.6 %

Table 4. Timing Report

Xilinx Virtex4 XC4VLX200 (TIMING)			
Payload Size	Optimal Estimated Frequency (to avoid negative slack)	Total Path Delay (Propagation + Setup)	
		Logic	Route
		8 bits	74.3 MHz (13.451 ns)
16 bits	76.4 MHz (13.082 ns)	6.377 ns (48.7%)	6.706 ns (51.3%)
32 bits	78.0 MHz (12.815 ns)	6.134 ns (47.9%)	6.681 ns (52.1%)
64 bits	76.1 MHz (13.139 ns)	6.377 ns (58.6%)	6.752 ns (51.4%)
128 bits	61.8 MHz (16.174 ns)	8.826 ns (54.6%)	7.348 ns (45.4%)

4. Conclusions

In this paper, we presented synthesis and simulation results for an FPGA implementation of a CDMA switch for use in network-on-chip applications. The switch was synthesized onto the Xilinx Virtex4 XC4VLX200 device using Synplify Pro 7.7, and throughput and latency values were obtained for a range of payload sizes. The results show that this architecture would be practical to use in this FPGA device with payloads from 8 to 32 bits.

References

[1] L. Benini and G. D. Micheli, "Networks on chip: A new paradigm for systems on chip design," *IEEE DATE Conference*, pp. 418-419, 2002.

[2] D. Kim, M. Kim and G. E. Sobelman, "CDMA-based Network-on-Chip architecture," *IEEE Asia Pacific Conference on Circuits and Systems*, pp. 137-140, 2004.