Partial Reconfiguration for Design Optimization

Marie Nguyen, Nathan Serafin, and James C. Hoe Carnegie Mellon University

Pittsburgh, Pennsylvania

Abstract—FPGA designers have traditionally shared a similar design methodology with ASIC designers. Most notably, at design time, FPGA designers commit to a fixed allocation of logic resources to modules in a design. At runtime, some of the occupied resources could be left idle or under-utilized due to hard-toavoid sources of inefficiencies (e.g., operation dependencies). With partial reconfiguration (PR), FPGA resources can be re-allocated over time. Therefore, using PR, a designer can attempt to reduce idleness and under-utilization with better area-time scheduling.

In this paper, we explain when, how, and why PR-style designs can improve over the performance-area Pareto front of ASICstyle designs (without PR). We first introduce the concept of area-time volume to explain why PR-style designs can improve upon ASIC-style designs. We identify resource under-utilization as an opportunity that can be exploited by PR-style designs. We then present a first-order analytical model to help a designer decide if a PR-style design can be beneficial. When it is the case, the model points to the most suitable PR execution strategy and provides an estimate of the improvement. The model is validated in three case studies.

I. INTRODUCTION

Motivations. Today, with growing emphasis on deploying Field Programmable Gate Arrays (FPGAs) for computing, we are starting to see FPGAs' reprogrammability being recognized as a deciding feature in selecting FPGAs over ASICs [1]. Yet, partial reconfiguration (PR), which allows parts of an FPGA to be reconfigured at millisecond timescales, remains an under-appreciated capability.

This paper explores the questions of when, how, and why FPGA designers should consider using PR. The discussions in this paper focus on the use of PR in challenging design scenarios that have to deliver required performance under strict area, cost, power, and energy constraints (e.g., [2], [3]). This work is particularly relevant to AI-driven applications at the Edge (e.g., [4], [5], [2], [3]) that (1) are deployed on low-end FPGAs due to cost, power, and size concerns, and (2) need to accelerate many compute intensive tasks with stringent latency or throughput requirements ([2], [6], [7]).

Shortcomings of ASIC-Style Designs. To accelerate these constrained applications on the FPGA, designers typically commit, at design time, to a fixed allocation of logic resources to modules. We refer to this design as an ASIC-style design. At runtime, some of the occupied resources could be left idle or under-utilized due to hard-to-avoid sources of inefficiencies (e.g., operation dependencies) which may occur even in a highly-optimized design. Under-utilization may result in (1) the design not running at the desired performance given an area budget, or (2) the design running at the desired performance but being too big to fit in the given area.

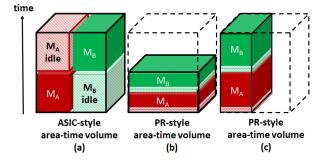


Fig. 1: In an ASIC-style design, logic resources that are inactive still occupy the fabric. In a PR-style design, underutilization can be reduced with better area-time scheduling.

PR-Style Designs to Reduce Under-Utilization. Using PR, a designer can attempt to reduce under-utilization by changing the allocation of resources over time. In this paper, we identify under-utilization of resources as an opportunity that can be exploited by PR-style designs to improve upon ASIC-style designs. We refer to a PR-style design as a design in which *logic resources are allocated to different modules of one design over time. In return, a PR-style design may be faster and/or smaller than an ASIC-style design* (illustration in Figure 1).

This work: when, how and why PR. To address the questions of when, how, and why PR, this paper develops a set of PR execution strategies (allocation and scheduling) applicable to a range of non-trivial applications. An application consists of a set of tasks, and each task is accelerated by a hardware module. Modules can be dependent, execute concurrently, and have multiple implementation variants with different performancearea trade-offs. Dependent modules share data either through (1) external memory or (2) on-chip memory. The paper proposes a first-order analytical model to help a designer (1) determine a suitable PR execution strategy and (2) analyze the throughput and latency of ASIC-style and PR-style designs. The model enables quick exploration of the design space to help decide if a PR-style design can be beneficial for a given problem. The effectiveness of this model is examined in three compute-bound case studies involving computer vision and machine learning tasks.

The contributions of this paper are:

- developing a set of PR execution strategies for practical design scenarios
- developing a first-order performance model to estimate ASIC-style and PR-style designs' performance
- demonstrating the effectiveness of the performance model

with three case studies of implemented designs.

II. BACKGROUND AND RELATED WORK

Partial Reconfiguration. When using PR, the FPGA fabric is divided into a non-reconfigurable region (containing the I/O infrastructure) and PR regions that can be reprogrammed individually at runtime. Each PR region can be reprogrammed at runtime with partial bitstreams built for this region at design time. When loading bitstreams from on-board DRAM, the time to load a PR region (PR time) is a function of the bitstream size, e.g., approximately 453 MB/sec on an Ultrascale+ device through the processor configuration access port (PCAP).

Applications of PR Today. Many academic projects have explored the potential of using PR (e.g., [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20]). Commercially, PR has been mainly used in a "role-and-shell" approach ([1], [21]). A static shell design provides I/O and isolation while independent designs with different functionalities, or roles, can be loaded as required (e.g., [1], [21]). The different role designs reuse the same logic resources over time. However, each role is still an ASIC-style design. This paper does not focus on using PR in a role-and-shell approach.

PR-Style Benefits. In a PR-style design, the designer decides how the FPGA is divided into PR regions and when/which reconfigurations are needed during the design's execution. For instance, in [22], to accelerate a vision processing pipeline, a PR region is reconfigured every few milliseconds with different pipeline stages.

For domain-specific applications, other prior works have exploited under-utilization in ASIC-style designs, and have shown that using PR can provide area [23], performance [24], [25], [26], power/energy [27], [28], and compilation time reduction [29] benefits. For instance, in adaptive [30] or cloud computing applications ([31], [32], [33]), multiple modes or implementation variants exist for a module but only one is needed at a time depending on the context. Instead of mapping all variants of a module in an ASIC-style design, only one variant is reprogrammed on the fabric at a time.

Scheduling for PR-Style. A vast body of work on FPGA OSes ([34], [35], [36], [37], [38]) and on FPGA virtualization ([39], [33], [31]) has focused on the theory of spatial and temporal sharing, mechanisms for task preemption, or hardware and software task scheduling [40]. Mostly, these works share the common goal of maximizing resource utilization to improve throughput, and often assume that PR time is negligible compared to compute, and/or that tasks are independent.

Building on top of prior work, this paper introduces the concept of area-time volume to make clear why PR-style designs can be beneficial. We also give practical examples of when it is the case considering both throughput, which is the metric to optimize in many applications (e.g., video analytics [4], [2], batch jobs [5], [41]), and latency, the metric of interest for an emerging class of Edge applications that have tolerance for 100 ms-response time, and that could benefit from FPGA acceleration ([6], [7]). We also account for cases where PR time can be equal to or greater than compute time.

III. WHEN AND HOW CAN PR HELP?

In this section, we use an idealized and simplified example to develop the intuitions behind when and how PR-style designs can be faster or smaller than ASIC-style designs. The next section continues with a more complete examination.

A. Simplified Execution Model

We consider an application with two dependent tasks, $task_A$ and $task_B$; $task_B$ can start only after $task_A$ is finished. Each task runs once per execution of the application. The latency of the application is the sum of the two dependent tasks' latencies. Multiple implementation module variants exist for $task_A$ and $task_B$ and are characterized by the latency function $Lat_i()$. $Lat_i(a)$ is the latency achieved by the module variant for $task_i$ using a logic resources. For a given $task_i$, larger variants have lower latency, $Lat_i(a) < Lat_i(b)$ if a > b.

B. ASIC-Style Design

Consider two common design objectives: (1) minimize latency given an area budget, or (2) minimize area given a latency upper bound. For simplicity, assume $Lat_A(a)=Lat_B(a)$ for any a. In that case, to achieve optimality in either objective, the total logic resources, A_{total} , must be equally divided between $task_A$ and $task_B$'s modules ($A_A=A_B=0.5A_{total}$). The latency of the application is $2Lat_{A/B}(0.5A_{total})$. Solving either optimization scenarios repeatedly for different latency or area targets will produce a set of ASIC-style implementations that trade off latency against logic resources. Starting from this, we ask the question: can a PR-style design improve over the Pareto front of an ASIC-style design?

C. PR-Style Design

The above scenario for the ASIC-style design is shown in Figure 1.a. In this area-time volume representation of the FPGA, the fabric area is 100% occupied by the modules for $task_A$ and $task_B$. However, due to the dependency between the two modules, only one of the two modules is active at a time. In other words, the ASIC-style design has underutilization since some resources available to the design are not active all the time.

In contrast to an ASIC-style design where resource allocation cannot change over time, it is possible to reduce under-utilization with better area-time scheduling in a PR-style design. Therefore, a PR-style design may be able to achieve a smaller area-time volume by being faster, by using fewer resources, or both. For instance, to minimize latency given the same area budget, we can allocate the entirety of A_{total} to a module for task_A first and then to task_B (Figure 1.b). By doing so, the PR-style design's latency is reduced as both modules now run faster using all of the resources available. On the other hand, a PR-style design can maintain the same latency using half the resources by allocating 0.5 A_{total} to a module for task_A first and then to task_B (Figure 1.c). With under-utilization reduced, both PR-style designs fit into smaller area-time volumes than the ASIC-style design. Notice

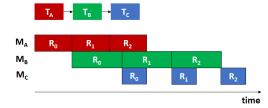


Fig. 2: Example timeline of an application with three dependent tasks accelerated by modules M_A , M_B , and M_C .

in Figure 1.b and Figure 1.c, a small amount of underutilization appears when switching between modules to reflect the non-zero delay to perform PR.

D. Opportunities for Improvement by PR

In ASIC-style designs, resource under-utilization stemming from data dependencies cannot be eliminated without changing the initial algorithm or implementation. In practice, underutilization can arise in other forms. In our simplified example, we assume that module variants exist for any amount of resources. However, module variants for a task only exist at certain performance/resource combinations in practice. The modules selected to fit an area budget in an ASIC-style design may not sum up perfectly to use all resources. Further, when the modules of $task_A$ and $task_B$ are executed in a pipelined fashion to improve the throughput of many independent executions, it may not be possible to find variants with equal throughput for the two tasks; in the resulting unbalanced pipeline, a too-fast stage has to stop or slow down to wait for the other stage. A more subtle example exists when implementing a generic engine capable of accelerating different algorithms or neural networks. This generalized engine consists of a superset of features to accommodate all possibilities but only a subset of features is needed at a time (e.g., NPU [42], DPU [43]). A PR-style design could potentially remove this type of inefficiencies.

IV. ANALYTICAL MODEL

In this section, we present our model and discuss the additional memory requirements of a PR-style design and the impact of limited memory bandwidth on design's performance.

A. Overview

Optimization Goals. To derive our performance model, we consider the problem of maximizing an application's performance given an area budget.

- *minimize the application's latency given an area budget* A. We label this problem as **min L given A**.
- maximize the application's throughput given an area budget A. We label this problem as max T given A.

Execution Model. In this section, we consider an application with N dependent tasks; each task is accelerated by a module. Dependent modules share data either through external or onchip memory depending on data size. Though our discussion focuses on applications with dependent tasks, our model also applies if tasks are independent. We define I as the set

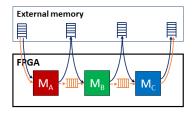


Fig. 3: In an ASIC-style design, dependent modules share data through either external (blue) or on-chip memory (orange) depending on data size.

of subscripts for tasks in the application. A single start-tofinish execution of a module is referred to as a run. If an application requires multiple independent runs, modules can execute concurrently. Figure 2 illustrates this execution model. The example application consists of three dependent tasks $task_A$, $task_B$, and $task_C$ accelerated by three modules. In this application, each module needs to complete three runs R_0 , R_1 , and R_2 . Modules execute concurrently to complete the runs as quickly as possible, subject to the dependency constraints.

We consider two performance metrics, latency and throughput. Latency is defined as the start-to-finish time required for all modules accelerating an application to complete one run (including I/O time for data read and write and compute time). Throughput is defined as the number of runs completed per unit time in steady-state.

Performance-Area Trade-offs. For each module, a finite set of implementation variants exists. A variant accelerating $task_i$ is characterized by its area a_i , its latency $Lat_i(a_i)$, and its throughput $Tput_i(a_i)$ as functions of area. We assume that Lat_* and $Tput_*$ are monotonically increasing functions but make no further assumption on their shape, e.g., performance can scale sub-linearly or lineary with area.

PR-Style Design Considerations. We define $Time_{PR}(a)$ as the time to reconfigure a PR region of size a, and assume that PR time is proportional to the PR region size.

B. ASIC-Style

We first derive the equations for the ASIC-style design that are applicable whether dependent modules share data through external or on-chip memory (Figure 3). In both cases, the number of buffers required to hold intermediate data is N+1. **Min L Given A.** Let $Lat_{Asic}(A)$ be the latency of the ASICstyle design given A resources.

$$Lat_{\mathsf{Asic}}(A) = \sum_{i \in I} Lat_i(a_i), \sum_{i \in I} a_i \le A$$
(1)

Max T Given A. Let $Tput_{Asic}(A)$ be the throughput of the ASIC-style design given A resources.

$$Tput_{\mathsf{Asic}}(A) = \min(\{Tput_i(a_i) \mid i \in I\}), \sum_{i \in I} a_i \le A \quad (2)$$

C. Ignoring PR Time: PR-Style Performance Bounds

Ignoring PR time, we first derive the lower and upper bounds on the latency and throughput, respectively, achievable by any PR-style design presented in the next subsections. The

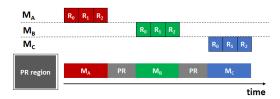


Fig. 4: Example of serialized execution in a PR-style design with one PR region when batching (B = 3).

simplest and most efficient execution strategy is to schedule tasks serially on one PR region. Each module runs once before the PR region is reconfigured with the next module. In the best-case scenario, the PR region is of size A and the highest performance variant using A resources exists for all modules. **Min L Given A.** Let $Lat_{PR,1,min}(A)$ be the lower bound on latency for the PR-style design with one PR region.

$$Lat_{\mathsf{PR},1,\min}(A) = \sum_{i \in I} Lat_i(A) \tag{3}$$

Max T Given A. Let $Tput_{\mathsf{PR},1,\mathsf{max}}(A)$ be the upper bound on throughput for the PR-style design with one PR region.

$$Tput_{\mathsf{PR},1,\mathsf{max}}(A) = \frac{1}{\sum\limits_{i \in I} \frac{1}{Tput_i(A)}}$$
(4)

D. Including PR Time: Serialized Execution on one PR Region

When accounting for PR time and scheduling tasks serially on one PR region, each module runs once before the PR region is reconfigured with the next module. Given N tasks, the PR region is reconfigured N times. Compute and reconfigurations are serialized.

Min L Given A. Let $Lat_{PR,1}(A)$ be the latency of the PR-style design with one PR region.

$$Lat_{\mathsf{PR},1}(A) = \sum_{i \in I} Lat_i(a_i) + N \times Time_{PR}(A)$$
(5)

Scheduling tasks serially on one PR region of the largest size may not result in the design's minimum latency. Though using larger variants leads to a decrease in compute time, it also has the effect of increasing PR time, which may offset the speedup benefit of larger variants. In the next subsection, we discuss a scheduling alternative where compute and reconfigurations are overlapped.

Max T Given A: Batching to Amortize PR Time. Let $Tput_{PR,1}(A)$ be the steady-state throughput of the PR-style design with one PR region.

$$Tput_{\mathsf{PR},1}(A) = \frac{1}{\sum\limits_{i \in I} \frac{1}{Tput_i(a_i)} + N \times Time_{PR}(A)}$$
(6)

If PR time is non-trivial compared to compute time, we can amortize PR time by executing each module B times (i.e. batching B runs) before reconfiguring the PR region (Figure

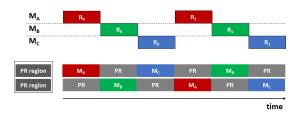


Fig. 5: Interleaved execution on two PR regions. PR time can be hidden by overlapping compute and reconfiguration.

4). Let $Tput_{PR,1}(A)$ be the steady-state throughput of the PR design with one PR region when batching runs.

$$Tput_{\mathsf{PR},1}(A) = \frac{B}{\sum_{i \in I} \frac{B}{Tput_i(a_i)} + N \times Time_{PR}(A)}$$
(7)

Batching allows us to reduce the ratio of total PR time to total compute time at a greater resource cost to buffer intermediate results. Given enough buffering capacity, PR time can be almost totally amortized for large enough B.

E. Including PR Time: Special Cases

Min L Given A: Interleaved Execution on Two PR regions. When optimizing for latency, interleaving task execution on multiple PR regions allows us to overlap reconfigurations and compute to hide PR time, which may result in better latency than serializing task execution on one PR region. Figure 5 shows an example of interleaved execution for k = 2. In this example, $Time_{PR}(A/2) = Lat_i(a_i), \forall i \in I$. By overlapping compute and reconfigurations, PR time is completely hidden. Having k > 2 may be beneficial provided that multiple PR regions can be reconfigured simultaneously. Simultaneous reconfiguration of multiple PR regions is not supported from a user standpoint using current FPGA tools and PR flow. In this paper, we only consider the case where k = 2, and define $Lat_{PR,2}(A)$ as the latency of the PR-style design with two PR regions.

$$Lat_{\mathsf{PR},2}(A) = \sum_{i \in I} \max(Time_{PR}(A/2), Lat_i(a_i))$$
(8)

Max T Given A: Serialized Execution on k PR regions. When optimizing for throughput, it is generally preferable to choose the smallest k to reduce a design's complexity in terms of buffering management since each PR region requires its own intermediate buffer. A k-PR region solution should be considered when appropriately large module variants are not available for all modules in a single PR region solution.

When having multiple PR regions executing in parallel (similar to k-way SIMD), task execution can be serialized on each PR region of size A/k. On each PR region, each module runs once or multiple times before the PR region is reconfigured. Let $Tput_{\mathsf{PR},1}(A/k)$ be the steady-state throughput of a single PR region of size A/k and $Tput_{\mathsf{PR},k}(A)$ be the steady-state throughput of the PR-style design with k PR regions. Assuming that k reconfigurations can occur simultaneously,

$$Tput_{\mathsf{PR},\mathsf{k}}(A) = k \times Tput_{\mathsf{PR},\mathsf{1}}(A/k) \tag{9}$$

As explained previously, only one reconfiguration can happen at a time using current tools. The above throughput can still be achieved by offsetting the start of compute on each PR region by a sufficient number of PR times to ensure that two PR regions are not reconfigured simultaneously.

F. Memory Requirements in PR-style designs

In this section, we discuss the buffering and memory bandwidth requirements of a PR-style design. Compared to an ASIC-style design, a PR-style design requires additional buffering capacity for batching and additional external memory bandwidth when faster module variants are used. A module variant is faster if it uses more resources and/or operates at a higher clock frequency. For the **Max T Given A** problem, we also model the impact of limited memory bandwidth on throughput.

Buffering Requirement. In a PR-style design, each PR region requires two intermediate buffers to hold its intermediate input and output data. The intermediate buffers can be stored in on-chip or off-chip memory depending on the data size. The on-chip buffering option is preferred to minimize the latency and power/energy for data movement. In practice, when batching to amortize reconfiguration time, the buffering capacity required by a PR-style design exceeds the amount of on-chip memory available on current FPGAs (few MBs on large FPGAs). The amount of data to buffer can range from tens to hundreds of MBs depending on the use-case.

If the intermediate buffers are stored in on-chip memory, additional architecture support is needed so that the output of the upstream module stored on chip is used as the input to the next module. One possible solution if to design an intermediate on-chip memory controller to connect the PR region to the intermediate buffers instead of having static, direct connections between the PR region and the buffers. The on-chip memory controller fetches the data from the appropriate intermediate buffer to send to the PR region, and writes the output from the PR region to the appropriate buffer.

Max T Given A: Memory Bandwidth Requirement. When maximizing throughput given an area budget, the best strategy is to serialize module execution on one PR region. An upper bound on the memory bandwidth required by the PR-style design can be determined by considering the read and write bandwidth required by the fastest variant in the design i.e. the variant with the highest throughput.

When the memory bandwidth required by the variant is greater than the total memory bandwidth available in the system, the variant throughput is going to be degraded by some factor proportional to the memory bandwidth required. We introduce a scaling factor F to model the impact of limited memory bandwidth on a variant's throughput. F is equal to the ratio of memory bandwidth required by the variant to the memory bandwidth available in the system if the bandwidth required by the variant is greater than the bandwidth available. Otherwise, F is equal to 1. Let $Tput_{i,peak}(a_i)$ be the peak throughput of the module variant that accelerates task_i, BW_i the bandwidth requirement of the variant, and BW_{total} the total bandwidth available in the system.

$$Tput_{i}(a_{i}) = F \times Tput_{i,peak}(a_{i}), F = \begin{cases} BW_{i}/BW_{total}, & \text{if } BW_{i} > BW_{total} \\ 1, & \text{otherwise} \end{cases}$$
(10)

V. EXPERIMENTAL SETUP

We develop three compute-bound applications representative of real-world applications with cost constraints [44], [45], [46]. For all studies, we use a low-end FPGA board (Ultra96 v2) with a XC7ZU3EG Zyng part that has 70,560 LUTs, 216 BRAMs and 360 DSPs. These studies serve as concrete examples of ASIC-style designs with under-utilization (due to module dependencies or modules having mismatched throughput). Each application consists of three dependent tasks, with some tasks being more compute intensive than others, which perform common vision processing such as detection or classification. Dependent modules share data through external memory since the amount of on-chip memory on the Ultra96 is not sufficient to hold the inter-module buffers in on-chip memory. Note that having more tasks per application would favor PR-style designs, since the length of the dependency chain would increase. In other words, we choose to focus on more challenging design scenarios (shorter pipelines).

Design Scenario. In the studies, we solve the **max T given A** and **min L given A** problems from Section IV, and also consider the problem of minimizing area given a latency upper bound, which we refer to as **given L min A**. Using our model, we search the design space to find the best-achievable ASIC-style and PR-style designs for a given problem. The best-achievable design consists of the set of module variants resulting in the design's maximum throughput, minimum latency or minimum area possible given the module variants available. We use Vivado 2019.1 to build our designs [47].

PR-Style Designs. We consider three possible PR-style designs: (1) P_1 with a single large PR region on which tasks are scheduled sequentially, (2) $P_{1,s}$ with a single smaller PR region (one PR region of P_2) on which tasks are scheduled sequentially, and (3) P_2 with two almost equally-sized PR regions on which tasks are executed in an interleaved fashion. Table I reports the resource utilization of P_1 and P_2 (the PR region of $P_{1,s}$ has the same size as PR region 1 of P_2) on the Ultra96 v2 board at 150 MHz. In both designs, most resources on the Ultra96 v2 are used for compute. The time to reconfigure a PR region through the processor configuration access port (PCAP) when partial bitstreams are stored in external DDR is 12 ms (partial bitstreams of 5.5 MB for P_1) and 6 ms (partial bitstreams of 2.8 MB for P_2). We use one ARM core to manage the operation of the fabric at runtime (i.e. reconfiguration of the PR regions and module execution). PR bitstreams are stored into on-board external DDR.

When optimizing for latency, we report the latency of P_1 , $P_{1,s}$, and P_2 whenever possible. We refer to latency (or frame latency) as the time to process one input frame by the application, i.e. the time it takes for each module to run once.

TABLE I: Resource utilization of the two PR-style designs P_1 and P_2 post place & route on the Ultra96 v2 board at 150 MHz. In both designs, most resources are spent for compute. In P_2 , the PR regions are almost equally-sized.

		P_1	(1 PR region)		P_2	(2 PR regions)	
	I/O infrastructure	PR region	Total	I/O infrastructure	PR region 0	PR region 1	Total
LUT	3366 (4.8%)	61,920 (87.8%)	65,286 (92.5%)	5231 (7.4%)	28,800 (40.8%)	30,240 (42.9 %)	64,271 (91%)
BRAM36Kb	0	198 (91.7%)	198 (91.7%)	0	108 (50%)	108 (50%)	216 (100%)
DSP	0	288 (80%)	288 (80%)	0	144 (40%)	216 (60%)	360 (100%)
PR time (ms)	N/A	12	N/A	N/A	6	6	N/A

TABLE II: Resource utilization, average memory bandwidth, and throughput of the ASIC-style design and the module variants used post place & route on the Ultra96 v2 board at 150 MHz for the activity recognition study.

		Module variants			ASIC-style	
	hog	cnn	lstm	I/O Infrastructure	Modules	Total
LUT	15,495 (22%)	14,614 (20.7%)	7715 (10.9%)	6082 (8.6%)	37,824 (53.6%)	43,906 (62.2%)
BRAM36Kb	34 (15.7%)	92 (42.6%)	80.5 (37.3%)	0	206.5 (95.6%)	206.5 (95.6%)
DSP	64 (17.8%)	10 (2.8%)	7 (1.9%)	0	81 (23%)	81 (23%)
Memory bandwidth (MB/s)	23.6	42.7	3.3	N/A	N/A	64.6
Throughput (fps)	30	16	271	N/A	N/A	16

When optimizing for throughput, we report the throughput of P_1 for different batch sizes *B*. In the context of our studies, the input to an application is a frame. When B > 1, the module processes *B* frames before the PR region is reconfigured.

Performance Density. In addition to latency and throughput, we also compare the performance density of ASIC-style and PR-style designs. Performance density is defined as the number of frames processed per unit time per unit area. This metric quantifies how efficiently a design utilizes available resources. The higher the performance density, the more area-efficient the design is (less under-utilization in the area-time volume). Since there is no simple definition for area on an FPGA, we consider the resources used by the bottleneck resource as a proxy for area. For instance, if BRAM is the bottleneck as it is the case in our studies, performance density is computed as the number of frames processed per unit time per BRAM. For latency, we divide 1/latency by the number of BRAM used in the design. For throughput, we simply divide throughput by the number of BRAM used in the design.

Module Characterization. In the studies, we use six modules: hog [48], cnn [49], lstm [50], viola [51], flow [52], and stereo (developed in-house). Each module has up to three implementation variants generated with Vivado HLS 2019.1 [53]. The variants are provided by the module developer or obtained by changing parameters in the HLS source code, such as the number of compute engines, the data precision, and the on-chip buffering size. The modules' interfaces are modified to conform to our PR region interfaces. In our studies, all PR regions have the same interfaces, namely, one AXI memorymapped, one AXI-lite, a clock, a reset, and an interrupt. All data transfers, including data sharing between modules in the ASIC-style design, happen through external DRAM.

Modules operate on 256×256 frames, except for the lstm module which operates on 32×32 frames. Modules process one frame at a time. Therefore, frame latency is the inverse of throughput, and includes both compute and data movement TABLE III: Resource utilization, throughput and frame latency of the variants used in P_1 .

	hog	cnn	lstm	stereo	flow	viola
LUT	55,635	27,573	47,745	51477	40,509	42,283
BRAM36Kb	109	180	144	96.5	195	91.5
DSP	114	11	13	0	49	101
Throughput (fps)	116	32	2.1k	240	180	41.3
Frame latency (ms)	8.6	31.2	0.48	4.2	5.6	24.2

TABLE IV: Resource utilization and frame latency of the variants used in P_2 .

	hog	cnn	lstm	stereo	flow
LUT	27,879	15,009	7461	23,551	20,106
BRAM36Kb	53.5	92	80.5	96.5	95.5
DSP	114	11	13	0	48
Frame latency (ms)	17.9	62.5	0.87	8.3	11.1

time. Data movement accounts for no more than 15% of the end-to-end latency. For all variants, module throughput scales mostly linearly with its resources. The bottleneck resource for all modules is either LUTs or BRAM on the Ultra96 v2.

A. Model Validation: Case Study Results

In this section, we illustrate how to use our model and validate its effectiveness in three case studies. We show that (1) our first-order model allows to accurately estimate a design's throughput and latency. (2) Our analysis helps determine the most suited PR execution strategy for a problem. Notably, when optimizing for latency, it is important to evaluate both PR execution strategies (serialized execution on one PR region and interleaved execution on multiple PR regions) to find the best one for a given problem. (3) PR-style designs improve performance and performance density upon ASIC-style designs with under-utilization. (4) Given an area budget, if the ASIC-style design is too big to fit, using PR can help make the design fit and run at useful performance.

Study 1: Activity Recognition. The first case study performs activity recognition and is based on [44]. Three dependent

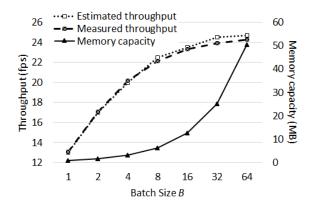


Fig. 6: Throughput of P_1 vs. B for the first case study.

tasks are accelerated by a hog, a cnn and a lstm modules. This study explores the **max T given A** and **min L given A** problems. In this study, we explain how to use our model for quick design space exploration. The same methodology is used for the two other studies.

Max T Given A. Table II shows the resource utilization and the throughput of the ASIC-style design and the module variants used. The ASIC-style design's throughput is equal to 16 fps and is limited by the throughput of the slowest module (cnn). The hog and lstm variants are roughly $2\times$ and one order of magnitude faster than the cnn variant, respectively. The amount of computation per frame for the lstm variant is much less than the two other modules. Therefore, the ASICstyle design has under-utilization, and there is opportunity for PR to improve.

Based on our analysis and on module variants available, batched execution on a single PR region solution (P_1) should provide best performance. Figure 6 shows the estimated and measured throughput, and the intermediate buffering capacity required for P_1 vs. batch size B. We use equation 7, measured throughput variants (Table III) and PR time (Table I) to compute these estimations. We observe that (1) as predicted by the model, when B increases, PR time gets amortized, but with diminishing return when $B \ge 32$. (2) For all B, the estimated and measured throughput match within 2.35%. (3) At B = 64, the throughput of the PR-style design is 24.7 fps, which represents a 54.4% improvement over the ASIC-style design. (4) Intermediate buffering capacity linearly increases with B, and is equal to 50.3 MB for B = 64. The intermediate buffers are stored in on-board external memory (on the Ultra96, 2 GB of external DDR is available). The peak external memory bandwidth (read and write) requirement for P_1 is 91.2 MB/s due to the hog module. This represents a 41.2% increase over the ASIC-style design which needs on average 64.6 MB/s (Table II).

The ASIC-style design uses 206.5 BRAMs (95.6% of BRAM resources) and has a performance density of 0.077 fps per BRAM. P_1 uses 198 BRAMs (91.7% of BRAM resources available) and has a performance density of 0.12 fps per BRAM, which represents a 55.8% improvement over the ASIC-style design.

Min L Given A. When optimizing for latency, the ASIC-style

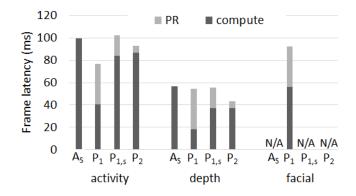


Fig. 7: Frame latency of the ASIC-style design (A_s) and the PR-style designs P_1 , $P_{1,s}$ and P_2 for the three studies.

design has under-utilization since modules are dependent (one frame processed at a time), and therefore, we expect PR to be beneficial. Figure 7.activity shows the frame latency of the latency-optimized ASIC-style design (A_s), and the three PRstyle designs (P_1 , $P_{1,s}$, and P_2). We estimate the latency of A_s using equation 1 and measured module latencies (Table II). The ASIC-style design has an estimated latency of 99.5 ms, which exactly matches our measurement.

We estimate the latencies of the PR-style designs using equations 5 and 8, measured latencies from Tables III and IV, and PR time from Table I. The estimated latencies for P_1 , $P_{1,s}$, and P_2 are 76.6 ms, 102 ms, and 92.4 ms, respectively. The measured latencies for P_1 , $P_{1,s}$, and P_2 are 76.8 ms, 102.2 ms, and 92.6 ms, respectively. We observe that (1) estimated and measured latencies match within 0.26%, and (2) among the three PR-style designs, P_1 has the smallest latency, as predicted by the model (22.8% improvement over the ASICstyle design). Note that PR time accounts for a non-negligible fraction of the frame latency of P_1 (46.9%). However, P_1 still outperforms P_2 , illustrating that the ratio of PR time to compute time should not be considered alone when optimizing for latency.

Considering performance density, A_s uses 206.5 BRAMs and has a performance density of 0.049 per-seconds per BRAM. P_1 uses 198 BRAM and has a performance density of 0.066 per-seconds per BRAM (34.7% improvement over ASIC-style).

Study 2: Depth and Motion Estimation. The second case study performs depth and motion estimation, and is based on [45]. Three dependent tasks are accelerated by a hog, a stereo, and a flow module, respectively. This study explores the **min L given A** problem.

Figure 7.depth shows the frame latency of the latencyoptimized ASIC-style design (A_s), and the three PR-style designs (P_1 , $P_{1,s}$, and P_2). We estimate the latency of A_s using equation 1 and module latencies from Table V. The estimated latency of A_s is 56.7 ms (matches the measured latency). Using the same procedure described in the first case study, we obtain latency estimations for P_1 , $P_{1,s}$, and P_2 of 54.4 ms, 55.3 ms, and 43.3 ms, respectively. The measured latencies for A_s , P_1 , $P_{1,s}$, and P_2 , are 56.7 ms, 54.4 ms, 55.3 ms,

TABLE V: Resource utilization and latency of the ASIC-style design and module variants used post place & route on the Ultra96 v2 board at 150 MHz for the depth and motion estimation study.

		Module variants			ASIC-style	
	hog	stereo	flow	I/O Infrastructure	Modules	Total
LUT	27,244 (38.6%)	13,767 (19.5%)	10,943 (15.5%)	3366 (4.8%)	51,924 (73.6%)	55,320 (78.4%)
BRAM36Kb	52.5 (24.3%)	79.5 (36.8%)	70.5 (32.6%)	0	202.5 (93.8%)	202.5 (93.8%)
DSP	114 (31.7%)	0	44 (12.2%)	0	158 (43.9%)	158 (43.9%)
Frame latency (ms)	17.8	16.7	22.2	N/A	N/A	56.7

and 43.3 ms, respectively. We observe that (1) estimated and measured latencies match within 0.18%, and (2) among all PR-style designs, P_2 has the lowest latency, as predicted by the model (23.6% improvement over the ASIC-style design), reinforcing the fact that using the largest variants available may not achieve minimum latency.

Considering performance density, A_s uses 202.5 BRAMs (93.8% of BRAM resources available) and has a performance density of 0.087 per-seconds per BRAM. P_2 uses 216 BRAMs, and has a performance density of 0.11 perseconds per BRAM (26.4% improvement over the ASIC-style design). Note that $P_{1,s}$ uses only 108 BRAMs while achieving a 2.46% latency improvement compared to A_s . P_1 uses 2× more BRAM but only improves latency by 1.8% compared to $P_{1,s}$. $P_{1,s}$ has a performance density of 0.165 fps per BRAM (92.2% improvement over the ASIC-style design). In a design scenario where area is to be minimized given a latency upper bound of 60 ms, $P_{1,s}$ would be the best design choice.

Study 3: Facial Emotion Recognition. The final study performs facial emotion recognition, and is based on [46]. Three dependent tasks are accelerated by a viola, a cnn and an lstm module, respectively. This study explores the **min L** given A and given L min A problems.

Min L Given A. The BRAM resources on the Ultra96 v2 are insufficient to map A_s , $P_{1,s}$, and P_2 . Figure 7.facial shows the frame latency of P_1 . Using the same procedure as in the first case study, we estimate the frame latency of P_1 to be 92.2 ms. The measured latency is 92.1 ms (0.11% error). P_1 uses 198 BRAMs and has a performance density of 0.055 perseconds per BRAM. In summary, when the ASIC-style design is too big to fit, PR can make the design fit and achieve useful performance (less than 100 ms).

Given L Min A. Given a latency upper bound of 100 ms, we want to estimate the minimum area needed by an ASIC-style design to achieve this requirement. On a larger FPGA board (Ultrascale+ 102), the ASIC-style design consisting of the smallest module variants available uses 65,987 LUTs, 249.5 BRAMs, and 56 DSPs, and achieves a latency of 100.2 ms post place & route at 150 MHz. The performance density of the ASIC-style design is 0.04 per-seconds per BRAM. Considering the PR-style design from **min L given A**, **P**₁ improves latency by 8% and performance density by 27.3% compared to the ASIC-style design.

VI. CONCLUSION

This paper investigates the question of when, how and why FPGA designers should consider using PR. To address this question, we identify reducing under-utilization in ASICstyle designs as one of the main means for improvement available to PR-style designs. We then present a set of PR execution strategies to build efficient PR-style designs that can (1) be faster given an area budget or (2) smaller given a performance bound than ASIC-style designs with underutilization. We discuss our first-order model to quickly and accurately estimate the relative merits of ASIC-style and PRstyle designs in the early stage of design development. We validate our first-order model in three study applications that serve as practical examples of ASIC-style designs with underutilization. Though limited, this choice of execution model and performance metrics allows us to cover a non-trivial range of design scenarios and applications (e.g., video analytics/image processing pipelines, feed-forward neural networks).

The model relies on the existence of a module library consisting of Pareto-optimal module variants used to build the ASIC-style and PR-style designs. The accuracy of the model depends on (1) how well the library has been characterized in terms of area, latency, throughput, and memory bandwidth requirement and (2) the ability to place and route modules at the required clock frequency, which can be challenging depending on the problem. The model could be improved to account for this clock frequency uncertainty, for instance, by defining different levels of confidence based on the design's complexity.

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