DSP-Packing: Squeezing Low-precision Arithmetic into FPGA DSP Blocks

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Abstract—The number of Digital Signal Processor (DSP) resources available in Field Programmable Gate Arrays (FPGAs) is often quite limited. Therefore, full utilization of available DSP resources for the computationally intensive parts of an algorithm is paramount for optimizing the non-functional properties of an implementation (i.e., performance, power, and area). The DSPs available in Xilinx devices implement large bit width operators (i.e. a 48-bit accumulator or a 18×27 multiplier). However, using such a DSP for low-precision quantized data (as is common in image processing or machine learning applications) leaves the DSP resources underutilized. As a remedy, A method has been proposed to pack and compute four 4-bit multiplications on a single DSP in a single clock cycle. This paper presents a generalization of this scheme to arbitrary bit widths and number of multiplications. We also demonstrate that the previously proposed approach leads to errors (Mean Absolute Error (MAE) = 0.37). Furthermore, we explain where these errors come from and how they can be corrected. On top, we introduce a novel approximate method called "Overpacking" which allows to squeeze even more multiplications into a single DSP at the cost of small errors (MAE = 0.47). Overpacking allows to squeeze six 4-bit multiplications into a single DSP compared to just four in the literature. Finally, we introduce an alternative method for packing multiple small-bit width additions into a single 48bit accumulator for use in applications such as Spiking Neural Networks.

Index Terms—Digital Signal Processing (DSP), Field-Programmable Gate Array (FPGA), Approximate Computing.

I. INTRODUCTION

Modern FPGAs have a heterogeneous architecture. They consist of programmable fabric, i.e., Lookup Tables (LUTs) and Flip-Flops (FFs), as well as non-programmable hard blocks like dedicated Digital Signal Processors (DSPs). The micro-architecture of such a DSP-block is vendor-dependent. The DSP48E2 that is present in Xilinx UltraScale FPGAs features a 27 bit preadder, a 18×27 bit multiplier and a 48 bit accumulator [1]. A single DSP48E2 block can implement functions of the form

$$P = B \times (A + D) + C + P_{in} \tag{1}$$

as shown in Fig. 1.

The DSP hard blocks can be used to implement arithmetic circuits that achieve a much better performance (in terms of speed, area and energy efficiency) compared to implementations that use the standard programmable FPGA fabric. Therefore, when designing arithmetic circuits for optimal results, maximal usage of the available DSP blocks is important [2].

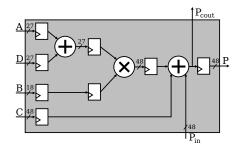


Fig. 1: Schematic architecture and dataflow of the Xilinx DSP48E2.

Since the DSP blocks are a scarce resource on an FPGA chip, it is important to use them as efficiently as possible. This is a problem for small bit width arithmetic, because implementing such a function on a DSP block would leave most of the DSP's resources unused. Applications in the domain of image processing or machine learning typically operate on quantized data with small bit widths of 8 bit or less [3], [4]. To improve the utilization of the DSP's resources for low-precision arithmetic, some techniques have been proposed to map multiple small bit width multiplications to a single DSP [3], [4]. An even better utilization can be achieved when applying Approximate Computing principles. Approximate Computing is an emerging paradigm where nonfunctional requirements like chip area, latency or energy efficiency are traded of for computational accuracy [5], [6]. Our contributions are as follows:

- We generalize the multiplication packing technique proposed by Xilinx Inc. [3], [4] to arbitrary bit widths and arbitrary number of multiplications independent of the DSP's architecture.
- We show how multiplication packing technique proposed by Xilinx Inc. [3], [4] leads to small errors and how these errors can be corrected.
- We present a novel packing strategy called "Overpacking" to squeeze more (logical) values into one (physical) DSP input such that partially incorrect results are produced. We show techniques how the erroneous results can be improved using additional logic. Overpacking allows up to 50% more multiplications on a single DSP compared to the approaches proposed by Xilinx Inc. [3], [4].
- We also present a strategy for packing small bit width additions into the DSPs 48-bit accumulator.

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II. RELATED WORK

Huang et al. [7] propose a method for implementing parallel multiplications on a single DSP slice. On the DSP48E2 that is present on Xilinx UltraScale FPGAs [1], this method allows to implement two multiplications $w_0 \cdot a_0 = r_0$ and $w_1 \cdot a_1 = r_1$ and a multiply-accumulate result $r_2 = w_0 \cdot a_1 + w_1 \cdot a_0$. To achieve maximal utilization, the operands w_0, w_1 must have a bit width of 4 and the operands a_0, a_1 must have a bit width of 5, resulting in a bit width of 4+5=9 for the results r_0, r_1 .

Mert et al. [8] propose a method to map two multiplications $c_0 \cdot a_0 = r_0$ and $c_1 \cdot a_0 = r_1$ to a single DSP. Note that c_0 and c_1 must be constants. Also note that the variable input a_0 is the same for both multiplications. This methods requires the constants to be decomposed into shift operations prior to the synthesis of the circuit. However, in many applications, the multiplication operands change during runtime, rendering the proposed method infeasible.

Kalali and Van Leuken [9] extend the method of Mert et al. [8] by using a table lookup technique for storing the decomposed constants. The lookup table allows the constants to be changed during runtime. In addition, an approximate computing technique is proposed to reduce the large overhead caused by this lookup table.

In the Xilinx white paper [3], a method is proposed to implement two multiplications of the form $w_0 \cdot a_0 = r_0$ and $w_1 \cdot a_0 = r_1$ on a single DSP. In the remainder of this paper, this procedure will be referred to as INT8-packing. Note that the variable input a_0 is the same for both multiplications. In this method, all input operands have a bit width of 8, thus resulting in two 16 bit results. A very similar method is proposed by Lee et al. [10].

In the Xilinx white paper [4], a method is proposed to implement four multiplications of the form $w_0 \cdot a_0 = r_0$, $w_1 \cdot a_0 = r_1$, $w_0 \cdot a_1 = r_2$, $w_1 \cdot a_1 = r_3$ on a single DSP. The input operands w_0, w_1, a_0, a_1 have a precision of 4 bit, thus resulting in four 8 bit results. In the remainder of this paper, this procedure will be referred to as INT4-packing.

III. PRELIMINARIES: INT4-PACKING

To generalize the ideas proposed by Xilinx Inc. [4], we first give an overview over INT4-packing. Here, we also introduce our notation. INT4-packing basically computes the outer product of two vectors **a** and **w**, with both vectors having two elements each:

$$\mathbf{a} \cdot \mathbf{w}^{\top} = \begin{bmatrix} a_0 \\ a_1 \end{bmatrix} \cdot \begin{bmatrix} w_0 \\ w_1 \end{bmatrix}^{\top} = \begin{bmatrix} a_0 w_0 & a_0 w_1 \\ a_1 w_0 & a_1 w_1 \end{bmatrix}$$
(2)

Computing the result of this outer product requires 4 multiplications in total. Using the INT4-approach, these multiplications can be packed on a single DSP if the entries of **a** are unsigned 4 bit integers and the entries of **w** are signed 4 bit integers. The strategy is to rearrange the individual inputs a_0, a_1, w_0, w_1 as described in the following equation:

$$(a_1 \cdot 2^{11} + a_0) \cdot (w_1 \cdot 2^{22} + w_0) = a_1 w_1 \cdot 2^{33} + a_0 w_1 \cdot 2^{22} + a_1 w_0 \cdot 2^{11} + a_0 w_0$$
(3)

Note that multiplications or divisions with 2^n can be implemented by fixed shift operations that only require a rewiring of the individual bits. The computation in Eqn. (3) can be mapped to the DSP48E2 as follows: The operand a_0 is mapped to the B-Port (see Fig. 1) with an offset of 0. a_1 is also mapped to the B-Port but with an offset of 11. This is a hardware-efficient way of implementing $a_1 \cdot 2^{11} + a_0 \cdot 2^0$. Input w_0 is mapped to the preadder port A with an offset of zero. Since w_0 is signed, the sign bit has to be repeated for all Most Significant Bits (MSBs) to perform sign extension. Input w_1 cannot be mapped to the same port as w_0 because it is signed. Therefore, w_1 is mapped to the preadder port D with an offset of 22. The 4 results of the outer product can be extracted from the P-Port. E.g., the result a_1w_1 can be extracted from bit 33 to bit 40 from the P-Port. The individual results are separated by $\delta = 3$ padding bits (see Fig. 2). This is important when multiple DSPs are chained together using the carry ports (P_{in}, P_{cout}) in order to accumulate their results. Thus, with δ bits padding a maximum of 2^{δ} results can be accumulated without error. When no results are accumulated no padding is needed.

IV. GENERALIZATION OF INT4-PACKING: INT-N

The architecture-independent packing INT-N is used to generate a multiplication packing that does not consider the constraints of the target DSP (i.e., limited bit widths and input ports). To generalize the INT4-approach, the multiplication packing technique has to be described in mathematical terms. For the generalization, the integer input vectors $\mathbf{a} = [a_0...a_n]$ and $\mathbf{w} = [w_0...w_m]$ can have any number of entries. A packing configuration can then be described as follows. The offsets of the entries of a and w are stored in the sets a_{off} and w_{off} and the bit widths are stored in $\mathbf{a}_{\mathrm{wdth}}$ and $\mathbf{w}_{\mathrm{wdth}}$, respectively. The bit widths of the individual elements can be chosen arbitrarily, even allowing for cases where the each entry has a different bit width. The result **r** contains the outer product, i.e., $\mathbf{r} = \mathbf{a} \cdot \mathbf{w}^{\top}$. Thus, the sets $\mathbf{r}_{\mathrm{off}}$ contains the offsets and $\mathbf{r}_{\mathrm{wdth}}$ contains the bit widths of the individual results. For example, INT4packing has the following packing configuration (see Fig. 2): Padding $\delta = 3$, $\mathbf{w}_{wdth} = \mathbf{a}_{wdth} = \{4, 4\}$, $\mathbf{r}_{wdth} = \{8, 8, 8, 8\}$, $\mathbf{w}_{\text{off}} = \{0, 22\}, \ \mathbf{a}_{\text{off}} = \{0, 11\}, \ \mathbf{r}_{\text{off}} = \{0, 11, 22, 33\}.$ The offsets of the inputs \mathbf{a}_{off} and \mathbf{w}_{off} determine the offsets of the results \mathbf{r}_{off} as described in Eqn. (4) (with $|\cdot|$ denoting the cardinality).

$$\begin{pmatrix}
\left|\mathbf{a}_{\text{off}}\right|^{-1} \\
\sum_{i=0}^{i} a_{i} \cdot 2^{\mathbf{a}_{\text{off},i}}
\end{pmatrix} \cdot \left(\sum_{j=0}^{|\mathbf{w}_{\text{off}}|-1} w_{j} \cdot 2^{\mathbf{w}_{\text{off},j}}\right) \\
= \sum_{j=0}^{|\mathbf{w}_{\text{off}}|-1} \sum_{i=0}^{|\mathbf{a}_{\text{off}}|-1} a_{i} w_{j} \cdot 2^{\mathbf{r}_{\text{off},j\cdot|\mathbf{a}_{\text{off}}|+i}} \quad (4)$$

Note that in the equation above, the offsets of the inputs $\mathbf{w}_{\text{off}}, \mathbf{a}_{\text{off}}$ determine the offsets of the results \mathbf{r}_{off} , i.e.: $\mathbf{r}_{\text{off},j\cdot|\mathbf{a}_{\text{off}}|+i} = \mathbf{a}_{\text{off},i} + \mathbf{w}_{\text{off},j}$ This can be understood as a generalization of Eqn. (3). Note that this generalized packing INT-N also applies to INT8 packing.

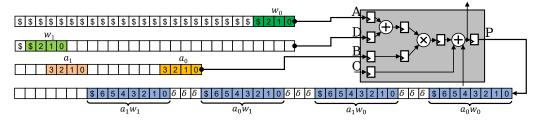


Fig. 2: INT4-packing for performing four parallel multiplications on a single DSP. Here, \$ denotes the (extended) sign bits and δ denotes the padding bits. The offsets of the individual inputs determine the offsets of the individual results as described in Eqn. (3).

V. ERROR ANALYSIS OF MULTIPLICATION PACKING

The generalized multiplication packing INT-N (and thus including the the INT4 and INT8 packing technique proposed by Xilinx) suffers from an error where some actual outputs O_{actual} are smaller than the expected outputs O_{expect} . This error is bounded by -1, i.e., $O_{\text{actual}} = O_{\text{expect}} - 1$. The error is introduced by the right-shifting operation that is implicitly performed when extracting the results from the bit string. The individual results $a_i w_j$ are extracted from the result vector by right shifting. The reasoning behind this is that

$$x \gg n = \frac{x}{2^n} \tag{5}$$

However, right shifting *signed* integers implements division that is always rounding down i.e.:

$$x \gg n = \left\lfloor \frac{x}{2^n} \right\rfloor \tag{6}$$

This biases the output towards negative infinity. For INT4packing, this leads to an error rate of around 37% over all possible input combinations.

We propose two error correction schemes: one method for full error correction requiring extra hardware (LUTs, FFs) and one approximate method that reduces the error probability from 37% to 3% and requires no additional hardware.

A. Full Error Correction

Since the errors are related to rounding, they can be fixed by applying the correct rounding. The correct rounding should implement rounding that does not introduce a bias. For this, rounding to the nearest integer is used. This rounding scheme can be implemented using the Round-Half-Up function:

$$round_half_up = |x + 0.5|$$
(7)

For example, 3.1 gets rounded to 3, and 3.6 gets rounded to 4. The advantage of this function is that it can be implemented easily in hardware by checking a single bit. To implement the Round-Half-Up function, the cases where the result needs to be rounded up have to be determined, because rounding down is done by default. For this, the results can be interpreted as fixed-point numbers:

- If the first bit behind the decimal point is 1, then round up by adding 1 to the result.
- Else, round down by adding a 0 (i.e. do nothing).

Full error correction requires additional hardware resources for implementing the required adders (see Fig. 3).

B. Approximate Correction

The idea is to anticipate if the first bit after the decimal point is 1 (thus requiring rounding up) and then adding a 1 to the result *before* extracting to result. The proposed solution works as follows. The assumption is that a contains unsigned entries and w contains signed entries. The first bit after the decimal point of the *n*'th result located at $\mathbf{r}_{off,n}$ is 1 if the sign of the result located at $\mathbf{r}_{off,n-1}$ is negative (due to the sign bits). The ideas is then that the sign of a result located at $\mathbf{r}_{off,n-1}$ can be anticipated by checking the sign of the operands. Thus, adding the sign bit of the operands that generated the result located at $\mathbf{r}_{off,n-1}$ resolves some of the errors. This addition can be performed using the DSP's accumulator that is accessed through the C-Port (see Fig. 4). In some rare cases, this does not resolve the errors, e.g. when one operand is zero.

VI. OVERPACKING

In the domain of digital signal processing, many applications do not require computations to be exact. Reducing computational accuracy often allows for improvements on energy efficiency, resource utilization or execution speed [11]. If approximation is acceptable and to what degree depends on the application. Typical applications are in the domain of image processing and machine learning, since the underlying algorithms in these domains are often of an approximate nature themselves. The general idea for approximate multiplication on DSPs is to reduce the amount of padding bits δ below the minimum. If δ is reduced below the minimum, some bits of the individual results are being merged together and errors occur. The benefit of this technique is that more multiplications with a higher bit precision can be fitted on a single DSP block. The minimum required amount of δ -bits is determined by how many results are supposed to be accumulated. For easier interpretation of the results, Overpacking experiments have been performed with no accumulation of results. Therefore, the minimum padding is $\delta = 0$. Thus, Overpacking can be introduced by setting $\delta = -1, -2$, etc.

A. Errors introduced by Overpacking

For Overpacking, the individual results are separated by less δ -bits than required. Thus, the individual results $a_i w_j$ overlap. The mathematical operation that fuses the overlapping results to the final output vector P is an addition (according to Eqn. (4)). This has the effect that the LSBs of a results r_1

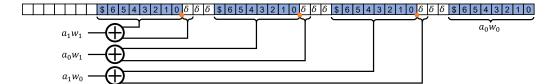


Fig. 3: Hardware circuit for implementing the round half up function using additional hardware. The orange dots denote the imaginary decimal points of the results that have to be extracted.



Fig. 4: 48-Bit correction term that is fed into the DSP's accumulator port C for the approximate error correction technique. Shown here for INT4 packing.

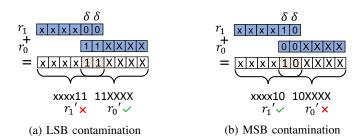


Fig. 5: Errors introduced by Overpacking. The result r_1 and r_0 overlap because of the negative padding $\delta = -2$. r'_1 and r'_0 are the corrupted results extracted from the output vector. X and x denote don't care bits of r_1 and r_0 , respectively.

located left of a result r_0 affect the MSBs of r_0 . For example, Fig. 5a shows how non-zero MSBs of r_0 contaminate the LSBs of r_1 . Fig. 5b shows how non-zero LSBs of r_1 contaminate the MSBs of r_0 . An approximate computing technique where the MSBs of a result are contaminated leads to very high errors and is therefore not desirable. We present a technique to correct these errors with very little hardware overhead.

B. MR-Overpacking

Most Significant Bit Restoring (MR) Overpacking is an improvement to the naive Overpacking technique introduced above. The idea of MR-Overpacking is to let the MSBs get contaminated (Fig. 5b), but to restore the MSBs after extraction. The reasoning behind this is: erroneous MSBs lead to a high error, erroneous LSBs are not having a large impact on the result. To restore the MSBs, the inverse process of the MSB contamination must be performed. As illustrated in Fig. 5b, δ MSBs of a result r_n that is located at $\mathbf{r}_{\text{off},n}$ are contaminated by adding δ LSBs of another result r_{n+1} that is located at $\mathbf{r}_{\text{off},n+1}$. Thus, the MSB contamination is an *addition* which can be inverted using a substraction. MR-Overpacking restores the δ MSBs of a result $\mathbf{r}_{\text{off},n}$ by substracting the δ LSBs of $\mathbf{r}_{\text{off},n+1}$. To perform the restoration, the contaminating LSBs have to be known. Therefore, the contaminating LSBs must be calculated. The first LSB (Eqn. (8)) and the second LSB (Eqn. (9)) of a result can be calculated with a little hardware overhead. Eqns. (8), (9) are simply the rules for binary multiplication.

$$a_i w_j[0] = a_i[0] \wedge w_j[0] \tag{8}$$

$$a_i w_j[1] = (a_i[0] \land w_j[1]) \oplus (a_i[1] \land w_j[0])$$
(9)

Consider the following example where $\delta = -2$, $a_0 =$ $1010_2 = 10_{10}, a_1 = 0011_2 = 3_{10}, w_0 = 1001_2 = -7_{10},$ $w_1 = 1100_2 = -4_{10}$, with w_0, w_1 being signed integers in 2's complement notation. For Overpacking, set $\delta = -2$. The expected result for a_0w_0 would be $1011 \ 1010_2 = -70_{10}$. However, due to Overpacking, $a_0 w'_0 = 0111 \ 1010_2 = 122_{10}$. The two LSBs of a_1w_0 that corrupt a_0w_0 are calculated using Eqn. (8), (9): $a_1w_0[0] = a_1w_0[1] = 1$. The correction is performed by subtracting the corrupting LSBs : $a_0 w_0 =$ $a_0w'_0 - 1100\ 0000_2$. Fig. 6 shows how this scheme can be implemented with extra hardware (LUTs and FFs). Note that this scheme must be adapted according to δ . For example, if $\delta = -1$, only the implementation of Eqn. (8) is required. When δ is increased further, the respective LSBs must be calculated according to the rules of binary multiplication. For example, setting $\delta = -4$ requires the calculation of the first four LSBs. Note that the hardware cost for implementing the correction logic increases exponentially with the number of LSBs.

The catch of the proposed scheme is as follows. Multiplication is very expensive in terms of hardware resources with two exceptions: the first and the second LSBs are very cheap to implement (see Eqns. (8), (9)). This means, that the expensive multiplication is performed in the optimized DSPs, the correction of corrupted MSBs is cheap to implement with additional hardware. The corruption of the LSBs only leads to small errors, as will be discussed in Section VIII.

VII. ADDITION PACKING

In Spiking Neural Networks (SNNs), the main computational operation is an addition [12], [13]. In contrast, standard Neural Networks (NNs) are based on Multiply-Accumulate operations (MAC) [14]. This means that SNN-accelerators require the implementation of thousands of adders, placing a high load on the FPGA's LUT and FF resources. In the following, we propose a method to pack multiple small-bit

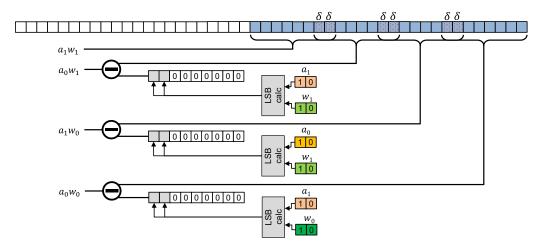


Fig. 6: Hardware circuit for implementing MR-Overpacking with $\delta = -2$. The boxes "LSB calc" implement the Eqns. (8), (9) for the construction of the correction terms that are then subtracted from the extracted results. To obtain this packing, the following setup is used: $\mathbf{w}_{wdth} = \{4, 4\}$, $\mathbf{r}_{wdth} = \{8, 8, 8, 8\}$, $\mathbf{w}_{off} = \{0, 12\}$, $\mathbf{a}_{off} = \{0, 6\}$, $\mathbf{r}_{off} = \{0, 6, 12, 18\}$.

additions into the large 48-bit adders of the DSP48. Consider the example in Fig. 7 where two 8 bit additions are mapped to a single 16 bit addition. One 8 bit addition is mapped to the lower 8 bits and the other 8 bit addition is mapped to the upper 8 bits. The addition in the upper bits is still connected to the addition in the lower bits by the carry chain. Thus, if the addition in the lower 8 bits causes a carry, this carry is propagated to the addition in the upper 8 bits. The propagated carry causes an error in the least significant bit of the upper addition. This has the following implications: a) the addition located in the lower bits never has errors. (b) If a carry occurs from one addition to another, only the least significant bit of a result is corrupted. Therefore, the worst case absolute error is bounded to 1. To completely prevent errors, an extra guard bit with the value of 0 can be added between all additions. This guard bit is used to prevent that a carry signal can propagate from one addition to another (as illustrated in Fig. 8). This guard bit is additional overhead as it cannot be used for addition. This scheme can be generalized to different bit widths and more additions. The DSP48 features a 48-bit adder. For example, five 9 bit adders can be packed into a single DSP leaving room for three guard bits. Therefore, only a single adder is approximating in the sense that some results may have errors. To maximize the utilization, two 9-bit adders and three 10-bit adders can be mapped to a single DSP, leaving no space for guard bits.

VIII. EXPERIMENTS AND RESULTS

To analyze the techniques and their errors described in the previous chapters, the following error metrics are used to compare an an expected output O_{expect} to an actual output O_{actual} [15]. All N possible input combinations were tested.

$$EP = \frac{\sum_{\forall n: O_{expect}}^{N} \neq O_{actual}^{(n)}}{N} \cdot 100\%$$
(10)

$$MAE = \frac{1}{N} \cdot \sum_{n=1}^{N} \left| O_{\text{actual}}^{(n)} - O_{\text{expect}}^{(n)} \right|$$
(11)

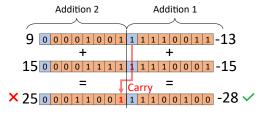


Fig. 7: Strategy for packing two small bit with additions to a large one. Shown is the origin of the error where the carry signal of addition 1 propagates to the least significant bit of addition 2.

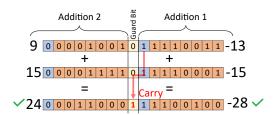


Fig. 8: Addition packing with no errors using a guard bit between the individual additions. The guard bit "catches" the carry signal and prevents it from propagating to addition 2.

WCE =
$$\max_{\forall n} \left| O_{\text{actual}}^{(n)} - O_{\text{expect}}^{(n)} \right|$$
 (12)

Note that the error statistics listed above are calculated for each result $a_i w_j$ individually. The result calculated over all individual results is indicated by a bar accent (e.g., MAE). To evaluate the hardware cost of the individual circuit implementations, each circuit was implemented on the the Xilinx Zynq UltraScale+ MPSoC (XCZU7EV-2FFVC1156). For best comparability with the related INT4-approach by Xilinx, all

TABLE I: Results of the various presented multiplication packing approaches, compared to the approach proposed by Xilinx [4]. All operands are 4-bit with four multiplications on a single DSP.

Approach	MAE	$\overline{\mathrm{EP}}$	$\overline{\mathrm{WCE}}$	LUTs	FFs
Xilinx INT4 [4]	0.37	37.35%	1	0	0
INT4 Full Correction	0.00	0.00%	0	27	32
INT4 Approx. Correction	0.02	3.13%	1	0	0
Overpacking $\delta = -1$	24.27	49.85%	129	0	0
Overpacking $\delta = -2$	37.95	58.64%	194	0	0
Overpacking $\delta = -3$	45.53	78.26%	228	0	0
MR-Overpacking $\delta = -1$	0.37	37.35%	1	4	6
MR-Overpacking $\delta = -2$	0.47	41.48%	2	6	20
MR-Overpacking $\delta = -3$	0.78	49.95%	4	17	30

TABLE II: Detailed error statistics of the individual results $a_i w_j$ for INT4 Packing and MR-Overpacking.

	INT4 Packing			MR-Overpacking $\delta = -2$			
Result	MAE	EP	WCE	MAE	EP	WCE	
a_0w_0	0.00	0.00%	0	0.00	0.00%	0	
a_1w_0	0.47	46.87%	1	0.60	52.34%	2	
a_0w_1	0.50	49.80%	1	0.64	55.41%	2	
a_1w_1	0.53	52.73%	1	0.66	58.20%	2	
for all $a_i w_j$	0.37	37.35%	1	0.47	41.48%	2	

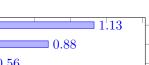
TABLE III: Results of the addition packing scheme.

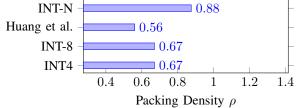
Approach	MAE	EP	WCE	LUTs	FFs
Addition Packing	0.51	51.83%	1	0	0

tests in Table I and II have been performed with 4-bit operands and four multiplications. Note that the approaches introduced in this paper can be generalized to arbitrary bit widths and number of multiplications, restricted only by the DSPs architecture. Table III shows the result of a single 9-bit adder that is implemented along with four other 9-bit adders in a single DSP using the addition packing scheme without guard bits. To measure the effectiveness of the different packing schemes, we introduce the packing density $\rho = b_{used}/b_{total}$, where b_{total} is the number of output bits (e.g., 48 bits for the DSP48) and b_{used} is the number of bits that are occupied by the multiplication results. Fig. 9 compares the multiplication packing density for the different approaches. To evaluate INT-N, the following packing configuration is used: Padding $\delta = 0$, $\mathbf{w}_{wdth} = \{3, 3\}$ $\mathbf{a}_{wdth} = \{4, 4, 4\}, \ \mathbf{r}_{wdth} = \{7, 7, 7, 7, 7, 7\}, \ \mathbf{w}_{off} = \{0, 21\},$ $\mathbf{a}_{\text{off}} = \{0, 7, 14\}, \ \mathbf{r}_{\text{off}} = \{0, 7, 14, 21, 28, 35\}.$ The packing configuration for Overpacking is: $\delta = -2$, $\mathbf{w}_{wdth} = \{5, 5\}$ $\mathbf{a}_{wdth} = \{4, 4, 4\}, \ \mathbf{r}_{wdth} = \{9, 9, 9, 9, 9, 9\}, \ \mathbf{w}_{off} = \{0, 21\},$ $\mathbf{a}_{\text{off}} = \{0, 7, 14\}, \mathbf{r}_{\text{off}} = \{0, 7, 14, 21, 28, 35\}.$ Note that many more configurations for INT-N and Overpacking are possible (Eqn (4)), that can be adapted according to the application at hand.

IX. CONCLUSION

DSP-Packing offers a way to effectively use DSPs for small width multiplications. The INT4-approach as proposed by Xilinx [4] for multiplication packing has multiple limitations. First, the bit widths of the individual multiplications and the





Overpacking

Fig. 9: Multiplication packing density for different techniques.

amount of operands is fixed. The padding is δ is also fixed to 3 and it introduces a rounding-related error. We showed that this technique can be generalized to arbitrary packings. While the rounding error introduced by INT4-packing is relatively small (MAE = 0.37), it adds a small bias towards negative infinity to the results which might be an issue for some applications. The full error correction requires the implementation of additional adders, introducing an overhead as additional resources are required. Approximate error correction uses the internal accumulator of the DSP48E2, requiring no external hardware. The error that is still present is very small (MAE = 0.02) making approximate error correction an ideal solution. Overpacking can be used to improve the utilization of DSP blocks significantly. Overpacking itself introduces a very large error since the MSBs of the extracted results are corrupted. MR-Overpacking reduces the error significantly with a very small hardware overhead. This makes MR-Overpacking an interesting solution, for example for Convolutional Neural Networks (CNNs), because they are inherently resilient to quantization and approximations. For example, MR-Overpacking can be used to map 6 individual 4-bit multiplications on a single DSP48E2, allowing 50% more 4-bit multiplications compared to INT4-packing while achieving the same MAE = 0.37. MR-Overpacking can also be used to increase the precision of multiplications. For example, setting $\delta = -2$ allows 4 individual 6-bit multiplications on a single DSP, resulting in an increase in bit precision of 50% compared to INT4-packing. In the future, we plan to explore methods to dynamically change the DSP packing during runtime according to the requirements of the computational task at hand.

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