Keynote Lecture I

Recent Advances in Die Stacking and 3D FPGA

Arifur Rahman

Altera, USA

ABSTRACT

Die stacking technology with high-bandwidth interconnect is enabling new product architectures and capabilities. Although 3D integration, where TSVs are incorporated in active device layers, is the Holy-Grail of die stacking, the early phase of technology adoption is driven by passive silicon interposer (2.5D) based integration scheme or some variants of it. This presentation will provide an overview of recent advances in die stacking and FPGA application trends which are driving the need for stacking technologies. I will present some of the industry challenges in technology integration and design infrastructure and how they are being addressed to enable broader technology adoption.

Arifur Rahman is an Architect at Altera, where he led Product Architecture team and currently leads FPGA based System in Package product development. He has more than 15 years of research and product development experience in circuits and architecture, design methodology, manufacturing technology, and supply chain strategy. His expertise includes all aspects of advanced die stacking, from technology development to design methodology and product architecture. He incubated and productized silicon interposer based FPGAs at Xilinx and co-invented stacked silicon interconnect (SSI) products. Prior to Altera, he worked at Xilinx, Agere Systems, Lattice Semiconductor, and Polytechnic University, NY. Arif holds a PhD degree from MIT in Electrical Engineering and an MBA from Santa Clara University. He has authored numerous articles and has been granted 56 patents. He serves in the program committee of IEEE Custom Integrated Circuits Conference (CICC) and was the Co-Chair of the 9th International RTI 3-D Architectures for Semiconductor Integration and Packaging conference in 2012. He is a senior member of IEEE.