Keynote Lecture II

Reconfigurable chip Advantage compared with GPGPU from the compiler perspective

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ABSTRACT

This presentation discusses how FPGA or coarse grained reconfigurable processor is superior to CPU/GPGPU from the view point of C compiler. Initially, we introduce the architectural characteristic of CPU, GPGPU and fine grained and coarse grained reconfigurable process with FSM+Datapath model. Then, we explain what kind of applications can be accelerated with "FPGA and C-based High Level Synthesis Tool" better than GPGPU according to the compiler techniques (freedom of compiler parallelization).

Kazutoshi Wakabayashi received his B.E. and M.E. degrees and Ph.D from the University of Tokyo in 1984, 1986 and 2006. He was a visiting researcher at Stanford University during 1993 and 1994. He joined NEC Corporation in Kawasaki Japan in 1986 and he is currently a Senior Principal Researcher of Central Research Labs. NEC Corporation. Dr.Wakabayashi has been engaged in the research and development of VLSI, CAD systems; high-level and logic synthesis, formal and semi-formal verification, system-level simulation, HDL, emulation, HLS and floorplan links, and reconfigurable computing. He served on executive committee or organizing committee of some international conference including: ASP-DAC'09 General Chair, CODES+ISSS'09 Co-Technical Program Chair. a Secretary of Steering Committee of ASPDAC, and Executive Committee for ICCAD and DAC, Tutorial Chair of ASPDAC2006, Steering Committee of ITC-CSCC (09-). He has served on the program committees for several international conferences including: DAC, ICCAD, DATE, ASP-DAC, ISSS, SASIMI, and ITC-CSCC, ISCAS, VLSI-TSI, SBCCI, VLSI Design, ESS, ISLP and so on. Also, he has served as a general chair, a secretary, and a Technical Program Committee member for a number of Japanese conferences, including: Institute of Electronics, Information and Communication Engineers of Japan (IEICE), the Information Processing Society of Japan (IPSJ), System LSI WS, Karuizawa WS. He is currently chair of SIG on VLSI design methodology of IEICE, and elected member of IEICE. He was an associate editor of Transactions on IEICE on VLSI CAD, DAEM. He is a rep. of CEDA (Council for EDA) of IEEE. He is also a member of IEEE, IPSJ, and IEICE. He received the IPSJ Kiyasu Special Industrial Achievement Award 2011, the Yamazaki-Teiichi Prize in 2004, and the IPSJ Convention Award in 1988, Sakai Kinen Special Award in 2001, and the NEC Distinguished Contribution Award in 1993 for his logic synthesis system and in 1999 for his formal verification, and in 2006 for his High Level Synthesis. His C-based Synthesis and Verification tool suite called "CyberWorkBench" received a Grand prize of "LSI of the Year 2003" and "LSI of the Year 2007".