3D Thermal Model of Power Electronic Conversion Systems for Wind Energy Applications

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***Abstract*— Energy is vital for continual progress of human civilization. Accessing to low-cost, environmental friendly, renewable energy sources are keys to economic future for developing countries and around the globe. Wind energy systems are one of the most adequate option where power electronic converters are used for monitoring and conditioning the energy flow; however operating environmental conditions such as variable wind speed cause temperature fluctuations that derive degradation and failures in these systems. Therefore, proper thermal management and control are necessary to monitor their reliability and lifecycle. Besides, power capacity of these devices is being increased by new technological improvements such as multichip designs. Meanwhile, the heat path through the devices has also become more complex due to the heat coupling effect among several chips and it is not possible to be estimated by conventional methods found in literature. In this paper, a three dimensional finite element model (FEM) is implemented for accurate estimation of thermal profile of a power module. Based on the thermal characteristic obtained by the FEM, an electro thermal model was developed to predict the temperatures of each layer of the power module that cannot be measured during service. The work is essential as it solves massive heat transfer issues and it is important to provide health management of power electronics embedded in wind systems.**

Keywords— Insulated gate bipolar transistor (IGBT); two level converter; electro thermal model; junction temperature; 3D FEM.

I. INTRODUCTION

Wind energy systems are non-polluting source of energy. They do not produce greenhouse gases or other pollutants. Their uses vary from single households to small towns and villages, from local and international businesses to huge wind farms. Nationally and locally owned wind systems decrease reliance on foreign sources of fossil fuels and would bring energy independence to a country [1]. Increase in the number of local wind systems will also help the decrease of load on existing transmission lines since bringing power from far places (i.e. conventional power plant) will not be necessary. On the other hand, variable and unpredictable wind and natural effects still remain an issue for the reliability of these systems [2].

In wind energy applications, power electronic converters are embedded as an interface between wind turbines and utility grid, for monitoring and conditioning of the energy flow (i.e. voltage and frequency regulation) and safety [3]. However, it is well known that failure of these devices is the most frequent cause of loss of generation in wind applications [4, 5]. A recent Wind Energy Update and Maintenance Report [6] states that 66% of the operation and maintenance cost of conversion units at offshore wind farms is due to unscheduled maintenance where the total cost is up to €300,000 per year, per turbine. As stated in [7, 8], estimated lifetime of wind energy conversion system is only 20-25 years because of the unaddressed issues, such as uncertainty of mission profiles, reliability of components, lack of understanding the failure mechanisms [3] and increase in the electronic content and complexity (i.e. heat coupling effects [9]).

The Insulated Gate Bipolar Transistor, IGBT, is one of the semiconductor devices that are operated as switching elements within the conversion unit for interfacing purposes. Temperature and temperature cycling are the major stressors which affect the performance and reliability of these systems. Due to the thermo mechanical effects or long-term exposure to high temperatures [10] caused by variable wind profile, degradation and eventual failures occur. According to [11], almost 60% of failures are temperature induced as seen in Fig. 1 a, and for every 10 °C temperature rise the failure rate nearly doubles in the operating environment.

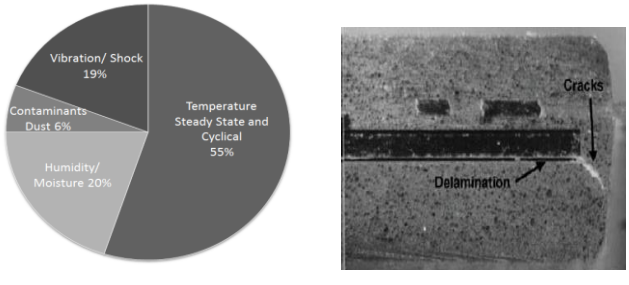


Fig. 1. (a) Stress Distribution over a power electronic system [2] , (b) Solder Failure due to crack [12]

Developing an accurate electro thermal model that provides proper estimation of the temperature profile of the device at various load conditions [12] is very important for reliability prediction and to achieve better performance and proper maintenance [11].

In literature, many thermal models have been proposed by authors [13, 14]. However, they do not represent accurate heat transfer paths of power electronic devices since they contain complex mathematical functions based on numerical convolution [15] in time and frequency domains. The available circuit simulator based models with PLECS [16], and SPICE [17, 18] are only applicable for simple structures, like one directional heat flow, and they cannot be easily adapted for multi-layered devices. Researchers also worked on analytical solutions by using Fourier transform [19], Green's function theorem [20, 21], Fast Fourier transform [22] and Neural Network [23] for heat transfer phenomena of semiconductor devices. These methods cannot be integrated into circuit simulators easily and they are not computationally efficient to be extended as an electro thermal model. Recent developed models [24], based on thermal information supplied in datasheets, are not accurate enough because of the lack of heat coupling effects among adjacent layers. Measurement and estimated temperature data based thermal modelling approaches are also assessed by thermocouples [25], infrared cameras [26], optical fibers [27, 28] and direct measurement of voltage drop [29-32]. Thermal modelling is generally limited to the die and base plate temperatures in such models [33]. IGBT modules contain a number of parallel connected semiconductor dies which are bonded to substrate by solder joints. Aluminum wires are also commonly used as wire-bonds attached to the silicon die surfaces [11]. During operation, heat flux transfers through different paths from die chips to the cooling system. Thermal cycling generates temperature fluctuations within the different layers. This causes stress between the bonded materials and hence it develops fatigue and cracks, and eventually failure due to the different coefficient of thermal expansions [12] as seen in Fig. 1 b. Temperature measurement is difficult for these layers and therefore direct determination of the thermal parameters within the module is impractical. To overcome these challenges, Finite Element models of power devices are developed within commercially available software programs such as ANSYS [9, 34-35] and FLOTHERM [28] to define accurate thermal profile. However, estimation of the dynamic temperature characteristic of the power modules with several chips is challenging because of the thermal coupling effects among the internal layers during operation [9]. A promising modelling approach was proposed in [12, 27] which accounts for heat coupling effects. This approach used a thermal impedance matrix to represent the actual behavior of each internal component of the power modules. The thermal characteristics of the adjacent layers were obtained by FEM in time domain and used in the electro thermal model [36].

The main purpose of this paper is to design an electro thermal model for a power electronic module that is used in wind energy conversion unit applications. The technique applied in this paper analyzes the thermal characteristics of whole module using 3D FEM. In this study, the heat distribution was modelled successfully with discrete time analysis in order to increase accuracy and computational efficiency. The actual module (DIM1200ASM45) which is used for this study and its circuit configuration are shown in Fig. 2 a & b, respectively. It consists of several parallel connected IGBTs and diodes.

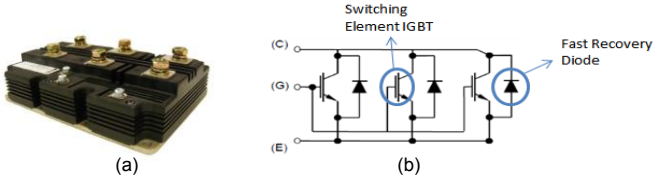


Fig. 2. (a) Physical view and (b)circuit configuration of DIM1200ASM45

II. ELECTRO THERMAL ANALYSES OF POWER MODULES

A. *Energy and Power Loss Modelling*

Developing a proper electro thermal model strictly requires effective power loss calculation and integration of the heat generation represented by internal self-heating and cross coupling effects. Total power loss can be measured over one period of switching processes. It combines both switching and conduction losses. Turn on losses, $E_{on,}$ in the IGBT and recovery losses, $E_{rec,}$ in the diode occur simultaneously since the diode is blocked as soon as the IGBT is conducting. Turn off losses, $E_{off,}$ occur in the IGBT simultaneously with the turn on losses in the diode. In this work, diode turn on losses are very small compared to other losses and hence can be ignored in rapid switching processes. The switching of power modules for one switching cycle is shown in Fig. 3.

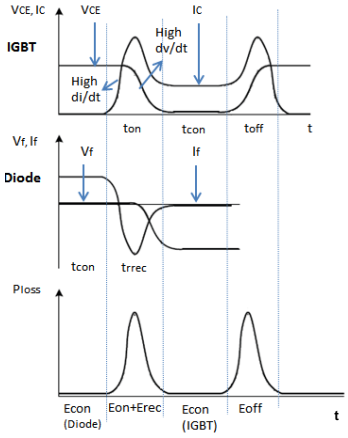


Fig. 3. Characteristics of IGBT and Diode energy losses with respect to voltage/current and switching behavior

The stepper change in *di/dt* and *dv/dt* causes the total switching losses which leads to increase in the temperature through the device. Energy losses can be expressed as a function of collector current I_c, voltage across the device V_{DC} and junction temperature T_j over one switching cycle as in (1)

$$E_{SW} = \int_{ton} V_{CE(t)}.I_{C(t)}.dt + \int_{toff} V_{CE(t)}.I_{C(t)}.dt + \int_{trec} V_{f(t)}.I_{f(t)}.dt = f(V_{DC}, I_C, T_J) \quad (1)$$

Hence, the switching power losses can be expressed as follows:

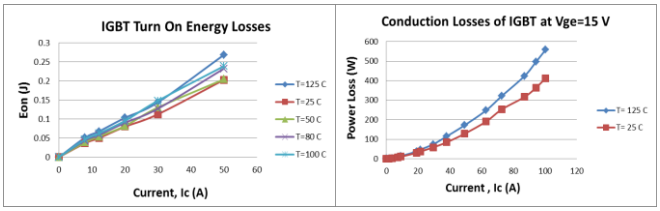
$$P_{SW} = (E_{SW}) f_{sw} \quad (2)$$

where f_{sw} is the switching frequency and V_{CE} is the collector-emitter saturation voltage of the IGBT. V_f and I_f are the forward conduction voltage and current of the diode, respectively. The total conduction power can be calculated as:

$$P_{Con} = V_{CE}.I_C + V_f.I_f = f(I_C, T_J, D) \tag{3}$$

where D is the duty cycle of switching signal.

Power loss models [37] have been developed in literature. These models are based on energy loss data supplied in manufacturers' datasheets. Since parallel die chips have individual power loss profiles, these approaches cannot provide an accurate representation of power losses within the individual elements of the power module. In this work, a new model was developed based on the actual current measurement that passes through each individual active device. Switching losses were obtained using double pulse step input test over a range of temperatures between 25°C-125°C. Conduction losses are obtained from the forward current/voltage characteristics for both IGBT and Diode. Both conduction and switching losses data were obtained over a range of temperatures and are saved in lookup tables. Using (1-3), the total power loss for each active device is calculated in each switching cycle. The algorithm is designed in Simulink. The turn on losses and the conduction losses of each IGBT active device are shown in Fig. 4 a & b.



(a) (b)

Fig. 4. (a) IGBT switching on losses (b) IGBT conduction losses

B. *Proposed Thermal Modelling for IGBT/Diode Module*

The thermal characteristics of each layer that are affected by heat flux must be determined precisely for an accurate thermal design. The heat diffusion equation (4) can be used to describe the distribution of heat flux through any material as a function of position and material properties. It can be used to give a solution for temperature variations of a defined region in the time domain, caused by conduction heat transfer as;

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} + \frac{q}{k} = \frac{\rho.c}{k}\frac{\partial T}{\partial t} \tag{4}$$

where T is the temperature, k is the thermal conductivity, c is specific heat capacity, ρ is the mass density and q is the rate of generation of energy per unit volume. A simplified form of (4) can be derived as in (5). It uses Laplace transform to solve the heat distribution within the power module [38].

$$D\left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2}\right) = sT - T_0 \tag{5}$$

where D denotes the diffusion coefficient, $k/\rho c$, $T(x,y,z,s)$ is the Laplace transform of the temperature and T_0 is the initial temperature. The thermal resistance R_{th} and capacitance C_{th}, functions of the material properties, are derived from (4) as;

$$R_{th} = \frac{l}{kA} \tag{6}$$

$$C_{th} = c.\rho.A.l \tag{7}$$

where l is the length and A is the cross-sectional area of a heated path. To represent the actual transfer function for each individual material, two commonly known thermal equivalent circuits, Cauer and Foster models can be used. The Cauer network has the advantageous of describing the temperature distribution between the actual physical layers (die, solder, substrate, etc.) but has analytically complex solution as shown in Fig 5 a. Foster network has cascaded mathematical form with parallel connected thermal resistance and capacities as shown in Fig. 5 b. To avoid complexity of computational analysis, Foster form was used in this work.

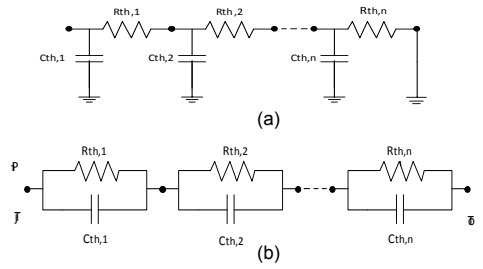


Fig. 5. Equivalent thermal model of (a) Cauer and (b) Foster networks

The transient thermal impedance for each component can be represented as follows:

$$Z_{th}(s) = R_{th} \,//\, 1/sC_{th} = \frac{R_{th}}{sR_{th}C_{th}+1} = \frac{1/C_{th}}{s+1/\tau} \tag{8}$$

$$\text{where } \tau = R_{th}C_{th} \tag{9}$$

By taking the inverse Laplace transforms of (8), Z_{th} becomes;

$$Z_{th}(t) = R_{th}(1-\exp(-\frac{t}{\tau})) \tag{10}$$

and for steady state analyses:

$$R_{th}(t) = \frac{T_j - T_0}{Pi} \tag{11}$$

where Pi is the initial heat source. For M layers and n heating sources, the temperature of each layer can be expressed as:

$$T_m(s) = \sum_{n=1}^{N}\sum_{k=1}^{Kmn}\frac{A_{mnk}}{s+\alpha_{mnk}}P_n(s) \tag{12}$$

where A is the coefficient $1/C_{th}$ and α is the $1/\tau$ in (8). A matrix form of (12) can be derived as in (13) where $a_1 a_{1,\ldots} a_{MN}$ are the transfer functions of thermal impedances.

$$\begin{bmatrix} T_{j1} \\ T_{j2} \\ \vdots \\ T_{jN} \\ T_{solder1} \\ \vdots \\ T_{AlNN} \\ \vdots \\ T_{baseplate} \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & \cdots & a_{1N} \\ a_{21} & a_{22} & \cdots & a_{2N} \\ & \vdots & \vdots & \\ a_{N1} & a_{N2} & \cdots & a_{NN} \\ & \vdots & & \\ & \vdots & & \\ & \vdots & & \\ a_{M1} & a_{M2} & & a_{MN} \end{bmatrix} \begin{bmatrix} P_{in1} \\ P_{in2} \\ \vdots \\ P_{inN} \end{bmatrix} + T_0 \tag{13}$$

III. DEVELOPMENT OF THE THERMAL MODEL

A. *Overview of the Model*

Fig. 6 shows a schematic of the internal layout of the IGBT power module defined in Fig 2. Each device consists of several layers as shown in Fig.7. Physical material and thermal properties are shown in Table I alongside the calculated thermal parameters (*Rth, Cth*).

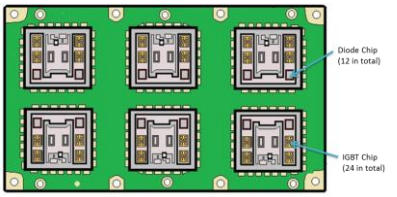


Fig. 6. Chip locations on the DIM1200ASM45 power module

The heat transfer function for each layer was represented using first order Laplace transfer function. Using a simplified form of the heat diffusion equation (5), one dimensional heat transfer function is used to represent the thermal behavior of each internal component. The transfer function accounts for the transient thermal impedance in (8) and considers the thermal parameters calculated in Table I. Each transfer function was implemented in Simulink with circuit element blocks based on Foster network arrangement.

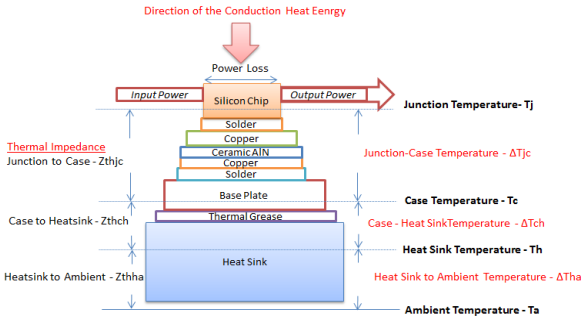
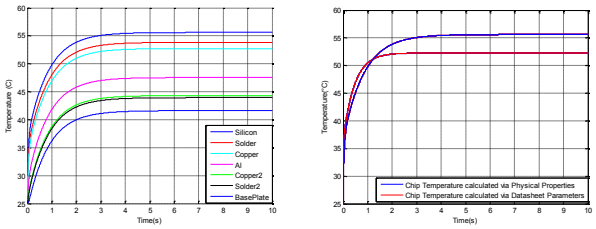


Fig. 7. Internal structure of the IGBT power module

TABLE I. PROPERTIES OF LAYER MATERIALS

Layer	Physical Property			Thermal Identity	
	ρ	k	c	C_{th}	R_{th}
Silicon, Die	2330	153	703	0.1127	0.013
Solder	7360	33	200	0.013	0.008
Copper, Cu	8850	398	380	0.182	0.004
AIN	3300	180	750	0.454	0.030
Copper, Cu	8850	398	380	0.185	0.040
Solder	11300	35	129	0.046	0.027
Baseplate	3010	180	741	2.047	0.151

As a test case, a power source of 133.2 W was applied to each silicon chip within the developed model as input heat source. The temperature distribution within each component of the power module is estimated as shown in Fig. 8. a. Considering the time constants of the individual module components, the test was applied for 10s. It is noticed that the junction temperature reaches steady state at 55.8 °C while the baseplate temperature is 42.6 °C. In this test the ambient temperature is kept constant at 25°C. Using the information supplied in the manufacturer's data sheet, the temperature-time data for the silicon die (silicon chip) was extracted and represented in Fig. 8.b alongside the same chip temperatures obtained from the previous results. In this figure it is noticed that the transient response is slightly faster compare to the temperature data based on the data sheet. Also there is slight difference in the steady state values. This is due to the fact that the estimated temperatures are not accurate enough because the developed model doesn't account for the heat coupling effects.



(a) (b)

Fig. 8. (a)Temperature distribution over one die from junction to baseplate (b) Junction temperature verification with datasheet

B. *Implementation of electro thermal model in Simulink*

The schematic of the developed electro thermal model with the power loss model is shown in Fig. 9. The generated input current signal was combined with look up tables where energy losses are provided to the thermal model. The control scheme triggers the power loss calculation and the total dissipated power is integrated with the thermal model.

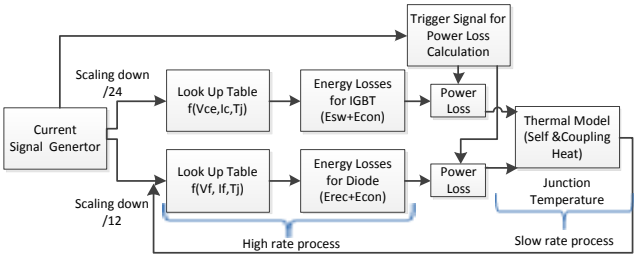


Fig. 9. Schematic of the Developed Model in Simulink

The Forward Rectangular Euler's rule was applied to the thermal coefficients that were extracted in s-domain. The transfer function *H(s),* equivalent to (8), can be expressed in discrete domain as:

$$H(s) = \frac{b}{s+a} \rightarrow H(z) = \frac{b}{\frac{z-1}{Ts}+a} \tag{14}$$

where T_s is the sample time. By applying a heat source, P_i, the change in the temperature, ΔT, can be expressed as follows:

$$\Delta T = \frac{1/C_{th}}{s+1/R_{th}C_{th}} P_i \tag{15}$$

This can be rearranged as in (16):

$$\Delta T = \frac{P_i}{sC_{th}} - \frac{\Delta T}{sR_{th}C_{th}} \tag{16}$$

Then conversion from s to z-domain can be written as:

$$\Delta T = \frac{P_i}{C_{th}} \frac{1}{z-1} - \frac{\Delta T}{R_{th}C_{th}} \frac{1}{z-1} \tag{17}$$

The thermal model was updated using (17) which was used to represent each first order transfer function. Hence each RC component of the Foster network was represented by a discrete z-form to illustrate the thermal behavior of each internal layer within the actual power module. This is useful for faster computation and for higher modelling accuracy. An example load profile is applied to the modified model using regular square wave of amplitude 133.2W to represent the actual phase current. The results are shown in Fig 10.

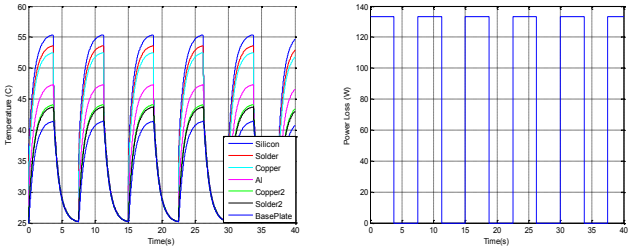


Fig. 10. (a)Temperature estimated for each layer and (b) Total Power Loss

IV. 3D MODEL OF THE POWER MODULE

In the previous model, heat coupling effects were not included. In order to detect cross coupling heat spread through the power module, 3D finite element model was implemented using COMSOL software. The 3D model of the power module can be seen in Fig. 11.

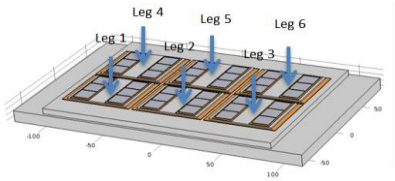


Fig. 11. 3D FEM of IGBT/Diode Module and attached Heat Sink

The module has six legs, each consists of four IGBT and two diode chips. All chips are at the same size and located with geometrical symmetries. Therefore, for instance, the heat flux distribution caused by chip DG33 will be equal to heat flux distribution at UG11, UG33 and DG11 as shown in Fig.12. Similarly, UD21, DD22, DD21 and DD22 are also in symmetry along different axes. Heat Diffusion Equation (5) was defined for the whole model to solve distribution of heat and temperature variations when an input heat power is applied. The ambient temperature was set to be 25°C and all outer boundaries are thermally isolated. A heat sink was attached to the rear surface of the base plate via a thermal grease layer for providing heat emission and was modelled as a block with the recommended size in [38].

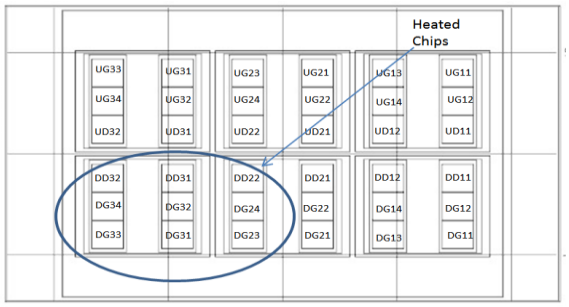


Fig. 12. View of the model with entitled chips where UGs & DGs state upper and down IGBTs and UDs and DDs are the upper and down diodes

A. 3D Thermal Modelling of Heat Flux

In order to extract the thermal characteristics of the whole module, the conduction power losses were applied as a constant heat source in time domain. The initial ambient temperature was set to 25 °C .Simulation time step was set to 1 millisecond and the simulation was computed until the step response of heating curve reaches steady state or thermal equilibrium. Individually heated chips are shown in Fig. 13

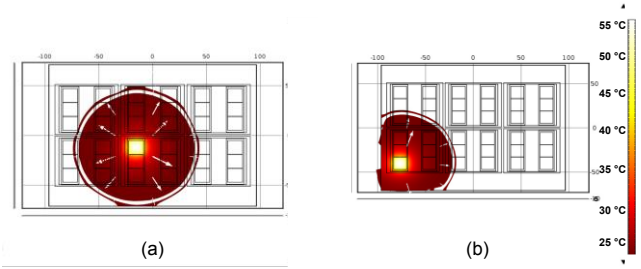


Fig. 13. Heating operation for (a) DG33 and (b) DD22 with 133.2W heat source

As depicted in Fig 13, the area of the effective heated region strongly depends on the location of the heat source. For example, when the chip DG33 is heated, only five neighboring chips and the layers underneath are affected by heat coupling effects. However, the total affected region is wider when DD22 is heated. In other words, the chips located in the middle will experience higher temperatures caused by cross coupling effects. The temperature distribution due to self-heating and heat coupling effects when the chip DG33 was used as a heat source is presented in Fig. 14 a & b, respectively.

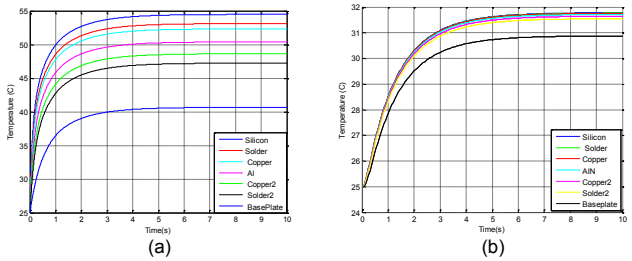


Fig. 14. (a)Temperature estimations of DG33 and the layers underneath (due to self-heating) (b) Temperature estimations of DG33 and the layers underneath (due to heat coupling effect caused by heating operation of DG34)

B. *Extraction of Thermal Impedances of the Internal Power Module's layers*

From the generated heat curves using FEM simulation, the coefficients R_{th} and C_{th} for each individual layer, were extracted by curve fitting using least square method. The extracted data was used to regenerate temperature estimates for each individual layer based on (17) using Matlab code. The extracted curves were verified by comparisons with the original 3D FEM model results as shown in Fig .15.

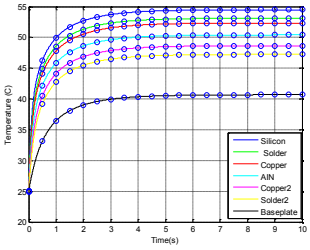


Fig. 15. Temperature estimation of DG33 and layers underneath by FEM-(self-heating of DG33) vs. fitted data using curve fitting

The extracted curves are represented as dots on the estimated temperatures of each layer. For more accuracy, the thermal impedance of each extracted curve was represented by three exponential terms. Using the extracted coefficients A and α of (12), 3rd order form of the extracted thermal parameters for the Silicon Die device, DG33, can be written as follows:

$$R_1(s) = \frac{A_1}{s+12.953},\ R_2(s) = \frac{A_1}{s+0.822},\ R_3(s) = \frac{A_1}{s+2.8212}$$

where A_1=1.127, A_2=0.057.4, A_3=0.183 and time constants τ_1=0.077s, τ_2=1.215s and τ_3=1.354s. The same process was applied for all the internal layers and the extracted parameters are shown in Table II.

TABLE II. THERMAL PARAMETERS FOR CHIP DG33 AND LAYERS UNDERNEATH DUE TO SELF HEATING

Layer	Thermal Capacitance			Thermal Resistance		
	$C_{th,1}$	$C_{th,2}$	$C_{th,3}$	$R_{th,1}$	$R_{th,2}$	$R_{th,3}$
Silicon, Die	0.887	17.53	5.45	0.0871	0.069	0.065
Solder	1.066	17.76	5.67	0.0785	0.068	0.063
Copper, Cu	1.187	17.91	5.81	0.0737	0.068	0.063
AIN	1.593	18.44	6.4	0.0634	0.066	0.060
Copper, Cu	2.147	19.16	7.27	0.0558	0.065	0.056
Solder	2.709	19.99	8.35	0.0513	0.062	0.052
Baseplate	7.177	18.32	641	0.051	0.062	0.003

TABLE III. THERMAL PARAMETERS FOR CHIP DG34 AND LAYERS UNDERNEATH DUE TO COUPLING EFFECT WHEN DG33 IS HEATED

Layer	Thermal Identity	
	C_{th}	R_{th}
Silicon, Die	23.074	0.0554
Solder	23.104	0.0553
Copper, Cu	23.144	0.0552
AIN	23.075	0.0549
Copper, Cu	23.568	0.0544
Solder	23.949	0.0537
Baseplate	26.8	0.0486

Thermal parameters due to the heat coupling effects were extracted using one exponential term and they are shown in Table III. The previously developed Simulink model was updated with thermal blocks which represent self heating and heat coupling effects for each layer on the module.

C. *Validation of the Simulink Model with FEM*

In order to verify the extraction process, an open loop test was applied for both FEM and Simulink models. A square wave input signal of 133.2 W was used to represent the power loss for the thermal model. This signal was applied at switching frequency 20 Hz and with 50% duty cycle. The ambient temperature was set at 25°C in both models. Comparison of estimated junction temperatures between FE and Simulink models are shown in Fig. 16 a & b, for IGBT and diode chips, respectively.

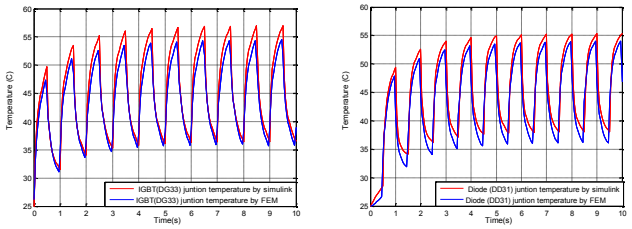


Fig. 16. Junction temperature estimated with FEM and Simulink for (a) IGBT and (b) Diode chip

As seen in Fig. 16 a, the maximum junction temperature difference between the FEM and Simulink model is approximately 2°C for the IGBT die. It can be concluded that good agreement in the estimated results is obtained between both models. Simulink model was further tested by generating pulse width modulation controlled current at 50 A with 50% duty cycle at 25°C ambient temperature. In this case the total calculated power is automatically applied to the thermal model by closed loop system discussed in Fig. 9, at 10 kHz frequency.

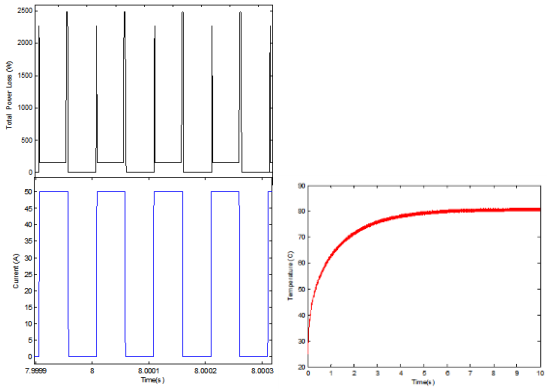
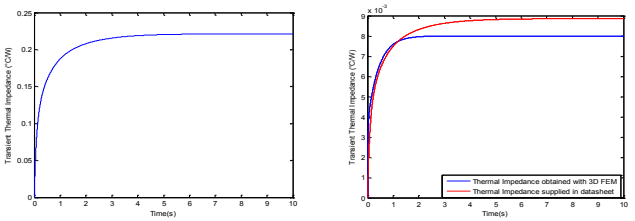


Fig. 17. (a) Chip current vs. power loss (b) junction temperature of DG33

As it is seen from Fig. 17 a, when maximum allowed current 50 A passes through IGBT chip DG33, as an example, power losses are automatically calculated using lookup tables as function of the applied current, duty cycle and temperature estimates. The junction temperature estimates for this test reaches 81.2 °C as it shown in Fig. 17 b.

D. *Verification of the Estimated Thermal Impedance*

In order to verify the calculated thermal characteristic of the power module, the junction to case thermal impedance which is estimated from FEM simulation is compared with the one supplied in the manufacturer's datasheet. Fig. 18 a shows the thermal impedance for one chip derived from FEM simulation.



(a) (b)

Fig. 18. (a) Thermal impedance for one chip derived from FEM simulation, (b) Thermal Impedance extracted from 3D FEM vs. the thermal impedance extracted from the datasheet

From the comparison shown in Fig. 18 b, the transient responses of both curves are similar which indicates that the time constants of each curves are quiet similar. The steady state value for the curve extracted from FEM results is 0.00895 °C/W while the datasheet provides a value of 0.008°C/W. This means that the junction to case thermal resistance difference between the FEM and datasheet value is less than 0.001 °C/W. Hence, the developed 3D FEM model can be validated to provide proper representation of the thermal behavior within the power module under study. This also applies for the latest Simulink model.

V. DISCUSSION AND FUTURE BENEFITS

In today's world, power electronic conversion units have been used to transfer billions of kilowatts of electrical energy, especially within renewable energy systems. They are essential for the contribution of remarkable energy saving and environmental pollution control in broader perspective. European countries commit themselves that 20% of the entire electricity consumption will be provided through wind energy by 2020 [2]. According to the [39], doubling the use of wind energy in the Mid-Atlantic and Great Lakes would save for the consumers a net $6.9 billion per year, in US. On the other hand, the increase in the energy estimated from renewable sources will lead even greater currents passing through the power electronic components; hence in future trends, the ability of withstanding the imposed stresses will be important factors in power electronics module reliability [1]. With this particular study, thermal management will be assessed for the power conversion elements of wind turbine system. More control among these devices, in terms of reliability [2], surely will bring more trust to wind energy systems and this would increase the number of national or locally owned businesses and investments. The presented work is essential for reliability of wind energy applications. The verification test of models showed very good agreement with the thermal profile supplied in the manufacturer's datasheet and could also be improved with experimental validation tests in future work.

VI. CONCLUSION

In this paper, an electro-thermal model for power electronics module DIM1200ASM45 is developed. The commercially available circuit simulators cannot represent the actual heat flux distribution through the device. Therefore in this work, 3D FEM thermal analysis has been developed to estimate heat interactions between different internal layers of the module. Multi-chip design technology brings the disadvantage of highly complex temperature profile. The cross coupling effects occur through the hidden layers that cannot be easily estimated in practice; hence the proposed model defines each heat path of the individual components. The 3D FEM results were verified based on the thermal impedance data supplied by the manufacturers' module datasheet where they showed good agreement. The developed electro thermal model is used to represent the actual behavior of the power module in operation. It can be concluded that the proposed method is well-suited for monitoring the internal behavior of the thermal effects within power electronic modules under their working conditions. The proposed model can also be extended for providing life consumption monitoring and prognostics methods that will bring higher trust on wind energy systems by solving heat transfer problems and reliability issues.

VII. FUTURE WORK

The future work will present the electro thermal modelling of a two level back to back converter with a control scheme that considers six DIM1200ASM45. Fig 19 shows schematic of such converter which is embedded in a wind energy system.

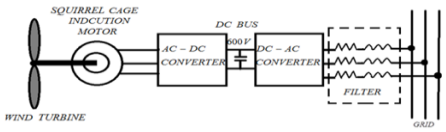


Fig. 19. Schematic of two level back to back converter in wind applications

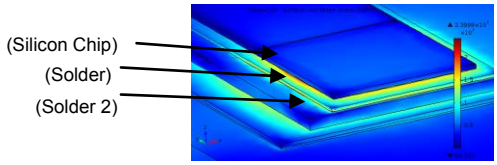


Fig. 20. Stress analysis for a single die chip

Furthermore, in order to detect the thermal expansion and stress analysis, 3D FEM studies will be extended. A pilot study shown in Fig. 20 represents the most stressed regions of device. Edges of solder layers have the most stressed region due to different material properties (thermal expansion coefficient). Future study will consider failures in power conversion units used in wind energy applications and investigating proper techniques based on the developed thermal model for failure analysis and health monitoring.

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