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A Wideband Sliding Correlator based Channel Sounder in 65 nm CMOS: An Evaluation Board Design

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Abstract-Wide swaths of bandwidth at millimeter-wave (mm-Wave) and Terahertz (THz) frequencies stimulate diverse applications in wireless sensing, imaging, position location, cloud computing, and much more. These emerging applications motivate wireless communications hardware to operate with multi-Gigahertz (GHz) bandwidth, at nominal costs, minimal size, and power consumption. Channel sounding system implementations currently used to study and measure wireless channels utilize numerous commercially available components from multiple manufacturers that result in a complex and large assembly with many costly and fragile cable interconnections between the constituents and commonly achieve a system bandwidth under one GHz. This paper presents an evaluation board (EVB) design that features a sliding correlator based channel sounder with 2 GHz null-to-null RF bandwidth in a single monolithic integrated circuit (IC) fabricated in 65 nm CMOS technology. The EVB landscape provides necessary peripherals for signal interfacing, amplification, buffering, and enables integration into both the transmitter and receiver of a channel sounding system, thereby reducing complexity, size, and cost through integrated design. The channel sounder IC on the EVB is the world's first to report gigabit-per-second baseband operation using low-cost CMOS technology, allowing the global research community to now have an inexpensive and compact channel sounder system with nanosecond time resolution capability for the detection of multipath signals in a wireless channel.

Index Terms—Sliding correlator channel sounder, on-chip baseband, pseudo-random noise sequence, RF grounding, microstrip impedance, printed circuit board

I. INTRODUCTION

Wireless communication technologies utilize mm-Wave frequencies in fifth-generation (5G) cellular wireless [1]–[3], while future sixth-generation (6G) cellular wireless systems and beyond envision operation at even higher frequencies into the Terahertz (THz) range [4]. The higher frequencies provide wide swaths of GHz range bandwidth that can be leveraged for diverse applications involving thousands of interconnected devices communicating at multi Gigabits-persecond (Gbps) data rates with sub-millisecond latency [5]. Especially in the study of wireless channels, GHz wide bandwidths allow systems to detect multipath signals at

nanosecond time differences which facilitates development of accurate channel models for indoor and outdoor environments, and applications such as centimeter level accurate position location, environmental sensing, and imaging [4], [6]–[8].

The onward march into higher frequency ranges necessitates the improvement of existing RF hardware in terms of operating frequency, bandwidth, noise figure (degradation factor of signal-to-noise ratio by a device), sensitivity (minimum signal level detectable at the receiver), and monolithic integration of high performance components [9]. As an example, present foundry technologies are able to typically fabricate transceivers that operate up to 200 GHz with sub-GHz RF bandwidth, noise figures at 9 dB and power amplifiers that can provide 180 mW power [9], [10]. Evidently, the operational bandwidth of most commercial-off-the-shelf (COTS) wireless devices remains under one GHz and monolithic designs are pursuant of achieving higher bandwidth. Currently, most channel measurement setups also operate under one GHz bandwidth and involve the integration of multiple discrete COTS components including clock sources, amplifiers, mixers, signal generators, and transceivers [11]-[15]. Alongside cost implications, complexity and interfacing requirements among multiple components from different manufacturers, COTS systems are limited by the maximum chip rate of the baseband electronics, time resolution in the power delay profile (PDP) of the signals received, and difficulty in implementing multiple transmitting and receiving channels in parallel for the study of multiple antenna wireless communications [11], [13], [14], [16].

This paper presents an evaluation board (EVB) design that features an ultra-wideband, programmable, synchronization capable channel sounder integrated circuit (IC) implemented in 65 nm complementary metal oxide silicon (CMOS) technology as the principal component. The EVB introduces peripherals necessary to interface the IC into a channel sounding system including clock buffers, single ended and differential signal converters, amplifiers, programming switches and a power supply. The rest of the paper is organized as follows: Section II describes fundamental concepts involved in design-

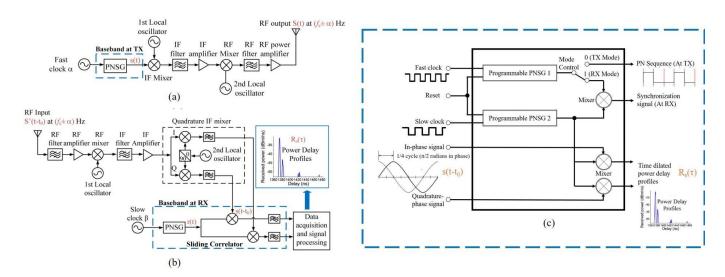


Fig. 1. (a) A transmitter system block diagram that generates pseudo-random noise sequence at chip rate α . (b) A receiver system block diagram with a sliding correlator implementation for generating time dilated power delay profiles. (c) Block diagram of the baseband at tansmitter and receiver merged on a single channel sounder chip

ing the baseband monolithic IC, Section III highlights the board design process, and Section IV presents the final board fabrication with initial test results.

II. DESIGN AND SPECIFICATIONS OF THE ON-BOARD SLIDING CORRELATOR BASED CHANNEL SOUNDER CHIP

A. Sliding correlator based channel sounding

Introduced by Don Cox in [17], sliding correlation is a time tested method for the measurement of ultra-wideband wireless channels using direct sequence spread spectrum signals. The method involves transmission of a predetermined signal known both to the transmitter (TX) and receiver (RX) beforehand, with signal statistics that resemble Gaussian white noise, known as the pseudo-random noise (PN) sequence [18]. The RF signal received at RX is then correlated with the PN sequence replica which results in a power delay profile of the received signal.

Fig. 1(a) and (b) are block representations of TX and RX setup in a sliding correlator based channel sounder [16]. In reference to Fig. 1(a), initially a PN sequence generator (PNSG) generates a PN sequence, s(t), at a chip rate equal to the fast clock input, α . The PNSG is implemented using maximal linear feedback shift registers with programmable feedback taps. At the subsequent mixer, s(t) modulates an intermediate frequency (IF) signal generated by the first local oscillator. The modulated signal at IF is upconverted to the RF carrier frequency, f_c , resulting in the RF output signal at $f_c \pm \alpha$ that is transmitted over the wireless channel. The wideband signal thus transmitted is subject to reflection, diffraction, scattering, and transmission through blockages in the channels before arriving at the receiver. The effects of the channel cause multiple replicas of the transmitted signal to arrive at the receiver over multiple paths at different delays. As illustrated in Fig. 1(b), the received multipath signals are down-converted and demodulated before sliding correlation is performed with a replica of the transmitted PN sequence operating at a slightly slower clock rate of β , referred to as r(t). The result of the sliding correlation process is a time dilated PDP that represents the time domain response of the channel, given by:

$$R_s(\tau) = \int_0^T r(t)s(t - t_0 - \tau)dt,\tag{1}$$

The dilation in the time scale of the received PDP corresponds to the sliding factor γ , obtained as in Eq. (2).

$$\gamma = \frac{\alpha}{\alpha - \beta},\tag{2}$$

B. Design of the on-board channel sounder IC

The dashed blue boxes in Fig. 1(a) and (b) represent the baseband components of the TX and RX which is combined by the channel sounder chip design on a monolithic IC design that is capable of operating at either end of the channel sounder system. As shown in Fig. 1(c), the 'Mode Control' pin on the IC is used to switch between TX mode for the pin set to 'Low' and RX mode for pin set to 'High'.

The output of PNSG 1 directly generates PN sequence at chip rate of α in TX mode. In RX mode, the output of PNSG 1, s(t), is mixed with the output of PNSG 2, r(t) at chip rate β , to generate the synchronization signal which is a zero delay absolute timing reference for the multipath components arriving at the receiver. The signal r(t) is also fed into two mixers in order to perform the sliding correlation function with the in-phase and quadrature components of the demodulated received signal. The output of the two mixers constitute the result of the sliding correlation function, $R_s(\tau)$.

III. DESIGN AND TESTING OF THE EVB COMPONENTS

A. Channel Sounder IC Specifications based on Measurements

Fabricated in a 65 nm CMOS process, the channel sounder chip is a monolithic design of 1 mm \times 0.66 mm silicon,

packaged in an industry standard QFN48 IC package of 6 mm \times 6 mm, as displayed in Fig. 2, and is the centerpiece of the EVB design [16], [19], [20].



Fig. 2. The 1 mm \times 0.66 mm channel sounder chip in 65 nm CMOS housed in a QFN48 IC package of 6 mm \times 6 mm with 48 pin connections along the edges.

Initial tests with the chip directly wire bonded to a printed circuit board (PCB), and a 1.1 V supply voltage verified the sequence accuracy, chip rate, and bandwidth for different lengths of PN codes. Upon feeding with a 1 GHz clock signal as α and programming a sequence length of 2047 $(2^N-1,N=11)$, the chip sequence was observed in time domain as the black trace in Fig. 3(a). Peak-transitions in the analog waveform higher than 0.5 V were recorded as '1', else '0' to obtain the blue trace and verify valid strings of same consecutive bits (runs) in the sequence. The spectrum measurement for the 1 Gbps PN sequence was as shown in Fig. 3(b) with the power profile showing a distinct energy peak of -18.4 dBm at 1 GHz, indicating 2 GHz null-to-null RF bandwidth. Specifications of the chip following the initial testing are tabulated in Table I [16].

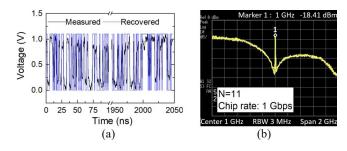


Fig. 3. (a)Time domain measurement of the generated PN sequence; analog waveform (black), bit sequence (blue). (b) Measured spectrum for the PN sequence operating at 1 Gbps for sequence length N=11

B. Layout of the EVB

The EVB design focuses on interfacing the wideband channel sounder IC to the 142 GHz channel sounding setup at NYU WIRELESS [15]. The board provides essential peripherals for the IC operation, which perform amplification and filtering of RF signals, inter-conversion between signal communication methods—differential and single-ended signaling, buffering and amplification of clock signals, and provide stable power supply at different voltages. Electronic components on the board are grouped into sub-units based on

TABLE I

MEASURED SPECIFICATIONS FOR THE FABRICATED WIDEBAND CHANNEL
SOUNDER BASEBAND DESIGN

Item	Specification			
Technology	65 nm CMOS			
Maximum Chip Rate	1 Gbps			
Multipath Delay Resolution	1 ns			
Null-to-Null RF Bandwidth	2 GHz			
PN Code Length	$2^N - 1 \ (N = \{5, 6,, 12\},\$			
	programmable)			
Power Consumption	6 mA at 1.1 V			
IC Packaging	QFN48 6×6 mm ²			
Synchronization	Supported			

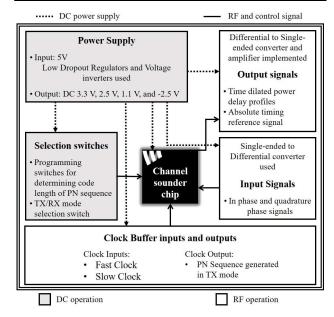


Fig. 4. Functional block diagram of the EVB sub-units with relative board positioning. Gray highlighted blocks represent DC operating frequency.

function and distributed over the board area according to the layout displayed in Fig. 4.

The board is laid out with sub-units operating at DC placed in a separate region from sub-units operating at frequencies up to 1 GHz. The separation of regions helps prevent interference on RF signal traces from the DC common-mode, and manage return paths within separated DC/RF ground planes. It helps preserve the integrity of signals near RX sensitivity (typically below -100 dBm) common at mm-Wave and THz frequencies.

C. Design considerations for the EVB

Grounding: All signals flowing in a circuit seek the lowest impedance path to return to the signal power source to complete the circuit. As many signals are operating in a typical circuit, a single wire or trace of limited width and cross-section providing the return connection may have to carry hundreds of amperes current per cm^2 of cross-section area [21]. Thus, a ground plane is a standard method of providing a broad cross-section for returning signal currents while minimizing the return path resistance. However, it is not a panacea for providing return paths to all signals as

the behavior of returning currents varies by frequency. A DC signal returns over the shortest path on the ground plane, while RF signals seek out the path of minimum impedance [22]. For a two-layer PCB layout with signals routed on the top and ground on the bottom layer, RF signals above 1 MHz travel directly beneath the top layer signal trace. Furthermore, as DC signal return currents take the shortest path to ground, loops are formed on the ground plane, which may couple noise and interfere with RF signals.

RF signal traces routed on multi-layer PCBs require a continuous ground plane underneath without any slits and breakages along the entire return path. The presence of disruptions in the ground plane changes the path length for RF signals, as returning signals loop around the breakage [23]. For example, at a millimeter wavelength, the change in path length by a half-mm may put differential signals in-phase and change the path impedance to cause complete signal reflections.

Impedance of RF signal traces: Reflection of RF signals is avoided, and maximum power flow is maintained during the propagation of an RF signal over traces across the circuit board when the impedance is uniform throughout the signal path. Sub-miniature version-A (SMA) connectors with characteristic impedance of 50 Ω are commonly used to transport RF signals over the wire in RF systems. Thus, RF signal traces with a continuous ground underneath, called micro-strip traces, are designed to have 50 Ω characteristic impedance for RF-PCBs, as obtained from Eq. (3) [24].

$$Z_0 = \frac{87}{\sqrt{\epsilon_r + 1.41}} ln\left(\frac{5.98h}{0.8w + t}\right),\tag{3}$$

where,

 $Z_0 = \text{micro-strip impedance}$

 ϵ_r = dielectric constant of insulating material

h =separation between trace and ground in mils (1 mil= 0.001 inches)

w = width of the trace in mils

t =thickness of the trace in mils

The trace width (w) in Eq.(3) may be varied to achieve the 50 Ω impedance. An extension to Eq. (3), shown in Eq. (4), is required to calculate the characteristic impedance for differential signal pairs as signals in a differential pair are referenced to each other and not to ground [24]. Finally, the trace length determines the input impedance offered by the trace and the connected load.

$$Z_d = \frac{174}{\sqrt{\epsilon_r + 1.41}} ln\left(\frac{5.98h}{0.8w + t}\right) \left(1 - 0.48e^{\left(-0.96\frac{d}{h}\right)}\right),\tag{4}$$

where, d is the separation of differential pair traces in mils

D. Sub-units of the EVB and Test Results

Before implementation on the final EVB, the sub-units were designed and tested on individual test PCBs. The test boards

were fabricated in-house at NYU-MakerSpace on double-sided bare PCB with 18 μ m copper layers each side separated by 0.79 mm flame retardant-4 (FR-4) insulation material with a dielectric constant of \sim 4.2. The fabricated test boards are displayed in Fig. 5. The sub-units are detailed as follows:

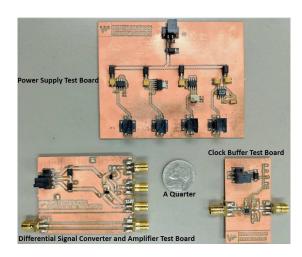


Fig. 5. In-house fabricated test boards on double sided PCB. RF connections terminated with SMA connectors, DC connections with wire terminal blocks.

Single-ended signal converter and amplifier: To eliminate noise from the power supply, and thermal noise from external components that single-ended signals are subject to, the mixers and amplifiers in the chip baseband are designed for differential operation [16], [25]. However, the RF signals carried on coaxial cables interconnecting components of the 142 GHz channel sounder, setup at NYU WIRELESS are single-ended. Based on Fig. 1(b), to interface the chip input with the preceding IF mixer at the RX, each single-ended input signal from the IF mixers are split into two signals of equal magnitude but opposite polarity using a 50 Ω 700 MHz balun circuit. The implemented balun is a transformer with a 1:1 turns ratio between the primary and center-tapped secondary winding [26]. The primary is fed by the 500 MHz low pass filter output of the preceding IF mixers [15]. The secondary winding terminals of the balun circuit provide the differential input signals required by the chip.

In initial tests, a 500 MHz 100 mVp-p square wave was split into out-of-phase 44 mVp-p sinusoids, indicating a 0.5 dB insertion loss.

Differential signal converter and amplifier: A sliding correlation on two PN sequences results in a low-frequency time dilated PDP component with distortion components at a frequency above $\alpha - \beta$. This waveform is output by the chip in two components, each as a differential signal pair as in Fig. 1(b). The differential signal converter-and-amplifier merges the output signal pair into a single-ended signal, then low-pass filters and amplifies the single-ended signal, using the schematic shown in Fig. 6.

The merging and filtering stage outputs a single-ended signal with an amplitude equal to the difference between the two input signal amplitudes. The resistor (R3) and

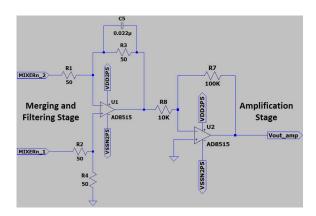


Fig. 6. Two stages of the differential to single ended signal converter and amplifier: the merging and filtering stage followed by the amplification stage; implemented with the AD8515 operational amplifier from Analog Devices.

capacitor (C5) placed in parallel on the feedback line in Fig. 6 implement a first-order low-pass filter with a 3 dB bandwidth of 150 kHz to suppress the distortion component of the waveform. The amplification stage then amplifies the single-ended signal by gain equal to the ratio of resistances on the feedback line (R7) to the input line (R8) in Fig. 6, thus implementing a gain of 10 dB. The final board design implements a switch-selectable gain of 3, 10, or 20 dB.

Clock Buffer: Clock signals are crucial to the implementation of a sliding correlator based channel sounder as they determine the rate of the PN sequence, bandwidth of the transmitted signal, and time dilation factor corresponding to γ . Direct distribution of the clock from a clock-source into different board components may degrade the waveform of the clock signal due to the added loading, noise from the on-board electronics, and cabling losses. For instance, a 10 pF additional stray capacitance can add a 200 mVpp ringing distortion on a 500 mVp-p square wave [22]. Thus, the addition of a buffer between the clock source and clock dependent components can alleviate the waveform degradation and amplify the clock source prior supplying the components.

A 7.5 GHz state-toggling capacity clock buffer is implemented as a test board based on Fig. 7, for both the fast and slow clocks α and β in Fig. 1(c). Testing showed a consistent 600 mVp-p square wave output at the input clock frequency for input down to 60 mVp-p.

Power Supply: The components of the EVB require DC supply voltage at different levels; the clock buffer operates at 3.3 V, the differential signal converter and amplifier operates at $\pm 2.5 \text{ V}$, and the wideband channel sounder IC requires 1.1 V for biasing transistors and 2.5 V for driving input and output pins on the IC. The three positive voltages are generated with low dropout (LDO) voltage regulators [27], while the negative voltage is generated with a switched capacitor charge pump voltage inverter [28]. The current drawn by each of the test boards is measured with the power supply test board connected to a bench top regulated DC power supply at 5 V and the other boards connected to the voltage output ports of the power supply test board and is presented in Table II.

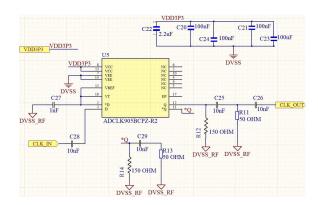


Fig. 7. Clock buffer circuit schematic with matched terminations and DC blocking capacitor filters on clock input and output.

TABLE II
CURRENT DRAW FOR EACH SUB-UNIT OF THE EVB

Sub-Unit of EVB	Type	Supply voltage	Current draw (standby)	Current draw (active)
Power supply	Active	5 V	4 mA	172 mA
Clock buffer	Active	3.3 V	< 1 mA	44 mA
Differential signal con- verter and amplifier	Active	- 2.5 V/ 2.5 V	< 1 mA	5 mA
Single-ended signal converter	Passive	N/A	N/A	N/A

N/A: Not applicable

IV. EVB FABRICATION AND INITIAL MEASUREMENTS

The final EVB is designed on a four-layer PCB with FR-4 dielectric insulation between layers. Micro-strip traces interconnecting components are routed on the top-layer with RF ground on the second layer plane. The third layer is used to distribute power supply lines and the bottom layer for grounding DC components in non-overlapping regions with the second layer. Further, the top-layer RF traces are shielded on either side by regions grounded with vias connected to the second layer RF ground. Such ground shielded traces minimize additional parasitic impedance from outward radiating fringing fields, prominent at mmWave and THz frequencies. Based on Eq. (3), the PCB has a top-layer copper of thickness (t) 1.4 mils, a separation (h) of 9.13 mils between each layer with FR-4 insulation of ϵ_r 4.2. Hence, an impedance of 50.01 Ω is obtained for micro-strip traces with width (w) of 15.75 mils. Differential signal traces on the top-layer have a pair separation (d) of 25 mils for a differential impedance of 96.56 Ω . The PCB features 50 Ω SMA connectors to interface with external components. The final PCB layout of the channel sounder EVB is presented in Fig. 8.

Following component assembly, EVB operation yielded a peak current draw of 172 mA at 5 V input when generating a transmit PN sequence at α of 1 GHz, with an energy peak of -30 dBm at 1 GHz in the measured spectrum power profile. The PN waveform showed consistent runs of ones and zeros, as described in [16], at 600 mVp-p for α and β input down to 70 mVp-p from 100 MHz to 1 GHz.



Fig. 8. Top view of the sliding correlator based channel sounder EVB with all components assembled. Channel sounder IC at the center.

CONCLUSION

A wideband sliding correlator based channel sounder IC fabricated using 65 nm CMOS processes is featured in an EVB design for interfacing with the 142 GHz channel sounder system at NYU WIRELESS. The monolithic channel sounder IC design, using low-cost CMOS technology, achieves a remarkable 1 Gbps baseband operation; the EVB for the IC implements the baseband of an entire channel sounder setup with null-to-null RF bandwidth of over one GHz. This design reduces channel sounder system costs from hundreds of thousands to a few thousand dollars while reducing system complexity, compressing size to portable volumes, and delivering higher resolution channel measurements. Future research involves interfacing the EVB and channel sounder system and measuring the board performance in operation.

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