The work is accepted for publication in IEEE International Symposium on Hardware Oriented Security and Trust (HOST), San Jose, USA, December 06-09, 2020 ©2020 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.

Secure Boot from Non-Volatile Memory for Programmable SoC Architectures

Franz-Josef Streit^{*}, Florian Fritz^{*}, Andreas Becher^{*}, Stefan Wildermann^{*}, Stefan Werner[†], Martin Schmidt-Korth[†], Michael Pschyklenk[†], Jürgen Teich^{*}

*Department of Computer Science, Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Germany

[†]Schaeffler Technologies AG & Co. KG, Germany

Email: {franz-josef.streit, florian.fritz, andreas.becher, stefan.wildermann, juergen.teich}@fau.de

{s.werner, schmmrt, pschymch}@schaeffler.com

Abstract-In modern embedded systems, the trust in comprehensive security standards all along the product life cycle has become an increasingly important access-to-market requirement. However, these security standards rely on mandatory immunity assumptions such as the integrity and authenticity of an initial system configuration typically loaded from Non-Volatile Memory (NVM). This applies especially to FPGA-based Programmable System-on-Chip (PSoC) architectures, since object codes as well as configuration data easily exceed the capacity of a secure boot ROM. In this context, an attacker could try to alter the content of the NVM device in order to manipulate the system. The PSoC therefore relies on the integrity of the NVM particularly at boot-time. In this paper, we propose a methodology for securely booting from an NVM in a potentially unsecure environment by exploiting the reconfigurable logic of the FPGA. Here, the FPGA serves as a secure anchor point by performing required integrity and authenticity verifications prior to the configuration and execution of any user application loaded from the NVM on the PSoC. The proposed secure boot process is based on the following assumptions and steps: 1) The boot configuration is stored on a fully encrypted Secure Digital memory card (SD card) or alternatively Flash acting as NVM. 2) At boot time, a hardware design called Trusted Memory-Interface Unit (TMIU) is loaded to verify first the authenticity of the deployed NVM and then after decryption the integrity of its content. To demonstrate the practicability of our approach, we integrated the methodology into the vendor-specific secure boot process of a Xilinx Zynq PSoC and evaluated the design objectives performance, power and resource costs.

Index Terms—Security, Memory-Protection, SoC, FPGA, Secure Boot, Hardware/Software Co-Design

I. INTRODUCTION

Many applications in emerging domains like the Internet of Things (IoT), industrial and automotive control as well as medical data processing depend on rigorous trustworthiness as well as system integrity. However, the fact that the deployment of these embedded systems in the field requires to control/program them remotely makes them susceptible to malicious manipulation and data or Intellectual Property (IP) theft. In order to cope with changing requirements over the lifetime of a product, connected and upgradable FPGAbased Programmable System-on-Chip (PSoC) architectures are gaining more and more interest and visibility. Examples are platforms for the Industrial IoT, autonomous driving, multicamera surveillance, cloud computing, connected health and other applications [1, 2, 3, 4, 5]. Especially here, undermining the security can have significant negative impact including monetary deficits, loss of privacy, and even physical damages.

This paper addresses the challenges of protecting the integrity and authenticity of such systems during boot, but also operational mode in a potentially unsecure environment. Since a processor typically boots from Non-Volatile Memory (NVM), e.g., a Flash memory or an external SD card, trust can only be assumed in case that this NVM can be a) unambiguously identified and b) checked that the content has not been altered by an attacker. Moreover, such NVM also often stores not only software, but also the configuration data of proprietary hardware IP blocks to be loaded to the reconfigurable fabric of an FPGA. In addition, on many devices, the memory is used to store sensitive user data, as well as login credentials which also must be protected. Nevertheless, an adversary with physical access could copy or even modify the content of the NVM in order to steal these valuable data, execute malicious code, or load undesirable hardware configurations [6]. In this context, researchers have just recently discovered unpatchable security flaws on Xilinx Zyng UltraScale+ PSoCs [7]. Here, a certain secure boot mode does not authenticate the boot image metadata and partition header tables stored on NVM, which leaves this data vulnerable to malicious modifications. As a consequence, an attacker could modify the boot header and partition tables to load arbitrary code, thereby bypassing the entire security measures offered by the vendor's secure boot process. Other attacks have shown that particularly configuration bitstreams could be manipulated in a way that the system exposes security sensitive information such as user data or keys [8, 9].

To address these problems and to ensure the confidentiality and integrity of the entire system configuration, a strong scheme for authentication of NVM and its content that extends beyond existing methods is required. In this paper, we propose therefore a hardware-centric boot process for PSoCs from NVM. Its central component realized in reconfigurable logic is called *Trusted Memory-Interface Unit* placed as an intermediate instance between the processor and the NVM to guarantee integrity, confidentiality, and authenticity of hardware/software programmable SoC configurations over the whole product lifetime, see Fig. 1. The main features of this hardware unit are:

- Entire NVM authentication as well as sector-wise de- and encryption including metadata.
- On-the-fly key generation for symmetric encryption instead of external key storage.
- Instant integrity checking of the boot image before any user application program is loaded into volatile memory.

This offers several advantages over conventional softwareonly solutions and can build upon existing methods provided by PSoC vendors resulting in a depth layered security. For instance, changing security requirements during the product lifetime can be addressed by upgrading the deployed cryptographic primitives, while software vulnerabilities and performance or power constraints are targeted through isolated execution in dedicated hardware accelerators. In addition, without the need for external key exchange, the TMIU allows to tie the NVM content to a specific PSoC device. In this way, these components form a permanent and immutable system to protect proprietary IP and sensitive data. In consequence, a configuration is only bootable from an NVM when it has been successfully authenticated and found in an unaltered condition. Subsequently, this raises both the trust and security level of the entire system and allows the system designer to keep track of the delivered IP.

In the following, we define the steps and flow of this secure boot process and the concept and structure of the TMIU. Subsequently, we integrate this concept into the secure boot process on a Xilinx Zynq *PSoC*-platform containing an Artix-7-based *Programmable Logic (PL)* and a dual-core ARM Cortex-A9 *Processing System (PS)*. Finally, we analyze performance as well as power and resource overhead of the proposed protection mechanisms. The remaining of the paper is organized as follows: Section II presents related work. Our system and threat model is briefly introduced in Section III. The proposed protection process and the hardware design of the TMIU concept is described in Section IV. Finally, experimental results of the secure boot methodology are demonstrated in Section V, followed by a conclusion and outlook on future work in Section VI.

II. RELATED WORK

In the recent past, several mechanisms have been proposed to provide trustworthy operation of embedded systems on the one side and the prevention of IP theft on the other side. These mechanisms include the deployment of cryptographic hardware, secure boot, the implementation of Physical Unclonable Functions (PUFs), and techniques for IP protection [10, 11, 12, 13, 14]. In this context, FPGAs have been proven to offer all necessary means for protection of confidentiality, integrity, and authenticity. Nevertheless, volatile FPGAs have an Achilles heel: they are highly vulnerable to bitstream manipulation, socalled tamper attacks, which can cause unwanted and illegal behavior or even lead to the leakage of sensitive data such as IP and secret keys.

Previous work has also shown that reverse-engineering of Lookup Table (LUT) content from an unencrypted FPGA bitstream is possible [15]. As a countermeasure, the FPGA vendors provide anti-tamper techniques such as symmetric bitstream encryption (AES-256) and private/public key authentication (HMAC + SHA-256, RSA-2048) already since a very long time. By encrypting the bitstream, the design is protected against any attempt to clone or reverse engineer valuable IP [16]. Whereas, bitstream encryption must be combined with authentication to protect the device against manipulation (e.g., fault and Trojan injection) and to ensure that the bitstream comes from a trusted authority [17]. On Xilinx FPGAs, this can be accomplished by available hardwired on-chip crypto modules, while the necessary decryption keys can be stored on either one-time programmable E-Fuse registers or batterybacked RAM [14]. However, both the AES and the SHA modules are not accessible from the programmable logic, and therefore, not applicable for any custom cryptographic system design. Moreover, neither hardwired instances nor onchip key storage can provide absolute security guarantees. For example, in the work of Moradi et al. [18, 19], a side-channel attack is described that performs Differential Power Analysis (DPA) during bitstream encryption to extract the secret AES key, while Skorobogatov [20] proposes optical fault injection attacks to extract decryption keys from secure embedded memory. In [21], a fault injection attack on an FPGA is described by tampering of configuration bits inside Block RAMs (BRAMs) to extract the AES key. Countermeasures targeting key theft can be realized by PUF implementations to generate FPGA-internal keys. However, these rely either on the reverse engineering complexity of undocumented bitstreams [22] or trivialise negative effects on their reliability caused by aging and harsh environment conditions [23, 24]. In comparison, our approach builds in the first instance on the basic capabilities already provided by commercial FPGAs and adds an additional but necessary layer of security by verifying the deployed NVM and the use of on-the-fly key generation to minimize the risk of system exposure. Moreover, the required cryptographic primitives are fully embedded into the programmable logic, and therefore, allow for customization if the security demands will change.

Although dedicated hardware units with cryptographic engines such as Trusted Platform Modules (TPMs) and Hardware Security Modules (HSMs) are widely used on conventional processor-based systems, cf. [25], and also concepts for their combination with FPGAs exists [10], the requirements on highly integrated PSoC architectures differ. The initialization of both hardware and software after power-up is a unique feature of PSoCs. For this reason, the PSoC vendors provide the option to initialize a system in a secure boot mode. However, previous PSoC generations used the embedded components (processors and peripherals) as slave devices to the FPGA, whereas for instance, the widely used Xilinx Zynq device family now uses the processing system as the master and the programmable logic as the slave [26]. This leads to several problems, software attacks such as code injection to trigger buffer overflows or hardware Trojans to apply direct memory or bus manipulation threaten now the whole system security. In addition, the Xilinx secure boot process is based on the creation of a chain of trust with the processor loading the entire system configuration from NVM while relying on the confidentiality of the decryption keys stored on-board. Although the system may take the verification and encryption of the bitstream into account, the system cannot detect or prevent any manipulation of the boot image metadata or partition tables of the NVM, which leaves this data vulnerable to malicious modifications [7].

Indeed, the secure boot process on Xilinx Zyng PSoC systems can be bypassed. This was demonstrated in [27] by direct memory manipulation through malicious hardware insertion. Here, the authors exploit the vulnerability of the processor-centric architecture of Xilinx PSoCs to circumvent the secure boot process by adding an IP block with direct memory access to the FPGA configuration. At the moment the processor loads the bitstream from NVM to initialize the FPGA fabric, the malicious IP block begins to scan the main memory for the boot parameters while the processor is still booting. As soon as these parameters are found, they are modified in a way that the processor loads an unauthorized software image from a remote server over the network instead of continuing the boot from NVM. In fact, such an attack can only be successful if the processor already loaded and executed code to provide the required network capabilities. The authors provide countermeasures against this form of attack by applying a hardware wrapper for IP blocks to prevent unauthorized memory access. Other solutions exist in the form of hardware sandboxes as proposed in [28]. However, our following approach is fundamentally different in specifying a hardware-centric secure boot process, where the loading of tampered configurations from NVM to volatile memory is prevented by direct hardware authentication.

An approach similar to us addressing the secure boot on PSoCs, is Self-Authenticating Secure Boot (SASB) proposed by Pocklassery et al. in [12]. Here, first an unencrypted bitstream is loaded from NVM to implement a PUF architecture on the FPGA. In a second step, challenges are applied to the PUF to generate a device unique key and to perform selfauthentication of the loaded bitstream. Afterwards, the key is used to decrypt the user application for the unused portion of the FPGA as well as software that runs on the processor. The authors claim that the secure boot process is protected in a way that any modification made to the unencrypted bitstream results in key regeneration failure of the PUF. Potential drawbacks of this method are supposably significant resource requirements of the SASB implementation and the fact that not only the initial bitstream but also the required First Stage Bootloader (FSBL) is stored unencrypted on the device, which in consequence can be tampered. Moreover, neither the deployed device can be locked to its intended configuration nor is the configuration verified if the NVM memory gets manipulated after the boot was successful. Instead, we leverage existing vendor techniques by making use of the device ID



Fig. 1: Proposed security architecture involving a fully encrypted SD card as Non-Volatile Memory (NVM) storing the boot image as well as a file system from which a Programmable System-on-Chip (PSoC) is booted. The NVM interacts with the processor over a proposed Trusted Memory-Interface Unit (TMIU), which is loaded from a one-time programmable ROM (PROM) into the programmable logic of the FPGA.

provided internally by an FPGA and a unique ID of the NVM to form an unseparable unit of device and configuration. The integrity of swapped data after the secure boot is in our approach verified by calculating a hash for every sector exchanged between the processor and the NVM. Furthermore, as we will show, our solution considers not only the integrity but also the confidentiality of data during operation through hardware-based full memory encryption including the FSBL.

III. SYSTEM AND ATTACK MODEL

Our system architecture is any common PSoC as illustrated in Fig. 1, where an SRAM-based FPGA is tightly coupled with one or multiple processors integrated on a single chip. Both the processor and the FPGA have access to an external main memory (DDR), where data is transferred after successful boot. Yet, the data exposure of this memory by, for instance, pin probing is not considered in this work. Instead, we consider the security vulnerabilities caused by access to NVM. Since SRAM-based FPGAs employ volatile memory, our approach expects the system to start the boot process from a small onetime programmable ROM (PROM) to provide an initial FPGA configuration after power-up. The PROM on the PSoC must be programmed ahead of shipment to contain the encrypted and signed TMIU bitstream. This bitstream is loaded initially into a dedicated area of the FPGA to serve as a trusted anchor between the processor and an NVM device from which subsequently, the operating system (kernel images and device trees), partial bitstreams, and even entire file systems are booted.

As for the attack model, we assume that the goal of an attacker is to access or modify proprietary and sensitive data stored on the NVM. This includes IP in the form of object code intended to run on the processor, full or partial hardware designs, or sensitive user data. Furthermore, it is assumed that the adversary has full physical access to the NVM device and can monitor and modify all communication lines to/from



Fig. 2: Flow diagram of the proposed hardware-centric 4-stage secure boot process from Non-Volatile Memory (NVM).

the NVM. Invasive attacks, including destructive methods to manipulate FPGA internals, system or component package damages, as well as denial of-service attacks are not taken into account. Again, attacks on the unprotected main memory for which countermeasures exist, e.g., [29], are not in our scope. Side channel attacks such as the analysis of power traces collected from the cryptographic operations performed inside the TMIU are in the scope of future work. We mainly address the integrity and confidentiality of the system's data stored on NVM and, based on this, conclude a secure boot process and operation. Moreover, we assume that the NVM content is fully encrypted using a PSoC-internally generated key and shipped together with the device. The initial configuration of the NVM is created and transferred encrypted by the PSoC without the used key leaving the device. In case the NVM should be stolen, the information on the NVM still remains confidential due to encryption, but the PSoC will not boot as desired. Further details of the key generation process are discussed in Section IV-B.

IV. PROPOSED SECURE BOOT PROCESS

This section describes the secure boot process for PSoCs from an encrypted mass storage NVM device. The general approach is based on the idea of an isolated execution of security-critical operations in the reconfigurable logic of the FPGA to guarantee a trustworthy system.

A. Boot Process

Figure 2 illustrates the proposed 4-stage boot process providing a hardware-based chain of trust to the NVM that includes the boot image of the PSoC. This 4-stage process is explained in the following. In stage 1), after power-on, the Trusted Memory-Interface Unit (TMIU) according to Fig. 1 is loaded from the PROM to a designated area of the reconfigurable logic region of the FPGA. The TMIU architecture itself will be described in details in Section IV-C, see also Fig. 3.

The PSoC is authenticated by a unique, non-volatile device identifier denoted as $ID_{dev.}$. For $ID_{dev.}$ we make use of a 57-bit, read-only, unique board-level-identifier that Xilinx calls

Device DNA [14]. This Device DNA is burned into an E-Fuse register during the manufacturing process and can only be internally read by the FPGA design (JTAG needs to be disabled ahead of shipment). Similar mechanisms are offered also by other FPGA vendors such as Intel/Altera over their ALTCHIP_ID Port [30]. In our implementation, the TMIU is reading out this register after power on. If the identifier is not matching a cryptographic hash compiled into the TMIU bitstream itself, the system will go into a secure lockdown mode. Other essential peripherals for booting from NVM such as clocks, General-Purpose I/Os (GPIOs), and memory controller are also initialized at this stage. Last in stage 1), to enable the communication between the NVM and the processor of the PSoC, a irreducible minimum of software is executed to establish the NVM communication protocol.

Once the TMIU has been loaded, initialized, and the PSoC device is authenticated successfully, the system goes into a memory identification mode (cf. Fig. 2 stage 2) to authenticate the connected NVM. In our following experiments, we use an SD card as non-volatile mass storage device. This card identifies itself via its unique 128-bit Card Identification number (CID), which is common praxis for memory identification and exist also for Flash and other NVM devices. The CID, which is factory-stamped and unchangeable, is encoded in the cards internal registers. For this reason, as long as the card complies to the official SD standard, the CID value denoted as ID_{NVM} can be used to lock the PSoC with device identifier ID_{dev} . uniquely together with the SD card with identifier ID_{NVM} . If one does not trust the CID alone, then for instance, the Card-Specific Data (CSD) register or other card internal information can be used in combination for authentication. The TMIU compares the ID_{NVM} number with a reference checksum also compiled into the bitstream to determine whether it is safe to activate the memory's data transfer function. In the situation where a different NVM is deployed, the ID_{NVM} is consequently not matching with the calculated checksum. In this case, all I/O functions of the NVM are suspended and the overall system will go into a secure lockdown mode.

The third stage, also implemented fully in hardware, involves the key generation with subsequent boot image decryption and authentication. Here, the memory identifier ID_{NVM} is used together with the internally-read device identifier ID_{dev} to perform on-the-fly key generation. As it will be discussed more detailed in Section IV-B, this guarantees a secure generation of the secret AES key denoted as K_{AES} to decrypt the boot image and other data stored on the NVM. After decryption, two additional authentication checks are performed. Due to the fact, that we assume full encryption of data on the NVM, we authenticate in a first step the encrypted Master Boot Record (MBR) of the NVM including partition tables and other metadata. The MBR is widely used and has established itself as the de facto standard partition table for storage media of all kinds. In a second step, the integrity of the entire boot image is checked by means of a SHA digest calculation. This is done by padding the unencrypted boot image in a secure environment to a suitable message length and appending the corresponding hash token denoted as T_{auth} , before storing it encrypted on the NVM. At boot time and after successful decryption of the overall boot image, the calculated hash is compared against the appended one. In this way, any tampering of the encrypted boot image will be detected through a different digest value, which in turn, will lead to an immediate termination of the boot process. Moreover, after successful boot, the system stays upgradable at any time for secure remote updates/upgrades performed by a trusted authority. After an authenticated remote login, a boot image could then even be replaced by a newer version on the boot partition of the NVM. In that case, after an automatic reboot cycle, the system would load the new configuration. Alternatively, the old boot image could be kept as a backup if space permits and serve as a fallback in an event, where the new boot image could not be loaded as expected. Thus, the entire system remains flexible and reduces in consequence the total costs of ownership.

We assume that the boot image can either contain one or multiple partial bitstreams to initialize the unutilized FPGA logic in combination with a bare-metal processor application or a Second Stage Bootloader (SSBL) such as U-Boot¹ to deploy a Linux-based Operating System (OS). Persistent data storage requires a second data partition to mount the appropriate encrypted file system. Not only during the boot process, but also during the normal operational mode of the system, the TMIU will retain the full memory en-/decryption and hash calculation, for instance, when data is swapped to/from main memory.

Stage 4: Only if the boot partition has been successfully loaded, the TMIU will hand over control to the processor system on the PSoC to setup the remaining operating system and finally starts the user application.

In summary, if any stage stops legitimization, the system will go into a secure lockdown mode, which prevents unintended system behavior and data release. Hereafter, we describe the key generation scheme and the implementation of the TMIU in detail.

B. Key Generation Scheme

As mentioned in Section II, FPGA vendors provide onchip key storage for bitstream decryption. To hamper the risk of key theft, we generate the keys for decrypting the boot image and other data stored on the NVM only after authentication, e.g., only if the combination of a PSoC with the device identifier ID_{dev} and the NVM identifier ID_{NVM} are successfully authenticated. This on-the-fly key generation is performed by applying the Concatenation Key Derivation Function (CKDF) [31]. As unique salt we utilize the memory identifier ID_{NVM} denoted as the byte-string OtherInfo and concatenate this together with the secret device identifier ID_{dev} . and a counter value c. In this way, the CKDF uses the SHA implementation embedded in the TMIU (cf. Fig. 3) to calculate a pseudorandom Hash-function H() for key derivation. Here, the CKDF is applied as a cryptographic secure key expansion function to derive the required 128-bit key for the AES from the 57-bit ID_{dev} , while at the same time the difficulty of a brute force attack increases by the number of iterations specified trough c.

The output of this calculation is an FPGA-internal unique secret, based on the external memory identifier ID_{NVM} and the private device identifier ID_{dev} that can be used as a symmetric de-/encryption key. Equation (1) shows this derivation to generate the secret AES key K_{AES} .

An alternative to the vendor-provided device IDs could be to rely, for some use cases, on a PUF implementation for device authentication as proposed in [13, 24]. However, in addition to extra costs in terms of FPGA resources for a proof of concept implementation, we decided to go for the vendor ID.

$$K_{AES} = H(c||ID_{dev.}||OtherInfo)$$
(1)

The TMIU reads the unique device identifier at the time power is applied and compares this number to a reference checksum compiled into the TMIU bitstream. The same applies to the NVM identifier ID_{dev.}, at the memory identification stage. So even if an attacker could read out the cards internal CID register or probes the communication signals, no plaintext attack on the key is feasible, because the attacker has no possibility to obtain the FPGA internal ID_{dev} from a locked (i.e., JTAG disabled) device. In addition, the keys are only applied within the programmable logic of the PSoC. Furthermore, a reset or power shutdown clears all generated keys and information. It follows that the card or any other connected memory device behaves similar to a *passive dongle* to tie permanently and immutable proprietary IP to an authorized device. Replacing either the memory device or changing its content or connecting a different PSoC device would result in a key generation failure and prevent the system from booting. Moreover, the NVM itself is only read- and writable in combination with the intended PSoC device. In this context,

¹https://www.denx.de/wiki/U-Boot/



Fig. 3: Trusted Memory-Interface Unit (TMIU) building blocks enabling a secure boot from external Non-Volatile Memory (NVM).

also different key handling or diversification procedures are conceivable. For instance, multiple encryption keys could be used across multiple memory partitions to further reduce the attack surface of the system.

C. Trusted Memory Interface Unit

To get a better understanding of how the TMIU interacts with the NVM device, which is in our case the SD card, first a brief introduction of the required Secure Digital Input/Output (SDIO) protocol specification is given. The SDIO protocol is the standard not only for removable SD cards but also for their on-board embedded counterpart the embedded Multi Media card (eMM card) and applies the master/slave principle, where a host controller communicates over two dedicated interfaces with the memory. A data bus is used to read or write data from the host to the memory on a bidirectional data interface (DATA). Here, data transfers to/from the SD card are performed in a single or multi-block read/write fashion. A block represents the data of a specific memory sector of 512 bytes on the card and is always followed by its 16-bit polynomial Cyclic Redundancy Check (CRC) value. This block-based communication allows our sector-wise de-/encryption and hash calculation of the memory sections. In addition, data transfers are triggered after the controller issues specific commands over a bidirectional command interface (CMD). These commands regulate the execution of protocol routines based on responses received from the memories internal controller. Similar to the data bus, every command sequence is protected by a 7bit CRC. The case that the calculated CRC value, either for commands or data transmissions, does not match the attached one, triggers a repetition which adds an additional layer of security to the protocol.

The TMIU is integrated as an intermediate instance to monitor and control the communication behavior between memory and host. Figure 3 provides a high-level description of its building blocks. As can be seen, the ports for the data and command lines are the only access points of the TMIU interfacing the processor and the connected NVM. On the right hand side, the ports towards the processor system are shown. The commands sent and received by the processor are observed by

the component NVM_CMD Controller within the TMIU. This controller serves not only for authentication but also to regulate the communication sequence between the processor system on the PSoC and the NVM. More precisely, if any tampering on either memory or processor side occurs, the NVM_CMD Controller would intervene and immediately terminate the transmission. As mentioned earlier, a deployed SD card needs to authenticate itself via its CID during the memory identification stage at boot-time. As soon as the card sends the CID, the NVM CMD Controller proofs and forwards this value to a Key Generator module. The Key Generator checks whether the received memory identifier ID_{NVM} and the internally-read device identifier ID_{dev} complies with the pre-initialized checksums and reports this back to the NVM_CMD Controller before triggering the generation of the 128-bit AES key K_{AES} . After successfully finishing the memory initialization and authentication step, the NVM_CMD Controller permits the processor to transfer data and keeps track of the accessed sector numbers.

If not carefully designed, the TMIU with its cryptographic operations would have the potential to heavily slow down not only the boot process but also general system performance. As high data throughput from memory to PSoC and vice versa is a must, special care has been taken in the implementation of the dedicated NVM_DATA Controller. In particular, all internal components are interconnected by a streaming interface. This interface is designed for high-speed data throughput and supports burst transmissions of unlimited size. Therefore, no address mechanism or explicit synchronization is needed, which makes it ideal for pipelined data streaming. However, incoming data from the memory or the processor must first be proven non-faulty, e.g., against any transmission errors (e.g., bit flips). This is done by CRC calculation before data is forwarded to the AES de-/encryption module. If the CRC check is not successful, the data is sent unencrypted to the PSoC to trigger a CRC error resulting in a new transmission. After de-/encryption, the CRC value is calculated again and subsequently attached to the data block before forwarding it to the PSoC/NVM.

Our AES core supports sector-wise both de- and encryption

and is switching between these two modes depending on the communication direction. The key which was used initially for encrypting the memory content in the secure environment ahead of shipment is now also applied when writing/reading data to/from NVM at boot-time and during the operational mode of the system. In this way, we can guarantee that at any point in time, only encrypted data is stored on NVM. Moreover, the NVM content is only deployable on the intended PSoC device.

The NVM_DATA Controller utilizes the 256-bit SHA algorithm to compare the calculated boot image hash token against the sent one $T_{auth.}$. If the calculated hash is not matching the appended one, the NVM_DATA Controller modifies the last byte to provoke a CRC error on the processor side to invalidate the data transmission, while the NVM_CMD Controller disables any further attempts to transfer data. In a similar fashion, sector authentication is performed after successful booting, when reading or writing data to the NVM. In this way, every sector is stored with a hash and fully encrypted on the NVM making any manipulation immediately detectable. Later, when a reset or power-off is applied, all internal registers are cleared and the TMIU will again start the proposed multi-stage boot process.

Finally, the TMIU is supposed to be clearly separated from the user design, while the remaining non-configured regions are free and can be used for user applications. This gets possible through the partial reconfiguration and isolated place and route capabilities of modern FPGAs [32]. In particular, it allows us to dynamically perform partial reconfigurations of certain independent regions to update the desired system functionality when the system is applied in the field. Therefore, the TMIU with all its security sensitive primitives is logically and spatially isolated and runs totally independent from other applications.

V. EXPERIMENTAL RESULTS

In this section, our proposed hardware-centric boot process and TMIU design is evaluated on a Xilinx Zynq xc7z010clg400-1 placed on the Digilent Zybo evaluation board, see Fig. 4. For a proof of concept, an SD card has been chosen as non-volatile mass data storage device for the following reasons: SD as well as eMM cards are cost effective due to their high memory density and good cost-per-bit ratio, making them suitable for storing relatively large amounts of data such as user data. Moreover, they can be easily used in a number of small, lightweight and low-cost systems due to their low-power consumption and standard sizes, which is a common requirement for many embedded and IoT devices. Nevertheless, the approach is not restricted to SD cards. Also different forms of NVM with similar properties such as Solid-State Drives (SSDs) or Flash chips are possible.

In order to successfully boot from a Zynq device, the experimental setup illustrated in Fig. 4 was required: As a PROM which would allow to store the bitstream of our TMIU that needs to be loaded initially is not available on the Zynq, we used an on-board (bottom side) available 17 MB



Fig. 4: Secure boot setup on a Xilinx Zynq evaluation board.

programmable Flash. This Flash is connected over a SPI-Flash controller with the processing system to emulate our PROM and assumptions introduced in Section III. The storage requirement for the encrypted TMIU implementation is 1.9 MB in total, with the bitstream accounting for the major part of the storage size. Beside the Flash memory, a 16 GB SD card was connected via an external MicroSD card slot to the PSoC. The card was formatted with one 100 MB FAT32 bootable partition containing the required boot image, device tree and the Linux kernel image. The remaining card space was utilized as ext4 partition to provide the Linux root file system. Furthermore, in our evaluation the boot process involves the configuration of the processor and the hardware. Therefore, the boot image includes a partial FPGA configuration in combination with the Second Stage Bootloader (SSBL) (U-Boot in this case) to load the kernel image and setup a Linux OS. Next, the processing system on the Zynq is routed via its SDIO interface to the TMIU ports on the FPGA. The clock speed of the TMIU adapts during the memory initialization phase according to the connected card standard. In this work, we were using a high speed card clocked by 50 MHz. To visualize the in Fig. 2 proposed 4-step boot process, four status LEDS were used indicating every successful authentication.

Furthermore, the Xilinx Vivado Design suite 2018.1 was utilized to synthesize the TMIU on the aforementioned Zynq PSoC. Here, the design objectives performance, power, and resource costs were collected at a 20 ns clock cycle time. The amount of required FPGA resources for the TMIU implementation in terms of Flip-Flops (FFs), Lookup Tables (LUTs), and 36K BRAMs – no Digital Signal Processor (DSP) 48-slices were needed – is highlighted in Table I. The numbers indicate that, with 39% of LUTs and 17% of FFs on the second smallest PSoC from the Zynq family, a TMIU implementation is even feasible on entry-level PSoC devices.

Concerning power consumption, an estimation including both static and dynamic power of the overall design including the TMIU netlist was obtained using the Vivado Power analysis tool. The switching activity was derived from constraints and simulation files. As a result, considering the additional FPGA resources introduced by the TMIU, the overall power TMIU Bitstream = 1.9 MBoot Image + Linux Kernel + Device Tree = 13 MB consumption of the design rises from 1.53 to 1.62 Watt, which is an overhead of only 5%. In this overall power, the processor consumes about 92% of the dynamic on-chip power, while clock and register activity of the TMIU contributes to 8% of the dynamic power. The static device power amounts to 7% of the overall power consumption.

In the following, we evaluate the boot time and achievable data transmission rate between NVM and PSoC using the proposed TMIU concept and implementation. Figure 5 shows the time needed for loading the TMIU configuration and the First Stage Bootloader (FSBL) from a PROM including the time for TMIU initialization and mutual device authentication (steps 1-3 in Fig. 2) which amounts to 98 ms corresponding to a throughput of $19.4 \,\mathrm{MB \, s^{-1}}$. Thereafter, the TMIU continues booting the Linux OS from the NVM. In our experiment, data with a total size of 13 MB for the required boot image, device tree and the Linux kernel image is loaded. The time for this subsequent boot from an SD card specified to provide a maximal line rate of 25 MB s⁻¹ was measured as 526 ms corresponding to a data rate of 24.7 MB s⁻¹. Therefore, the TMIU design does not reduce the achievable throughput of the NVM device and perfectly scales with the amount of data loaded at boot time. Concerning latency, the decryption and authentication of data in hardware takes 52 clock cycles to process a sector of size 512 Bytes. Therefore, the boot time is limited only by the bandwidth of the chosen NVM medium and its interface. Furthermore, resource, power, and timing overheads caused by the proposed TMIU approach are tolerable for the sake of security. An evaluation of alternative NVM devices is subject of future work.

VI. CONCLUSION AND FUTURE WORK

In this paper, we presented a novel approach for checking authenticity of Non-Volatile Memory (NVM) and the integrity of stored boot images for programmable System-on-Chip (SoC) devices. Here, apart from boot ROMs, NVM devices such as SD and eMM cards or Flash memories are typically used due to their high capacity. In order to prevent any fraudulent exchange of the memory device or modification

TABLE I: Resource requirements of the proposed TMIU implementation and its cryptographic building blocks.

Block	Num.	LUTs	FFs	BRAMs
Key Generator	abs.	70	249	0
	(%)	0.4	0.7	0
NVM_CMD Controller	abs.	83	331	0
	(%)	0.5	0.9	0
NVM_DATA Controller	abs.	6630	5354	0.5
	(%)	37.7	15.2	0.8
Total	abs.	6783	5934	0.5
	(%)	38.5	16.9	0.8

PROM SD-Card



Fig. 5: Performance of the Trusted Memory-Interface Unit (TMIU)-based secure boot. In the first phase, the bitstream of the TMIU is loaded and initialized from PROM. Subsequently, the boot process continues from an authenticated NVM (in this case an SD card). As can be seen, the data rate achieved is close to the 25 MB s^{-1} line rate of the SD card.

of its content, a fully hardware-centric solution is proposed in which a so-called Trusted Memory-Interface Unit (TMIU) is loaded first into the available reconfigurable region of the FPGA, which then initializes the communication interface of the PSoC with the NVM device including authentication, integrity checking, and de-/encryption of data. A 4-stage boot process and its hardware implementation have been evaluated in terms of resource utilization, power, and performance. As a result, the lightweight, low-power TMIU implementation can be used already in quite small, even IoT devices. Moreover, the proposed protocol has been shown to not limiting the speed of the boot process from NVM. Additionally, external key storage for decryption is avoided through on-the-fly key generation by making use of unique, factory-stamped IDs given by the device and the NVM. Due to the fact that our TMIU design and proposed protocols do not use any vendor-specific hardware or software primitives, our approach can target any PSoC platforms integrating processor and FPGA resources on a chip.

In future work, we want to investigate more deeply the applicability of the proposed approach in combination with dynamic update/upgrade services and their requirement for secure off-chip storage including policies for fail-safe fallback modes if these updates fail. Furthermore, it is planned to investigate the vulnerability of the approach to side-channel attacks. Last but not least, we intend to analyze the approach also for other types of NVM devices.

ACKNOWLEDGMENT

The work has been supported by the Schaeffler Hub for Advanced Research at Friedrich-Alexander University Erlangen-Nürnberg (SHARE at FAU).

REFERENCES

- [1] F.-J. Streit et al. "Model-Based Design Automation of Hardware/Software Co-Designs for Xilinx Zynq PSoCs." In: 2018 International Conference on ReConFigurable Computing and FPGAs (ReConFig). IEEE. 2018, pp. 1-8.
- [2] Xilinx with Κ. Morris. Hits the Road Daimler SoCs to Power Automotive AIApplications. https://www.eejournal.com/article/xilinx-hits-the-road-withdaimler. Accessed: April 2019.

- [3] F.-J. Streit et al. "High-Level Synthesis for Hardware/Software Co-Design of Distributed Smart Camera Systems." In: *Proceedings of the 11th International Conference on Distributed Smart Cameras.* ICDSC 2017. Stanford, CA, USA: ACM, 2017, pp. 174–179.
- [4] D. Firestone et al. "Azure Accelerated Networking: Smart-NICs in the Public Cloud." In: 15th {USENIX} Symposium on Networked Systems Design and Implementation ({NSDI} 18). 2018, pp. 51–66.
- [5] X. Zhai, A. A. S. Ali, A. Amira, and F. Bensaali. "ECG Encryption and Identification based Security Solution on the Zynq SoC for Connected Health Systems." In: *Journal of Parallel and Distributed Computing* 106 (2017), pp. 143–152.
- [6] G. Naumovich and N. Memon. "Preventing Piracy, Reverse Engineering, and Tampering." In: *Computer* 36.7 (2003), pp. 64– 71.
- [7] C. Cimpanu. Unpatchable security flaw found in popular SoC boards. https://www.zdnet.com/article/unpatchable-securityflaw-found-in-popular-soc-boards/. Accessed: November 2019.
- [8] S. Drimer. "Volatile FPGA design security-a survey." In: *IEEE Computer Society Annual Volume* (2008), pp. 292–297.
- [9] R. S. Chakraborty, I. Saha, A. Palchaudhuri, and G. K. Naik. "Hardware Trojan Insertion by Direct Modification of FPGA Configuration Bitstream." In: *IEEE Design & Test* 30.2 (2013), pp. 45–54.
- [10] T. Eisenbarth et al. "Reconfigurable Trusted Computing in Hardware." In: *Proceedings of the 2007 ACM workshop on Scalable trusted computing*. ACM. 2007, pp. 15–20.
- [11] T. Wollinger, J. Guajardo, and C. Paar. "Security on FPGAs: State-of-the-Art Implementations and Attacks." In: ACM Transactions on Embedded Computing Systems (TECS) 3.3 (2004), pp. 534–574.
- [12] G. Pocklassery, W. Che, F. Saqib, M. Areno, and J. Plusquellic. "Self-Authenticating Secure Boot for FPGAs." In: 2018 IEEE International Symposium on Hardware Oriented Security and Trust (HOST). IEEE. 2018, pp. 221–226.
- [13] J. Aarestad, P. Ortiz, D. Acharyya, and J. Plusquellic. "HELP: A Hardware-Embedded Delay PUF." In: *IEEE Design & Test* 30.2 (2013), pp. 17–25.
- [14] S. M. Trimberger and J. J. Moore. "FPGA Security: Motivations, Features, and Applications." In: *Proceedings of the IEEE* 102.8 (2014), pp. 1248–1265.
- [15] D. Ziener, S. Assmus, and J. Teich. "Identifying FPGA IP-Cores Based on Lookup Table Content Analysis." In: 2006 International Conference on Field Programmable Logic and Applications. IEEE. 2006, pp. 1–6.
- [16] S. Trimberger. "Trusted Design in FPGAs." In: Proceedings of the 44th annual Design Automation Conference. ACM. 2007, pp. 5–8.
- [17] S. Drimer. "Authentication of FPGA Bitstreams: Why and How." In: *International Workshop on Applied Reconfigurable Computing*. Springer. 2007, pp. 73–84.
- [18] A. Moradi, M. Kasper, and C. Paar. "Black-Box Side-Channel Attacks Highlight the Importance of Countermeasures." In: *Cryptographers' Track at the RSA Conference*. Springer. 2012, pp. 1–18.

- [19] A. Moradi, A. Barenghi, T. Kasper, and C. Paar. "On the Vulnerability of FPGA Bitstream Encryption against Power Analysis Attacks: Extracting Keys from Xilinx Virtex-II FPGAs." In: Proceedings of the 18th ACM conference on Computer and communications security. ACM. 2011, pp. 111–124.
- [20] S. Skorobogatov. "Flash Memory 'Bumping' Attacks." In: International Workshop on Cryptographic Hardware and Embedded Systems. Springer. 2010, pp. 158–172.
- [21] D. Ziener, J. Pirkl, and J. Teich. "Configuration Tampering of BRAM-based AES Implementations on FPGAs." In: 2018 International Conference on ReConFigurable Computing and FPGAs (ReConFig). IEEE. 2018, pp. 1–7.
- [22] D. Schellekens, P. Tuyls, and B. Preneel. "Embedded Trusted Computing with Authenticated Non-Volatile Memory." In: *International Conference on Trusted Computing*. Springer. 2008, pp. 60–74.
- [23] A. Maiti, L. McDougall, and P. Schaumont. "The Impact of Aging on an FPGA-based Physical Unclonable Function." In: 2011 21st International Conference on Field Programmable Logic and Applications. IEEE. 2011, pp. 151–156.
- [24] F. Tehranipoor, N. Karimian, K. Xiao, and J. Chandy. "DRAM based Intrinsic Physical Unclonable Functions for System Level Security." In: *Proceedings of the 25th edition on Great Lakes Symposium on VLSI*. ACM. 2015, pp. 15–20.
- [25] M. Wolf and T. Gendrullis. "Design, Implementation, and Evaluation of a Vehicular Hardware Security Module." In: *International Conference on Information Security and Cryptology*. Springer. 2011, pp. 302–318.
- [26] L. Sanders. "Secure Boot in the Zynq-7000 All programmable SoC." In: White Paper WP426 (v1. 0), Xilinx (2013).
- [27] N. Jacob, J. Heyszl, A. Zankl, C. Rolfes, and G. Sigl. "How to Break Secure Boot on FPGA SoCs through Malicious Hardware." In: *International Conference on Cryptographic Hardware and Embedded Systems*. Springer. 2017, pp. 425–442.
- [28] F. Hategekimana, T. J. Whitaker, M. J. H. Pantho, and C. Bobda. "Secure Integration of Non-Trusted IPs in SoCs." In: 2017 Asian Hardware Oriented Security and Trust Symposium (AsianHOST). IEEE. 2017, pp. 103–108.
- [29] J. Götzfried, T. Müller, G. Drescher, S. Nürnberger, and M. Backes. "RamCrypt: Kernel-based Address Space Encryption for User-Mode Processes." In: *Proceedings of the 11th ACM on Asia Conference on Computer and Communications Security*. ACM. 2016, pp. 919–924.
- [30] Intel. Chip ID Intel FPGA IP Cores User Guide. https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature Accessed: April 2019.
- [31] E. Barker, L. Chen, A. Roginsky, and M. Smid. Recommendation for Pair-Wise Key Establishment Schemes Using Discrete Logarithm Cryptography. SP 800-56A. National Institute of Standards and Technology. 2013.
- [32] Xilinx. Isolation Design Flow for Xilinx Zynq-7000 7 Series FPGAs orAPSoCs. https://www.xilinx.com/support/documentation/application_notes/xapp1222idf-for-7s-or-zynq-vivado.pdf. Accessed: July 2019.