Fun-SAT: Functional Corruptibility-Guided SAT-Based Attack on Sequential Logic Encryption

Yinghua Hu,¹ Yuke Zhang,¹ Kaixin Yang, Dake Chen, Peter A. Beerel, and Pierluigi Nuzzo Department of Electrical and Computer Engineering, University of Southern California, Los Angeles, CA, USA {yinghuah, yukezhan, kaixinya, dakechen, pabeerel, nuzzo}@usc.edu

Abstract—The SAT attack has shown to be efficient against most combinational logic encryption methods. It can be extended to attack sequential logic encryption techniques by leveraging circuit unrolling and model checking methods. However, with no guidance on the number of times that a circuit needs to be unrolled to find the correct key, the attack tends to solve many time-consuming Boolean satisfiability (SAT) and model checking problems, which can significantly hamper its efficiency. In this paper, we introduce Fun-SAT, a functional corruptibility-guided SAT-based attack that can significantly decrease the SAT solving and model checking time of a SAT-based attack on sequential encryption by efficiently estimating the minimum required number of circuit unrollings. Fun-SAT relies on a notion of functional corruptibility for encrypted sequential circuits and its relationship with the required number of circuit unrollings in a SAT-based attack. Numerical results show that Fun-SAT can be, on average, $90 \times$ faster than previous attacks against state-of-theart encryption methods, when both attacks successfully complete before a one-day time-out. Moreover, Fun-SAT completes before the time-out on many more circuits.

Index Terms—Logic Encryption, Hardware Security, SAT-Based Attack

I. INTRODUCTION

Integrated circuits (ICs) are often regarded as the root of trust of modern Internet-of-Things applications. However, their integrity and confidentiality can be seriously compromised by reverse engineering, among other threats, conducted by malicious parties in the supply chain. Various methods have been proposed to mitigate this threat, such as split manufacturing [1], gate camouflaging [2], and logic encryption [3]. Among these, logic encryption has gained significant attention over the past decade.

A class of logic encryption methods, namely, *combinational logic encryption* [4]–[7] aims to insert programmable elements and extra key ports into a portion of a circuit's combinational logic, so that the correct functionality can only be accessed by applying the correct

key. Models and metrics to help quantify the security and overhead of combinational logic encryption [8], [9] have been recently proposed and, consequently, securityoriented design tools [10]–[12] have started to appear. On the other hand, *sequential logic encryption* [13], [14] aims to create new states, marked as encrypted states, and modify the transitions in the circuit finite state machine. When powered on, the circuit is configured to be in an encrypted state and a predefined key sequence must be provided at the input ports before entering the true reset state.

A growing number of attacks have targeted combinational encryption methods over the years, the most notable being the SAT attack [15], based on Boolean satisfiability (SAT) solving. Given an encrypted netlist and a functional chip, i.e., an oracle providing the correct input/output response, the SAT attack searches for the correct key by solving a series of SAT problems that efficiently eliminate wrong keys. Because it assumes that the internal state is part of the input/output response, the SAT attack cannot be directly applied to a sequential circuit when the internal state is not scanned or is protected using a secure scan chain [16]. However, in this case, a SAT-based attack [17], [18] can still be developed by unrolling the sequential circuit to form a larger combinational circuit that represents the behavior of the original circuit over a number of clock cycles, and by applying the SAT attack to the unrolled version. A similar method can be used to formulate SAT-based attacks against sequential logic encryption [19]-[21].

A major challenge for these unrolling-based attacks on sequential circuits stems from the potentially large number of cycles a circuit needs to be unrolled in order to find the correct key, hence the growing size of the combinational circuits that need to be analyzed. To limit the size of the unrolled circuit, the attack usually starts by performing a SAT attack over a small number of unrollings. However, once the SAT attack terminates successfully, there is no guarantee that the set of candidate keys, obtained by matching the oracle response

¹Yinghua Hu and Yuke Zhang contributed equally to this work.

over a bounded time-horizon, will also match the circuit response for longer horizons. A model checking problem is then cast to verify the correctness of all the candidate keys. The attack gradually increases the unrolling depth and performs the SAT attack on the unrolled circuits until all the spurious keys are pruned out and the remaining keys are proven correct. Solving multiple instances of model checking and SAT attacks for growing unrolling depths can be expensive and drastically affect the feasibility of the overall attack.

This paper shows that the efficiency of SAT-based attacks on sequential logic encryption can be significantly improved by introducing an effective method to estimate the minimum number of unrollings needed to find the correct key. We propose Fun-SAT, a functional corruptibility-guided SAT-based attack, which relies on a notion of functional corruptibility for a sequential circuit to reduce both the SAT-attack effort spent to produce candidate key sets and the model checking effort spent to prove that a candidate key set is correct. Our contributions can be summarized as follows:

- We introduce a notion of functional corruptibility for sequential circuits and characterize its relation with the set of wrong keys that are pruned out by a SAT attack at each unrolling depth.
- We develop Fun-SAT, an attack to sequential logic encryption that leverages functional corruptibility to significantly reduce the overall execution time.
- We evaluate Fun-SAT on two state-of-the-art sequential logic encryption methods showing that, on average, it can be $90 \times$ faster than previous SAT-based attacks. Only 0.7% of the experiments timed out after one day, compared with 19% for the previous attack.

The remainder of the paper is organized as follows. Section II introduces two state-of-the-art sequential logic encryption methods and reviews the mechanism of the SAT-based attack on sequential logic encryption. Section III discusses the notion of functional corruptibility and its implications for SAT-based attacks. Section IV details the attack flow and implementation. In Section V, we validate the effectiveness of the proposed attack in comparison with the previous SAT-based attack. Finally, we conclude the paper in Section VI.

II. PRELIMINARIES

We first provide an introduction to sequential logic encryption and two state-of-the-art methods in this category. Then, we illustrate the mechanism of existing SATbased attacks on sequential logic encryption.

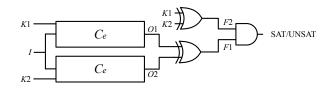


Fig. 1. Circuit visualization of the SAT instance at the first iteration of the SAT attack.

A. Sequential Logic Encryption

Sequential logic encryption methods encrypt the finite state machine (FSM) of a circuit via additional states and transitions [13], [14], [19], [22]. The FSM can operate in the *encrypted mode* or in the *functional mode*. After reset, the encrypted circuit is in the encrypted mode. It will transition to the functional mode, exhibiting the correct functionality, once it is provided with a correct sequence of multi-bit inputs, i.e., a correct key sequence, via the primary input ports. In this paper, we focus on two representative state-of-the-art sequential encryption methods, namely, *HARPOON* [13] and *Interlocking* [14], but describe applications to other decryption mechanisms in Section V.

In *HARPOON* [13], only a single path is designed from the encrypted to the functional mode, which makes the scheme potentially vulnerable to attacks that can analyze the state transition diagram of the encrypted FSM to recognize the single transition from the encrypted to the functional mode [19]. *Interlocking* [14] addresses this vulnerability by designing multiple paths between the encrypted and the functional mode so that the boundary between the logic in the two modes is less distinguishable. The circuit operates correctly only if the correct path is taken by providing the associated key sequence. Otherwise, errors will still occur despite the circuit enters the functional mode.

B. SAT-Based Attacks

The traditional SAT attack [15] as well as other SATbased attacks assume the availability of two resources: the encrypted circuit netlist C_e and an oracle circuit C_o , i.e., a black box providing the correct input/output response. The traditional SAT attack [15] can find the correct key of a combinational circuit which has no internal loops. The attack first constructs a SAT instance based on the circuit in Fig. 1, where I denotes the input ports, K1 and K2 the key ports, and O1 and O2 the output ports. Once a SAT instance is solved, the satisfying (SAT) assignment identifies an input *i* for which two different keys k_1 and k_2 lead to two different outputs. This input, called a *distinguishing input pattern* (DIP), will be used to query the oracle C_o for the

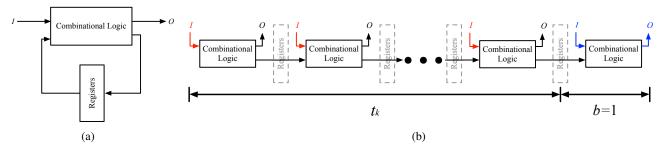


Fig. 2. Schematic of (a) a sequential circuit and (b) its unrolled version.

corresponding correct output. The input/output pair from the oracle is then encoded into a set of clauses that are appended to the current SAT instance. Once a DIP i^{dip} is found, the updated SAT instance effectively prunes out of the search space a set of wrong keys \overline{K} as follows,

$$\overline{K} = \{k | f'(i^{dip}, k) \neq f(i^{dip})\}$$

where f and f' are the functions implemented by C_o and C_e , respectively. The attack terminates when the updated SAT instance becomes unsatisfiable, meaning that all the wrong keys have been excluded, and any key in the remaining set can be returned as correct.

Because the SAT attack assumes that the internal state is part of the input/output response, it cannot be directly applied to sequential circuits when the internal state is not scannable. A set of SAT-based attacks [17], [18] have circumvented this limitation by leveraging circuit unrolling and model checking. Similarly, the SAT attack can be extended to sequential logic encryption by unrolling a sequential circuit, as shown in Fig. 2, to form a larger combinational circuit that represents the behavior of the sequential circuit over a fixed number of clock cycles [19]–[21]. We assume that the attacker knows the length of the key sequence t_k . The minimum number of unrollings required to start the attack is then $t_k + 1$. The input ports in red and blue are treated as key ports and input ports, respectively, for the unrolled circuit. The output ports in blue act as the circuit output.

Algorithm 1 summarizes the flow of this attack. The combinational circuit in Fig. 2 allows performing a SAT attack (line 3) to search for DIPs¹ that can prune out wrong keys. However, once a SAT attack terminates successfully for $t_k + b$ unrollings, there is no guarantee that the set of candidate keys, obtained by matching the oracle response over *b* cycles, will also match its response after *b* cycles. A model checking problem [18] can then be formulated (line 4) to verify whether this is the case, by taking as input one of the candidate keys

Algorithm 1 Reference SAT-Based Attack [17]–[19]

Input: Encrypted netlist C_e , oracle C_o , key sequence length t_k

Output: Correct key sequence k^*

b)

 k^* , the list of DIPs L_{dip} and their corresponding outputs L_{odip} generated by the SAT attack in line 3. Otherwise, the attack will try a different number of unrollings determined by an update function (line 5) and repeat this process until all the remaining keys are proven correct. The update function usually increments or multiplies *b* by a constant number. However, without any guidance on the unrolling depth that is required to eliminate all the wrong keys, Algorithm 1 tends to still require many SAT and model checking problems to be solved, especially when the required unrolling depth is large. Fun-SAT aims to significantly improve the efficiency of this attack on sequential logic encryption by directly estimating the number of unrollings that are required to prune out all the wrong keys.

III. BOUNDED-DEPTH FUNCTIONAL CORRUPTIBILITY

We introduce a notion of functional corruptibility (FC) for sequential circuits and discuss how it will be used to estimate the minimum number of required circuit unrollings for a successful SAT-based attack. Consistently with the literature, we assume the attacker's access to the encrypted netlist C_e , the black-box oracle C_o , and

¹For sequential circuits, a DIP can also be called a *distinguishing input sequence* (DIS) [17].

the key length t_k . We discuss extensions to the case of unknown t_k in Section V. In the following, we say that the *unrolling depth* is b for C_o and C_e to mean that the circuit is unrolled for b and $t_k + b$ cycles, respectively.

A. FC and Unrolling Depth

We denote by b_{req} the minimum number of unrollings required to prune out all the wrong keys for a sequential SAT-based attack. Let I and O be the sets of input and output ports of both C_o and C_e , respectively. Let $f_b : \mathbb{B}^{b|I|} \to \mathbb{B}^{b|O|}$ be the function implemented by the *b*-unrolled version of C_o , i.e., the function represented by the combinational circuit C_o^b obtained after unrolling C_o for *b* cycles. We also say that C_o^b has depth *b*. Similarly, we denote by $f'_b : \mathbb{B}^{b|I|} \times \mathbb{B}^{t_k|I|} \to \mathbb{B}^{b|O|}$ the *b*-unrolled version C_e^b of C_e . We also denote by SAT(b)the traditional SAT attack on C_e^b and by \overline{K}_b the set of wrong keys pruned out by SAT(b). Finally, we denote by |p| the length of a sequence *p* and recall that a partial order can be defined over sequences as follows.

Definition 1 (Partial Order Over Sequences). Let p and q be two sequences with |p| < |q|. We say that p (strictly) precedes (or is less than) q, written $p \prec q$, if and only if the following holds:

$$p_i = q_i, \forall i \in \{1, 2, ..., |p|\},\$$

where p_i is the *i*-th element of *p*, that is, if and only if *p* is a prefix of *q*. Otherwise, we say that *p* does not precede *q*, *i.e.*, $p \not\prec q$.

For example, $0110 \prec 011011$ holds while we have $0010 \not\prec 011011$. We introduce a notion of functional corruptibility for a sequential circuit by resorting to its *b*-unrolled version as follows:

Definition 2 (b-Depth Functional Corruptibility). The bdepth functional corruptibility of a circuit pair (C_e, C_o) is the ratio between the number of corrupted output values of C_e^b with respect to C_o^b and the total number of primary input and key combinations for C_e^b , i.e.,

$$FC_b = \frac{1}{2^{(b+t_k)|I|}} \sum_{i \in \mathbb{B}^{b|I|}} \sum_{k \in \mathbb{B}^{t_k|I|}} \mathbb{1}(f_b(i) \neq f'_b(i,k)),$$

where $\mathbb{1}(.)$ is the indicator function.

To study how FC_b evolves with b, we associate a tag to the errors introduced by f'_b , the function implemented by the b-unrolled version C_e^b of the encrypted circuit.

Definition 3 (Error Tag). We can associate a tag to an input $i \in \mathbb{B}^{b|I|}$ and a key $k \in \mathbb{B}^{t_k|I|}$ via the map \mathcal{T}_b :

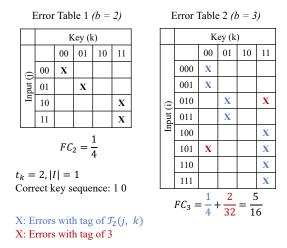


Fig. 3. Error distributions of a small encrypted circuit (|I| = 1 and $t_k = 2$) for the first two and three clock cycles.

$$\mathcal{T}_{b}(i,k) = \begin{cases} \perp, \text{ if } f'_{b}(i,k) = f_{b}(i); \\ 1, \text{ if } f'_{b}(i,k) \neq f_{b}(i) \text{ and } b = 1; \\ b, \text{ if } f'_{b}(i,k) \neq f_{b}(i), \ b > 1, \\ \text{ and } f'_{b-1}(j,k) = f_{b-1}(j); \\ \mathcal{T}_{b-1}(j,k), \text{ otherwise}; \end{cases}$$

 $\mathbb{R}^{b|I|} \times \mathbb{R}^{t_k|I|} \to \mathbb{N} \cup \{ \mid \}$ defined as follows:

where $j \prec i$ and $j \in \mathbb{B}^{(b-1)|I|}$.

For example, Fig. 3 shows two tables marking the errors introduced by f'_b for b = 2 and b = 3, with |I| = 1 and $t_k = 2$. Each entry is indexed by an input value i and a key value k. If $f'_b(i, k) \neq f_b(i)$, we mark the corresponding entry with an "x." By Definition 3, the errors marked in red are tagged with 3, while the blue ones depend on errors that were already introduced by f'_2 and will be tagged based on the error tags they had in f'_2 . We can then state the first result describing the behavior of FC_b .

Theorem 1. For all b > 1, $FC_b = FC_{b-1}$ holds if and only if $\mathcal{T}(i,k) < b$ holds $\forall i \in \mathbb{B}^{b|I|}, \forall k \in \mathbb{B}^{t_k|I|}$, i.e., if and only if no new errors, i.e., errors tagged by b, are introduced by f'_b .

Proof. We first prove that $FC_b = FC_{b-1}$ holds if f'_b does not introduce new errors, i.e., errors tagged by b. Suppose that n_{b-1} is the number of errors introduced by f'_{b-1} . Assume that an input $j \in \mathbb{B}^{(b-1)|I|}$ and a key $k \in \mathbb{B}^{t_k|I|}$ lead to an output error, i.e., $f_{b-1}(j) \neq f'_{b-1}(j,k)$ holds. By Definition 1, there are $2^{|I|}$ inputs i such that $i \in \mathbb{B}^{b|I|}$ and $j \prec i$ holds. Therefore, f'_b inherits $n_{b-1}2^{|I|}$ errors from f'_{b-1} . By Definition 2, we obtain

$$FC_b = \frac{n_{b-1} \cdot 2^{|I|}}{2^{b|I|+t_k|I|}} = \frac{n_{b-1}}{2^{(b-1)|I|+t_k|I|}} = FC_{b-1}$$

We now prove that f'_b does not introduce new errors if $FC_b = FC_{b-1}$ holds. Suppose by contradiction that $FC_b = FC_{b-1}$ holds and f'_b introduces indeed new errors. Let $n^{<b}$ and $n^{=b}$ be the number of errors with tags less than and equal to b in f'_b , respectively. By Definition 3, the number of errors in f'_{b-1} is

$$n = \frac{n^{$$

Therefore, we have

$$FC_{b-1} = \frac{n}{2^{(b-1)|I|+t_k|I|}} = \frac{n^{< b}}{2^{b|I|+t_k|I|}},$$

and

$$FC_b = \frac{n^{$$

leading to $FC_{b-1} < FC_b$, which violates our initial assumption.

From Theorem 1 and its proof we infer that FC_b can only remain constant or increase with b as new errors, tagged by b, are observed at the output of the b-unrolled circuit. This leads to the following result, stating that FC_b monotonically increases with b, independently of the sequential encryption method adopted.

Corollary 1.1. For all b > 1, we obtain $FC_b \ge FC_{b-1}$.

B. FC and Key Search Progress

The *b*-depth functional corruptibility can be related to the set \overline{K}_b of incorrect keys that are excluded by SAT(b). To establish this relation, we first provide a characterization of \overline{K}_b using the following lemma.

Lemma 2. Let \overline{K}_b be the set of wrong keys pruned out of the search space upon termination of SAT(b). Then, $\forall i \in \mathbb{B}^{b|I|}$, the following holds:

$$\{k|f_b(i) \neq f'_b(i,k)\} \subseteq \overline{K}_b.$$

Proof. We articulate the proof into two cases based on whether the input i is explicitly found as a DIP by SAT(b) (case 1) or not (case 2).

Case 1. By the definition in Section II-B, $\{k|f_b(i) \neq f'_b(i,k)\}$ is the set of keys that are pruned out by the DIP *i*. Therefore, we have $\{k|f_b(i) \neq f'_b(i,k)\} \subseteq \overline{K}_b$.

Case 2. We denote by k^* one of the correct keys. Suppose, by contradiction, that there exists a wrong key k' that does not belong to \overline{K}_b while satisfying $f_b(i) \neq f'_b(i,k')$. From the circuit visualization of the SAT instance in Fig. 1, if K1, K2, and I are assigned with k^* , k', and i, respectively, then the SAT instance is satisfied. By definition, this means that i is a DIP that would be found by SAT(b), which contradicts our initial assumption. Therefore, there is no such wrong key k' that does not belong to \overline{K}_b , i.e., $\{k|f_b(i) \neq f'_b(i,k)\} \subseteq \overline{K}_b$ holds.

Lemma 2 shows that a key k' is in \overline{K}_b if $f_b(i) \neq f'_b(i,k')$ holds, even if *i* is not explicitly found as a DIP by SAT(b). The following theorems characterize the relation between FC_b and \overline{K}_b , stating that \overline{K}_b monotonically increases with FC_b and remains the same if FC_b remains constant.

Theorem 3. For all b > 1, let $FC_b = FC_{b-1}$ hold. Let \overline{K}_{b-1} and \overline{K}_b be the sets of wrong keys pruned out by SAT(b-1) and SAT(b), respectively. Then, $\overline{K}_{b-1} = \overline{K}_b$ holds.

Proof. We first prove that $\overline{K}_{b-1} \supseteq \overline{K}_b$ holds. Let i_b^{dip} be a DIP found by SAT(b). The set of wrong keys that can be pruned out by this DIP is

$$\overline{K} = \{k | f'_b(i^{dip}_b, k) \neq f_b(i^{dip}_b)\}.$$

Since $FC_b = FC_{b-1}$, the tags of all errors introduced by f'_b are less than b according to Theorem 1. Therefore, by Definition 3, there exists an input $i_{b-1} \in \mathbb{B}^{(b-1)|I|}$ such that $i_{b-1} \prec i_b^{dip}$ and the following condition holds:

$$f'_{b-1}(i_{b-1},k) \neq f_{b-1}(i_{b-1}), \ \forall k \in \overline{K}.$$

By Lemma 2, SAT(b-1) can prune out the wrong keys in \overline{K} . Therefore, SAT(b-1) can prune out all the wrong keys pruned by SAT(b), hence $\overline{K}_{b-1} \supseteq \overline{K}_b$ holds.

We now prove that $\overline{K}_{b-1} \subseteq \overline{K}_b$ holds. Suppose i_{b-1}^{dip} is a DIP found by SAT(b-1). The set of wrong keys that can be pruned out by this DIP is

$$\overline{K} = \{k | f'_{b-1}(i^{dip}_{b-1}, k) \neq f_{b-1}(i^{dip}_{b-1})\}.$$

For any input i_b , such that $i_{b-1}^{dip} \prec i_b$, we have

$$f'_b(i_b,k) \neq f_b(i_b), \ \forall k \in \overline{K}.$$

By Lemma 2, SAT(b) can prune out the wrong keys in \overline{K} . Therefore, SAT(b) can prune out all the wrong keys pruned by SAT(b-1), i.e., $\overline{K}_{b-1} \subseteq \overline{K}_b$ also holds. \Box

Theorem 4. For all b > 1, let $FC_b > FC_{b-1}$ hold, and let \overline{K}_{b-1} and \overline{K}_b be the sets of wrong keys pruned out by SAT(b-1) and SAT(b), respectively. Then, $\overline{K}_{b-1} \subseteq \overline{K}_b$ holds.

Proof. Since $FC_b > FC_{b-1}$ holds, f'_b will also introduce

new errors, with tags equal to b. For an arbitrary wrong key $k \in \overline{K}_b$, we consider the following two cases based on whether the following condition holds (case 1) or does not hold (case 2):

$$\exists i \in \mathbb{B}^{b|I|} : (f'_b(i,k) \neq f_b(i)) \land (\mathcal{T}_b(i,k) < b), \quad (1)$$

i.e., whether there exists at least one error introduced by f'_b whose tag is less than b.

Case 1. By Theorem 3, there exists an input $i_{b-1} \in \mathbb{B}^{(b-1)|I|}$ such that $f'_{b-1}(i_{b-1}, k) \neq f_{b-1}(i_{b-1})$ holds. Therefore, by Lemma 2, the wrong key k is also in \overline{K}_{b-1} .

Case 2. Since $k \in \overline{K}_b$, the associated errors must all have tag b, i.e.,

$$\mathcal{T}_b(i,k) = b, \forall i : f'_b(i,k) \neq f_b(i)$$

By Definition 3, we also conclude:

$$f'_{b-1}(i_{b-1},k) = f_{b-1}(i_{b-1}), \ \forall \ i_{b-1} \in \mathbb{B}^{(b-1)|I|},$$

i.e., k is not in \overline{K}_{b-1} .

Based on whether all the wrong keys in \overline{K}_b satisfy (1) or not, we conclude that \overline{K}_b can be at least equal to and possibly a superset of \overline{K}_{b-1} . Therefore, $\overline{K}_{b-1} \subseteq \overline{K}_b$ holds.

Theorem 3 and Theorem 4 directly relate the behavior of \overline{K}_b , hence the progress made by the attack, to the behavior of FC_b , which can be efficiently approximated via logic simulation. Therefore, by efficiently estimating the sequence FC_b , we can look ahead and make informed predictions about whether a SAT-attack instance or a model checking instance need to be solved or can be skipped to rapidly progress with the attack.

Specifically, if we find that $FC_b = FC_{b-1}$ holds, then we infer that it is sufficient to execute SAT(b-1), which is a smaller and usually faster instance than SAT(b). In fact, we know from Theorem 3 that SAT(b) cannot exclude any more wrong keys other than those already pruned out by SAT(b-1). On the other hand, when $FC_b > FC_{b-1}$ holds, we infer that SAT(b) is at least as effective as SAT(b-1), or even more effective, in narrowing down the search for the correct key. We can then move forward and directly execute SAT(b) by skipping the execution of SAT(b-1) and the additional model checking problem needed to verify termination on C_e^{b-1} . We incorporate both of these insights into Fun-SAT, as detailed below.

IV. FUNCTIONAL CORRUPTIBILITY-GUIDED SAT-BASED ATTACK

We detail the attack flow of Fun-SAT and discuss its termination conditions.

Algorithm 2 Fun-SAT

Input: Encrypted netlist C_e , oracle C_o , key sequence length t_k , FC analysis window t_{win} , FC difference threshold δ , FC hold threshold Δ , simulation sample size S

Output: Correct key sequence k^*

1: $b_l = 1; \ b_u = t_{win}$

- 2: while True do
- 3: // ****** FC analysis phase *****
- 4: counter = 0
- 5: **for** $b = b_l$ to b_u **do**
- 6: $FC_b = simulate(C_e, C_o, t_k, b, S)$

7: **if** b > 1 **then**

9: 10:

11:

12:

13:

14:

15:

16:

17:

18:

19:

20:

8: **if** $FC_b - FC_{b-1} \leq \delta$ then

```
counter = counter + 1
```

```
else
```

```
counter = 0
```

end if

end if

 $b^* = b$ if $counter == \Delta$ then

```
b^* = b^* - \Delta
```

```
break
end if
```

```
end for
```

```
// ****** SAT attack phase ******
```

```
21: k^*, L_{dip}, L_{odip} = sat\_attack(C_e, C_o, t_k, b^*)
```

```
22: if !key\_verify(k^*, L_{dip}, L_{odip}) then
```

```
23: b_l = b^* + 1; \ b_u = b^* + 1 + t_{win}
```

24:	else
25:	break
26:	end if

27: end while28: return k^*

A. Attack Flow

As shown in Algorithm 2, Fun-SAT accepts as inputs a set of circuit-related and attack configuration parameters. Circuit-related inputs consist of the encrypted netlist C_e , the oracle C_o , and the key sequence length t_k . Configuration parameters include the FC analysis window t_{win} , the FC difference threshold δ , the FC hold threshold Δ , and the simulation sample size S, further described below.

The attack consists of an FC analysis phase (line 3 to line 19) and a SAT attack phase (line 20 to line 26). The first phase analyzes a sequence of FC values for different unrolling depths b and predicts the number of unrollings to be used in the second phase. To start the

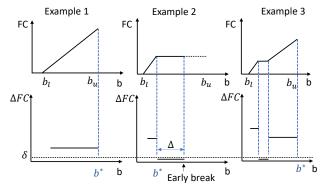


Fig. 4. Sample behaviors of FC as a function of $b (\Delta FC_b = FC_b - FC_{b-1})$.

first phase, we specify the initial range of b, i.e., the number of unrollings excluding the key length t_k , to be $[1, t_{win}]$ in line 1. FC_b is obtained via a logic simulation function in line 6, which simulates both C_e and C_o with random inputs and keys for S times and calculates an estimate of FC_b based on Definition 2.

As discussed in Section III-B, if $FC_b > FC_{b-1}$ holds for some b, then we pick b as the number of unrollings for the second phase (based on Theorem 4). Otherwise, if $FC_b = FC_{b-1}$ holds, we use b-1 (based on Theorem 3). The FC analysis step (line 7 to line 18) implements this decision rule as follows. If FC keeps increasing over the analysis window, we select the upper bound of the window b_u , as shown in Example 1 in Fig. 4. Otherwise, we relax the equality condition to accommodate approximation errors and check whether $(FC_b - FC_{b-1}) \leq \delta$ holds, where δ is a small positive number (e.g., 0.01). If this condition holds for very few occurrences before FCincreases again, as in Example 3 in Fig. 4, we count these occurrences and terminate the first phase with an early break only when the number of successive occurrences exceeds a pre-determined threshold Δ . This early break prevents unnecessary FC simulations when FC stops increasing at an early stage, as in Example 2 in Fig. 4.

In the second phase, the SAT attack is executed (line 21) with the number of unrollings b^* decided in the first phase. However, the resulting candidate key k^* can only guarantee the correct behavior of the sequential circuit up to b^* clock cycles after reset. Therefore, an additional key verification step is needed to check whether k^* is indeed the correct key (line 22). The candidate key k^* , the list of found DIPs L_{dip} and the list of the corresponding correct output values L_{odip} are used in this step, described in Section IV-B. When the key verification fails, we revisit the first phase and search for a new unrolling depth value with a new FC analysis window (line 23). This loop terminates when a correct key is found.

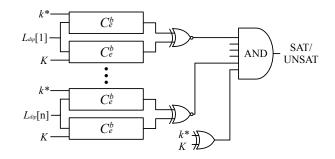


Fig. 5. Circuit visualization of the SAT instance to check the unique key (UK) condition.

B. Termination Conditions

The last step before the successful termination of the attack in Algorithm 2 is the key verification function (line 22). In this step, because the netlist of the oracle is assumed unavailable in the attack model, we cannot directly check the equivalence of the oracle C_o and the encrypted netlist C_e configured with k^* . We therefore build on the literature on SAT-based attacks [18] to formulate two key verification conditions, namely, unique key (UK) and model checking equivalence (MCE), and conclude on the correctness of a candidate key for a circuit encrypted via sequential logic encryption.

Unique Key. If k^* is the only remaining key that makes the encrypted circuit C_e behave the same as the oracle C_o for all DIPs in L_{dip} , then k^* is the correct key. We check this condition by verifying that the set

$$\{k'|f'_b(i,k') = f'_b(i,k^*), \forall i \in L_{dip}\} \setminus \{k^*\}$$

is empty. To do so, we construct a SAT instance as shown in Fig. 5, where C_e^b is the *b*-unrolled version of C_e and $L_{dip}[n]$ is the *n*-th DIP in L_{dip} . When this SAT instance is UNSAT, the UK condition is satisfied and the attack terminates successfully with the correct key k^* .

Model Checking Equivalence. The SAT attack in Algorithm 2 often returns a set of candidate keys that match the behavior of the oracle over the first b clock cycles, but may eventually lead to different outputs over longer horizons. We detect these spurious keys by leveraging model checking to search whether there exist two keys in the candidate set that lead to different outputs on the encrypted circuit C_e .

Fig. 6 shows the circuit visualization of an example model used for this task, where $t_k = b = |L_{dip}| =$ $|L_{odip}| = 2$. For better illustration purpose, we represent the unrolled circuit C_e^2 as a cascade of $t_k + b$, i.e., four copies of the combinational logic of C_e . The IO ports in red, blue, or grey, are treated by the model checker as free binary variables, constant values, or 'don't care' bits,

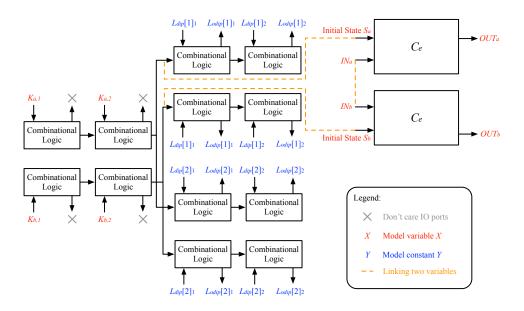


Fig. 6. The visualization of the model construction for checking whether the remaining keys are all correct.

respectively. K_a and K_b are the two keys. $K_{a,1}$ and $K_{a,2}$ represent the portion of K_a in the first and the second clock cycle, respectively. Similar subscript indices are used for K_b , the DIPs in L_{dip} , and the corresponding correct outputs in L_{odip} . The circuits on the left side of Fig. 6, whose inputs and outputs are assigned all the DIPs and the corresponding correct outputs, are used to model the constraints that limit the search space for K_a and K_b only to the candidate set. On the right side of Fig. 6, two copies of the encrypted circuit C_e are instantiated and forced to receive the same inputs at IN_a and IN_b , as denoted by the orange dashed lines linking the two ports. Importantly, the initial states S_a and S_b of the two copies of C_e are also set to the corresponding initial states obtained after applying K_a or K_b to the leftside circuit, respectively. These constraints ensure that the two copies of C_e on the right side are configured as if they were provided with K_a or K_b . Such a construction was not used in previous work [17], [18], since K_a and K_b could be directly provided to C_e via additional key ports.

The model above is given to a model checker to verify whether $OUT_a = OUT_b$ holds for an unbounded horizon. If the model checker returns false, it means there exists at least one key in the candidate set that eventually leads to the wrong circuit behavior on C_e . Therefore, the attack may not terminate. In our implementation, we first perform bounded model checking (BMC) with bound b + 1 as a preliminary check. If BMC returns false, we can already conclude that the SAT-based attack should continue. Otherwise, we need to perform unbounded model checking to verify the correctness of the candidate key set beyond b+1 cycles. The outcome of unbounded model checking will determine whether to conclude or continue the attack.

V. EXPERIMENTAL RESULTS

Experiment Setup. Fun-SAT was implemented in Python and executed on a Linux server with 48 2.1-GHz cores and 500-GB memory. In the FC analysis phase, we use Synopsys VCS to run the logic simulation on both the oracle and the encrypted netlist. The logic simulation time is deemed as a reasonable, if not conservative, approximation of the functional query time, since hardware execution is generally faster than software simulation. The SAT attack is adapted from the literature [15] and leverages MINISAT [23] as the SAT solver while model checking is performed using the interpolationbased algorithm [24] implemented by the NUXMV [25] model checker. The model is constructed as described in Section IV and encoded into the NUXMV format by a Python script. For the reference attack in Algorithm 1, we first evaluate increasing the unrolling depth b by one whenever the key verification fails. We then explore a multiplicative update rule, e.g., $b = 2 \cdot b$, which can speed up both the reference and Fun-SAT attacks. We select ten benchmarks from ISCAS'89 [26] and ITC'99 [27], as detailed in Table I, in line with the sizes of the benchmarks used in the related literature [17], [18], [21].

We implement the two sequential logic encryption methods, as described in the reference papers [13], [14]. Besides the key size t_k , there are other configuration parameters that are specific to the methods. In HAR-POON, the Modification Kernel Function (MKF) module

 TABLE I

 Overview of the Selected Benchmark Circuits

Circuit	s27	s526	s1488	s9234	s15850	s38584	b10	b12	b15	b19
Inputs	4	3	8	19	14	12	11	5	36	24
Outputs	1	6	19	22	87	278	6	6	70	30
DFFs	3	21	6	228	597	1452	17	121	449	6642
Gates	10	193	653	5597	9772	19253	214	1217	8169	190213

is inserted to corrupt the circuit function when the applied key is wrong. In our experiments, we randomly select the locations of the MKFs and use the ratio R_{mkf} between the number of MKFs and the number of gates in the original circuit as a parameter to configure the encryption. In Interlocking, a set of wrong keys can also bring the circuit to the functional mode without triggering output errors immediately. These keys trigger output errors only when the circuit enters certain predetermined states in the functional mode. Based on the distance between one such state s_{pre} and the true reset state in the functional mode, the occurrence of output errors may be delayed for a few cycles. In our experiments, we introduce the parameter D_{max} to set the maximum number of state transitions between the true reset state in the functional mode and a state s_{pre} in which output errors are triggered. A wrong key k_w is randomly assigned to s_{pre} such that an output error occurs in s_{pre} when k_w is applied.

We determine the simulation sample size S in Algorithm 2 using numerical experiments such as the one reported in Fig. 7(a), where the FC of the largest benchmark s38584, encrypted with a randomly selected Interlocking configuration, is simulated with different sample sizes. We choose S = 1000 in the rest of this section, since it leads to a reasonable approximation error for the FC. The FC difference threshold δ and hold threshold Δ are instead set to 0.01 and 5, respectively, which provide sufficient accuracy to detect when the FC remains constant. Higher values of S and Δ and lower values of δ can improve the prediction accuracy of the minimum unrolling depth at the cost of increased simulation time.

Case Study. We illustrate Fun-SAT on s38584, encrypted using Interlocking with $t_k = 4$, corresponding to a key bit-length of 48, and $D_{max} = 5$. Fig. 7(b) shows the behavior of FC for the encrypted circuit as a function of the unrolling depth b. In the FC analysis phase, the FC is calculated by logic simulation starting from b = 1. When b is increased to 5, the FC value starts to stabilize, i.e., the difference between two consecutive FC values is within δ . After a number of additional FC simulations equal to Δ , the first phase terminates by suggesting an unrolling depth of 5. In the SAT-attack phase, Fun-SAT

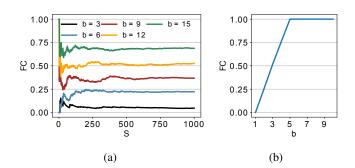


Fig. 7. (a) FC vs. simulation sample size S and (b) Behavior of FC as a function of the unrolling depth b for an encrypted version of s38584.

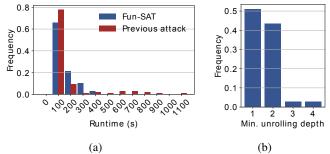


Fig. 8. Histograms of (a) the attack runtime and (b) the required unrolling depth for the HARPOON-encrypted circuits.

unrolls the encrypted circuit for 5 cycles and execute the SAT attack on the unrolled circuit. The attack terminates successfully with a single key within 507 s. In contrast, the reference attack in Algorithm 1 starts by unrolling the circuit once (b = 1) and performs 10 more checks of the termination conditions (five UK and five MCE checks), which takes 2.64 h and is $18.7 \times$ slower than Fun-SAT.

Numerical Experiments on the Benchmark Circuits. We encrypt the first nine selected benchmarks with HARPOON using different configuration parameters. The key size t_k ranges from 1 to 4 while the MKF ratio R_{mkf} is assigned four different values, namely, 5%, 10%, 15%, and 20%. We then apply both Fun-SAT and the reference attack in Algorithm 1 on all the 144 encrypted circuits. Fig. 8(a) shows the distribution of the attack runtime.

All the attacks successfully terminate within 20 minutes, with the average attack time for Fun-SAT and the reference attack being 83 s and 97 s, respectively. Such a small average attack runtime for both attacks is mostly due to the small number of unrolling cycles required by HARPOON-encrypted circuits, as shown in Fig. 8(b), which are designed to achieve high functional corruptibility. The benchmarks encrypted with Interlocking exhibit, instead, larger unrolling depth and, therefore, higher resilience to the reference SAT-based attack. We

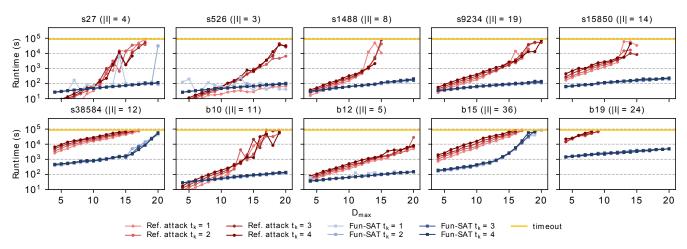


Fig. 9. Numerical results for Fun-SAT on Interlocking. (The key bit-length can be computed as $t_k[I]$.)

execute the two attacks on circuits encrypted with Interlocking with a time-out threshold of one day. The range of the key size is the same as for the HARPOON configurations while D_{max} ranges from 4 to 20. Fig. 9 shows the attack runtime for all the ten benchmark circuits together with the highlighted time-out threshold. The runtime of the reference attack drastically increases with D_{max} for all the benchmarks. Among all the encrypted netlists attacked by the reference attack, 19% reach the timeout after one day and the rest have an average runtime of 7 hours. In contrast, only 0.7% of the Fun-SAT attempts reach the time-out and 91% terminate successfully within 60 minutes. On average, Fun-SAT achieves 90× faster execution than the reference attack whenever both the attacks do not reach time-out. Executing Fun-SAT and the reference attack with the $2 \cdot b$ update rule on three representative benchmarks, s1488, s15850, and s38584, encrypted with the same Interlocking configuration, still shows $62\times$, $76\times$, and $10\times$ faster execution than the reference attack, respectively.

Extensions of Fun-SAT. We have demonstrated the effectiveness of Fun-SAT in finding the correct key when the key length t_k is known. In the case of an unknown t_k , we may still perform the attack by regarding the correct initial state of the circuit, encoded by the connections between the t_k -th and the $(t_k + 1)$ -th circuit replica in Fig. 2(b), as providing the *effective key* inputs in the unrolled circuit, with no substantial modifications to the circuit representation. This new key effectively configures the correct initial state of the circuit. To access the correct functionality, an attacker can then modify the reset values of all the registers in C_e according to the found key.

Recently, sequential encryption techniques [19], [22] have also been proposed that add extra key ports to

the encrypted circuit, forcing the users to provide the correct key even if the circuit is in the functional mode. Extending Fun-SAT to address these schemes by accordingly modeling the two types of keys is a possible direction for future research. Finally, while the focus of Fun-SAT is on boosting attack efficiency by replacing many, possibly expensive, SAT calls with less expensive logic simulations, the attack may be further improved by using more advanced SAT-attack tactics, such as the incremental SAT-solving in KC2 [17].

VI. CONCLUSIONS

We presented a functional corruptibility-guided SATbased attack method that can efficiently estimate the minimum unrolling depth required for a successful SAT attack to prune out of the search space all the wrong keys. Fun-SAT achieves on average two orders of magnitude runtime improvement when compared with a previous reference attack and can effectively be used as a method for evaluating the security of existing sequential encryption schemes. Moreover, Fun-SAT relies on a notion of functional corruptibility for sequential circuits and monotonicity properties that are independent of the specific encryption scheme. They can then be applied to accelerate other attack variants [17], [18] or circumvent newly developed encryption schemes [28] that aim to increase the required unrolling depth to achieve resilience against SAT-based attacks.

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