Efficient and Accurate Transient Simulation in Charge-Voltage Plane

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Abstract

Transient simulation has traditionally been performed in current-voltage plane (with current and voltage as variables) for verification of integrated circuits and systems. This paper introduces techniques for efficient and accurate transient simulation in charge-voltage plane (with charge and voltage as variables). For integrated circuits, both simulation cost and overhead to increase accuracy are drastically reduced by performing simulations in charge-voltage plane. Adaptively controlled explicit simulation in charge-voltage plane is used to demonstrate the feasibility of the approach. Solution of circuit equations in charge-voltage plane is 10-20 times more efficient than in current-voltage plane. Furthermore, simulation accuracy can be increased at an incremental cost. As a result, ACES in charge-voltage plane provides speedups of 300x-5000x or more over traditional circuit simulators with little or no loss in circuit timing accuracy.

1. Introduction

Traditionally, transient simulation has been performed in current-voltage plane (i.e. by considering current and voltages as variables of interest). Circuit equations are formulated in terms of currents and voltages leading to nonlinear ordinary differential equations. Once the circuit equations are formulated, transient simulation is performed by repeated evaluations of the circuit (or part of the circuit for multirate/event driven simulations). Solution of these nonlinear differential equations, along with model evaluation, constitutes the bulk of the simulation cost. Simulation accuracy is generally controlled by solution accuracy (local truncation error, etc.) and model accuracy (complexity of the device models). Both efficiency and accuracy are critically important in verification of complex integrated circuits. Lower feature sizes, advanced and sophisticated circuit design techniques and growing "analog" nature of integrated circuit behavior demand high levels of accuracy from a transient simulator. On the other hand, ever increasing circuit size and complexity (need to simulate circuits for larger and longer input vectors) contribute to increased efficiency and capacity requirements. Speedup factors of 100x-1000x compared to conventional simulators coupled with acceptable accuracy are required to be able to design today's and future's large integrated circuits in acceptable time.

This paper presents techniques for improving efficiency and accuracy by performing transient simulation in charge-voltage plane. Prevalent modeling techniques [3,4,5,6,7,etc.] model the transistor as nonlinear dissipative element (i.e. i-v relations are nonlinear, piecewise linear, piecewise constant, etc.) and linear energy storage elements (i.e capacitors are linear). Transformation of such a circuit into charge-voltage plane yields a circuit with nonlinear energy-storage elements and linear dissipative elements. Solutions of these circuits in charge-voltage plane using source-based integration methods yields significant advantage in computational efficiency. Example of source-based integration methods are Forward Euler integration, Adaptively controlled explicit integration [7], Asymptotic Waveform Evaluation [8](AWE-based piecewise linear methods [6,9]), etc. Charge-voltage plane simulations using adaptively controlled explicit integration is used to demonstrate advantages of such an approach.

2. Circuit Transformation

Nonlinear coupled-ordinary differential circuit equations are obtained by applying Kirchoff current law, Kirchoff voltage law and by the branch constitutive relations. The circuit's differential equations can be formulated in any independent set of basis variables (i.e. different from i-v) provided the new basis variable set is sufficient to describes the circuit's operation. The basis variable (charge) in the transformed circuit is an integral of the basis variable (current) in the original circuit.

$$q(t) = \int_{t_o}^{t} i(\tau)\, d\tau \tag{1}$$

The connectivity relations (i.e. KVL and KCL) remain the same in the charge-voltage plane. KCL, in the charge voltage plane, is written in its integral form indicating the conservation of charge at every node and cutset of the transformed circuit. Most branch constitutive relations (BCRs) are changed in the transformed circuit. For example, a conductance in the original circuit is transformed as follows,

$$i = Gv \Rightarrow \frac{dq}{dt} = Gv \Rightarrow \frac{1}{G}\dot{q} = v \tag{2}$$

Hence, a conductance in the original circuit is transformed to a inductance in the transformed circuit. Transformation of some representative circuit elements are shown in Figure 1. Consider a linear (or linearized) circuit with nodal equations in the original (current-voltage) plane as

$$C\dot{v}(t) + Gv(t) = i(t) \tag{3}$$

In the above equations, C matrix represents the energy storage portion of the circuit and G matrix represents the dissipative portion of the circuit. In the transformed circuit in charge-voltage plane, the G matrix represents the energy storage portion of the circuit and C matrix represents the dissipative portion of the circuit.

Motivation for Circuit Transformation

Transient simulation of a nonlinear circuit is performed by successive solutions of the circuit (or part of the circuit in case of event driven or multirate simulations) at various timepoints of interest. The solution of simultaneous equations $Mx = b$ is performed at the inner loop of the simulation process. At each "evaluation" of the cir-

Current-Voltage (I-V) Plane	Charge-Voltage (Q-V) Plane
$i = C\frac{dv}{dt}$ Capacitor	$q = Cv$ Resistance
$i = Gv$ Resistance	$v = \frac{1}{G}\frac{dq}{dt}$ Inductance
$v = V_c$ Voltage Source	$v = V_c$ Voltage Source
$i = I_c$ Current Source	$q = Q_c = \int I_c$ Charge Source
$i_2 = G_m v_1$ Trans-conductance	$\frac{dq_2}{dt} = G_m v_1$ Trans-inductance

Figure 1 *Transformation of circuit elements from Current-Voltage (I-V) to Charge-Voltage (Q-V) plane.*

cuit, the circuit equations $Mx = b$ change requiring a new solution of the simultaneous equations. A change in M requires a new LU-factorization of the matrix, where as a change in b requires a new forward and backward solve (FBS). The execution of the LU-factorization of the n linearized simultaneous equations is said empirically to be proportional to $n^{1.4}$ for integrated circuits, where n is the dimensionality of M matrix. Whereas, the forward and backward solve is empirically proportional to n for integrated circuit matrices.

Traditionally, in current-voltage plane, both M matrix and b vector change at each circuit "evaluation" requiring a new LU-factorization and a new FBS. Circuit equations are bound to change during a transient simulation of a nonlinear (or piecewise linear) circuit. However, it is computationally very attractive to concentrate most (or all) of the change in circuit equations in vector b. Hence, each solution of circuit equations will mostly (only) require a FBS (order n) compared to a matrix LU-factorization and FBS. Consider a simulation of the circuit which requires k solutions of simultaneous equations $Mx = b$. In the current voltage plane, the cost of solution portion of the simulation will be proportional to $kn^{1.4} + kn$. Whereas, if all the changes are concentrated on vector b the solution portion of the simulation will be proportional to $n^{1.4} + kn$. Transformation of circuit equations into charge-voltage plane can provide us with such a transformation such that the change in reflected in vector b most (or all) of the time.

Integrated circuits obtained by highly prevalent modeling techniques [3,4,5,6,7,etc.] have nonlinear dissipative characteristics and linear energy storage characteristics in the current-voltage plane. Circuit equations, so obtained, can be solved using a variety of integration methods and techniques. Transforming the original circuit to charge-voltage plane (Figure 2) is particularly attractive for techniques that use source-based solution methods. Source based solution methods is used to denote techniques that replace the energy storage elements by either independent voltage sources or independent current sources or both. Examples of such source based methods are Forward Euler integration, Adaptively Controlled Explicit Simulation (ACES)[7], Asymptotic Waveform Evaluation [8](AWE-based methods [6,9]), etc.

During a transient simulation, the circuit equations change at each "evaluation" due to both the nonlinearity and the integration of the differential equations. If an energy storage element is replaced by a time-varying independent source, these varying independent sources will account for both the numerical solution and nonlinearity of the circuit in charge-voltage plane. This can be seen in Figure 3. The changing independent source concentrates the circuit equation changes to the right hand side of the circuit equations. The dissipative part (or the matrix portion) of the circuit does not change from one timestep to another and hence circuit "evaluation" only requires a forward and backward solves (FBS).

If the original circuit in $i - v$ plane consists of mostly nonlinear dissipative elements and linear inductors, it might be advantageous to transform the circuit to current-flux ($i - \Phi$) plane. For most integrated circuits, transformation to $q - v$ plane is most beneficial. Furthermore, different portions of the circuit in $i - v$, $q - v$ or $i - \Phi$ planes can be combined in a single transient simulation. For example, a portion of the integrated circuit consisting of inductors can either be simulated with an inductor as a double derivative element in $q - v$ plane or as an inductor in $i - v$ or as a conductance in $i - \Phi$ plane.

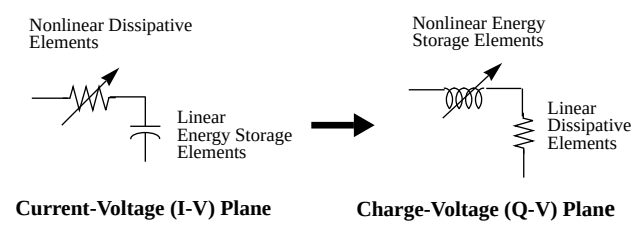

Figure 2 *Affect of charge-voltage plane transformation on dissipative and energy storage elements.*

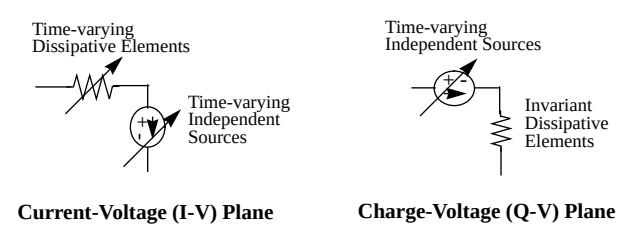

Figure 3 *Solution of integrated circuits in current-voltage (i-v) and charge-voltage (q-v) planes.*

3. Solution in Charge-Voltage Plane

The differential equations in charge-voltage plane are solved using adaptively controlled explicit simulation. Multi-dimensional continuous piecewise linear modeling techniques[11] are used to model the device characteristics.

3.1. Adaptively Controlled Explicit Simulation

Adaptively Controlled Explicit Simulation (ACES)[7] is a transient simulation methodology for integrated circuits and systems. ACES uses an adaptively controlled explicit numerical integration procedure which overcomes stability problems in earlier explicit techniques. The ACES integration approach naturally exploits the temporal latency in a circuit. Partitioning and event driven simulation[10] are used in ACES to exploit the spatial latency and multirate behavior of integrated circuits. For a state variable x, the ACES integration formula is written as follows,

$$x(t+\Delta t) = x(t) + \dot{x}^{+}(t)\Delta t \tag{4}$$

where $x(t+\Delta t)$ and $x(t)$ are values of state variable at time $t+\Delta t$ and t respectively, Δt is the timestep for integration, $\dot{x}^{+}(t)$ is the update derivative for the integration. $\dot{x}(t)$ is the time derivative of the state variable. ACES categorizes a state variable as either quiescent or nonquiescent. Quiescence is defined as the condition when a particular state variable has a zero time derivative, $\dot{x}(t)$. If a state variable is quiescent, $\dot{x}^{+}(t)$ may not be equal to $\dot{x}(t)$. ACES computes the response of the circuit as a transition from a condition when all state variables are nonquiescent to a condition when all state variables are quiescent. When all state variables are quiescent (i.e. have zero time derivatives) it is equivalent to steady state of the circuit. However, at intermediate timepoints during the transition from the initial condition (all state variables nonquiescent) to steady state (all state variables quiescent) some state variables are quiescent whereas others are nonquiescent. At any timepoint in the solution computation, ACES computes the timesteps that will take a nonquiescent state variable to quiescence (Δt_{qs}) and maintains in quiescence the state variables which are already quiescent. Hence, the response of the circuit gradually approaches steady state as more and more state variables become quiescent.

3.2. Circuit Equations in Charge-Voltage Plane

Let all inputs to the circuit to be comprised of combinations of steps and ramps. Device modeling techniques yield piecewise linear dissipative elements and linear energy storage elements (in current-voltage plane). Circuit equations at any time t can be written as,

$$Gv(t) + C\dot{v}(t) = I(t) \tag{5}$$

where v is a vector of node voltages, G is the conductance matrix, C is the capacitance matrix, and I is the current source contributions. Or, in the charge-voltage plane,

$$\int Gv(t) + Cv(t) = Q_i(t) \tag{6}$$

Alternatively,

$$q_n(t) = Q_i(t) - \int Gv(t) \tag{7}$$

where q_n is the vector of charge at the circuit nodes, $v(t)$ is a vector of circuit node voltages, $Q_i(t)$ is the contribution of independent charge-sources. Vector q_n is divided into two components: vector q_s, which is a vector of charge at circuit nodes with a path of independent voltage sources to ground from that node, and q_c, which is a vector of charge at capacitive circuit nodes. Independent set of charge variables (i.e. q_c) are taken as state variables for numerical integration. Let n_s be the number of state variables. Equation (7) can be written as,

$$q_n(t) = Q_i(t) - G\int_{t}^{t_{pwl}} v(t) \tag{8}$$

The change of integral represents the piecewise linear modeling of $i(t) = G(t)v(t)$. t_{pwl} is the time for which the piecewise linear elements remain linear with the present linearizations G. t_{pwl} is a function of $v(t)$, $\dot{v}(t)$ and piecewise linear device characteristics. t_{in} is defined as the time when the next independent input slope change occurs. Integration period, $T_{ip}(t)$, $T_{ip}(t) \geq t$, is defined as the minimum of t_{pwl} and t_{in}. Until the present integration period, T_{ip}, the circuit behaves as a linear circuit with same input slopes. Numerical integration is performed within each $T_{ip}(t)$. For a new integration period, the numerical integration procedure starts anew, with all state variables assuming nonquiescent status.

Let $q_q^{+} = [q_1, q_2, \ldots, q_q]$ be the set of quiescent state variables and $q_{nq} = [q_{q+1}, q_{q+2}, \ldots, q_{n_s}]$ be the set of nonquiescent state variables. Correspondingly, let $v_1 = [v_1, v_2, \ldots, v_q]$ be the vector of quiescent node voltages and $v_2 = [v_{q+1}, v_{q+2}, \ldots, v_{n_s}]$ be the vector of nonquiescent node voltages. Also, let v_s be the nodes with input voltage sources connected from the node. The circuit equations for the piecewise linear energy storage portion of the circuit in charge-voltage plane (dissipative in current-voltage plane, i.e. transistors, diodes, resistances, etc.) is written as follows,

$$\begin{bmatrix} g_{11} & g_{12} & g_{13} \\ g_{21} & g_{22} & g_{23} \\ g_{31} & g_{32} & g_{33} \end{bmatrix} \begin{bmatrix} v_q \\ v_{nq} \\ v_s \end{bmatrix} = \begin{bmatrix} \dot{q}_q \\ \dot{q}_{nq} \\ \dot{q}_s \end{bmatrix} \tag{9}$$

For a nonquiescent state variable the timestep to quiescence is computed using the equation:

$$\Delta t_{qs} = -\frac{\dot{x}_i^{+}(t)}{\ddot{x}_i^{+}(t)} \tag{10}$$

Using KCL (or conservation of charge in charge-voltage plane),

$$\ddot{q}_{nq} = \ddot{Q}_{s2} - \ddot{q}_{pwl} \tag{11}$$

where, $\ddot{q}_2$ is the double time derivative for nonquiescent state variables, $\ddot{Q}_s$ are independent charge source contributions and $\ddot{q}_{pwl}$ are contributions due to the piecewise linear elements (e.g., transistors in current-voltage plane). Since current sources are piecewise linear (ramps) in the current-voltage plane, and charge sources are time integral of the current sources, $\ddot{Q}_i$ exists and is nonzero for a nonzero slope ramp in current-voltage plane.

From Equation (9) and Equation (11):

$$\ddot{q}_{nq} = \ddot{Q}_{s2} - \left(g_{21}\dot{v}_q^{+} + g_{22}\dot{v}_{nq} + g_{23}\dot{v}_s \right) \tag{12}$$

For the quiescent state variables, state trajectories $\dot{q}_q^{+}$, are computed such that the state variable is maintained in quiescence. To ensure that, following constraint is imposed on the quiescent state variable,

$$\ddot{q}_q^{+} = 0 \tag{13}$$

Alternatively,

$$g_{11}\dot{v}_q^+ = \ddot{Q}_{s1} - g_{12}\dot{v}_{nq} - g_{13}\dot{v}_s \tag{14}$$

If the current through a voltage source is desired, the equations for the current are written as,

$$\dot{i}_{sv} = \ddot{Q}_{s3} - \left(g_{31}\dot{v}_q^+ + g_{32}\dot{v}_{nq} + g_{33}\dot{v}_s \right) \tag{15}$$

All the variables of interest at any timepoint (i.e., $\ddot{q}_{nq}$ for nonquiescent state variables, $\dot{q}_q^+$ or $\dot{v}_q^+$ for quiescent state variables and independent voltage source currents $\dot{i}_{sv}$) are included in a single matrix equation:

$$\begin{bmatrix} g_{11} & 0 & 0 \\ g_{21} & I & 0 \\ g_{31} & 0 & I \end{bmatrix} \begin{bmatrix} \dot{v}_q^+ \\ \ddot{q}_{nq} \\ \dot{i}_{sv} \end{bmatrix} = \begin{bmatrix} \ddot{Q}_{s1} - g_{12}\dot{v}_{nq} - g_{13}\dot{v}_s \\ \ddot{Q}_{s2} - g_{22}\dot{v}_{nq} - g_{23}\dot{v}_s \\ \ddot{Q}_{s3} - g_{32}\dot{v}_{nq} - g_{33}\dot{v}_s \end{bmatrix} \tag{16}$$

As mentioned earlier, all state become nonquiescent when a new integration period begins. A new integration period begins when any piecewise linear element has a change in it regions of operation or when any input source has a change in its slope. When all state variables are nonquiescent, circuit equations can be rewritten as,

$$\begin{bmatrix} I & 0 \\ 0 & I \end{bmatrix} \begin{bmatrix} \ddot{q}_{nq} \\ \dot{i}_{sv} \end{bmatrix} = \begin{bmatrix} \ddot{Q}_{s2} - g_{22}\dot{v}_{nq} - g_{23}\dot{v}_s \\ \ddot{Q}_{s3} - g_{32}\dot{v}_{nq} - g_{33}\dot{v}_s \end{bmatrix} \tag{17}$$

As seen from Equation (16) and Equation (17), majority (if not all) of the piecewise linear elements are on the right hand side of the circuit equations. ACES also uses partitioning and event-driven simulation for the exploitation of circuit latency. During any timepoint of interest, only “active” partitions are evaluated. The above mentioned procedure is applied to the solution of circuit equations for each active partition. Furthermore, if required, simulation can also be performed with some partitions in current-voltage plane and others in charge-voltage plane.

4. Results and Analysis

Transient simulation techniques in charge-voltage plane has been implemented in simulation program ACES(qv). This section presents ACES(qv) results for both simulation efficiency and accuracy.

4.1. Efficiency

Transient simulation cost consists of circuit solution, model evaluation, circuit parsing and partitioning and simulation overhead. Solution of circuit equations require repeated matrix solutions each of which involves, pivot candidate selection, lower-upper factorization and forward and backward substitution. Table 1: compares the circuit solution time in current-voltage (i-v) plane and charge-voltage (q-v) plane. Table 1: shows the ACES(iv) circuit solution time, ACES(qv) circuit solution time and ACES(qv) speedup over ACES(iv) for the various circuits. Circuits of various sizes/configurations are considered. The circuits considered are either MCNC CircuitSim90 benchmarks or are industrial designs. All run times are in seconds on an IBM RS/6000. As seen from Table 1, circuit solution time in charge-voltage plane almost disappears giving a speedup of 9x-26x over circuit solution in current-voltage plane.

Simulation accuracy can be improved by increasing the number of segments in the piecewise linear representations[11]. Increasing simulation accuracy in charge-voltage plane is much less expensive compared to increasing accuracy in current-voltage plane. Overhead for enhancing accuracy is the defined as the ratio of simulation cost for nine region simulation to the simulation cost for four region simulation. As seen from Figure 4, the overhead is lower in the Q-V plane compared to the I-V plane. The overhead is relatively small even in the current voltage plane (1.1-1.42), it is even smaller in charge-voltage plane (0.91-1.11). It should also be noted that not only is the overhead lower in charge-voltage plane, even the cost of a comparable four-region simulation is lower in charge-voltage plane compared to current-voltage plane.

Table 2 demonstrates ACES(qv) efficiency compared to SPICE3 and AS/X[2]. As seen from the table, ACES(qv) provides extremely efficient simulations with speedups of 300x-5000x over traditional circuit simulators. Furthermore, ACES(qv) simulation cost growths linearly with increase of circuit size (as shown in Figure 5). ACES(qv) has been used for simulation of circuits consisting of more than 1,000,000 transistors.

Circuit	MOSFETs	I-V	Q-V	**Speedup**
neural net	184	1.55s	0.1s	**15.5**
counter	220	1.6s	.07s	**22.8**
pchip	942	11.72s	1.05s	**11.16**
sram	1008	1.88s	.07s	**26.85**
add32	1984	11.94s	.82s	**14.56**
32cct	3328	5.05s	.51s	**9.9**
16alu	5696	23.8s	3.04s	**7.82**
ram2k	13880	54.16s	2.8s	**19.34**
256cct	26624	271.25s	21.82s	**12.43**

Table 1: *Speedup of circuit solution time for ACES in current-voltage (I-V) plane over charge-voltage (Q-V) plane.*

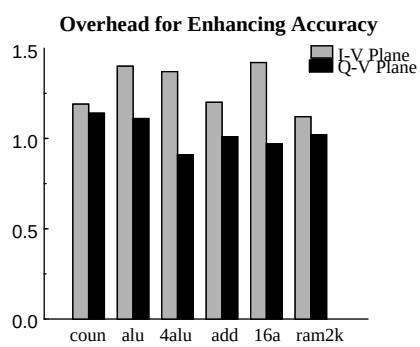

Figure 4 *Overhead for enhancing accuracy in current-voltage (I-V) and charge-voltage plane (Q-V) for various circuits. Overhead is defined as cost of nine region simulation divided by cost of four region simulation.*

Circuit	MOSFETs	ACES(qv) Speedup Over SPICE3
adder5	114	**371.2**
edc	208	**981.3**
add20	958	**3846.5**
Circuit	MOSFETs	ACES(qv) Speedup Over AS/X
counter	220	**853.6**
sram	1008	**1110.5**
4alu	1414	**3274.2**
64cct	6656	**5273.2**

Table 2: *Speedup of ACES (qv) over SPICE3 and AS/X for various circuits.*

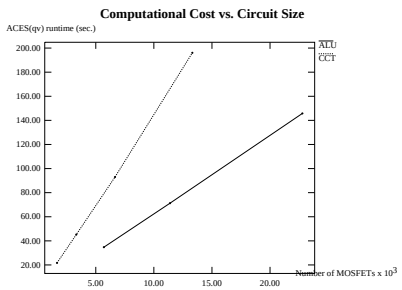

Figure 5 *Growth of ACES(qv) runtime (in seconds) for increase in circuit size for error detection/correct (1664 MOSFETs -13312 MOSFETs) and ALU (5696 MOSFETs- 22784 MOSFETs) circuits.*

4.2. Simulation Accuracy

This section illustrates the simulation accuracy of ACES(qv) through the simulation of a counter circuit (220 MOSFETs). As seen from Figure 6, ACES(qv) provides simulation waveforms which are almost indistinguishable from AS/X simulation waveforms. ACES(qv) accurate captures the glitches in the waveform, as seen in the close-up in Figure 7. ACES(qv) has been used for accurate simulation of variety of integrated circuits, including dynamic logic circuits, pass transistor logic circuits, mixed analog-digital circuits, interconnect circuits along with traditional CMOS circuits.

5. Conclusions

This paper has introduced efficient and accurate simulation techniques in charge-voltage plane. Prevalent modeling techniques model integrated circuits as nonlinear dissipative elements (transistors) and linear energy storage elements (capacitors). The original circuit is transformed to charge-voltage plane yielding integrated circuits which contain nonlinear energy storage elements and linear dissipative elements. Transient simulation of integrated circuits in charge-voltage plane by source-based integration methods yields tremendous advantage in both efficiency and accuracy. ACES in charge-voltage plane, ACES(qv), was used to demonstrate the advantage of such an approach. The solution of circuit equations in charge-voltage plane is 10-20 times more efficient that in current-voltage plane. Furthermore, cost of improving accuracy by adding more regions in the device models is insignificant in the charge-voltage plane. As a result of techniques presented in this paper, ACES(qv) simulates circuits of size over one million transistors and provides a speedup of 300x-5000x or more over conventional circuit simulators with little or no degradation in circuit timing accuracy.

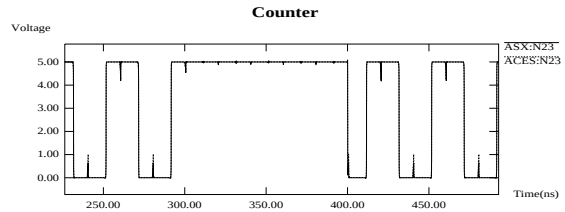

Figure 6 *Output waveforms for a counter circuit as obtained by ACES(qv) and AS/X.*

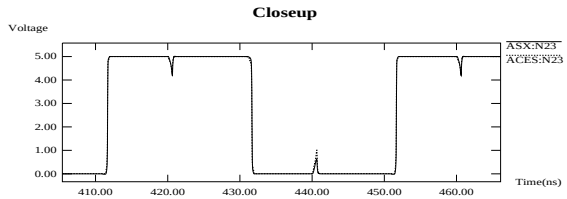

Figure 7 *Close-up of output waveforms as obtained by ACES(qv) and AS/X.*

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