A New Algorithm for the Design of Stable Higher Order Single Loop Sigma Delta Analog-to-Digital Converters

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Abstract

This paper presents a new algorithm to attain optimized network scaling in single loop, 1_bit Sigma Delta Analog to Digital Converters (SD ADC) of order three or more. The algorithm is based on a novel mathematical description of stability and performance criteria of the SD ADC and on the application of non linear interactive optimization techniques. The feasibility of the new algorithm has been confirmed in practical implementations. The method brings new insight on the correlation between system stability, performance, system order and the choice of the network scaling. Our method is extendible to cascaded SD as well as SD based on filter topologies.

Introduction

Single Loop, 1-bit SD ADCs of order greater than two have not been used up to now because of stability problems[1]. Slow or absence of recovery after an overload provoked through powerup, high input signal amplitudes or a short power distribution failure has made these higher order structures unreliable for practical applications. Nevertheless the need for higher resolution has lead to the development of new topologies based on loop filter design [2,3,4] and cascading of lower order SD ADCs[5]. Unfortunately, architectures based on filter topologies are considered as conditionally stable systems which have manifested recovery only after prolonged overload conditions[4] or have required additional reset circuitries in practice [3] to guarantee recovery after an overload. As for Cascaded SD ADC, stability is guaranteed at the cost of precise circuit matching, more performant analog components and larger die area as compared to an equivalent single loop SD. Therefore, if the stability problem in higher order single loop SD ADC is solved we can get more benefits out of a single loop structure than the alternative topologies. Unless precised, the term " single loop, 1-bit SD ADC " refers to the conventional architectures illustrated in figure 1 .

Optimized network scaling of a single loop, 1-bit SD ADC of order N (fig.1) consists in determining the adequate coefficients ((ai,bi)), which guarantee stability and high performance. Performance in a SD is related to its resolution given in bits. The idea that stability in higher order single loop SD ADC can be assured in practical implementations through an adequate network scaling is recent[6]. Yet no rigorous method applicable to all structures has been developed up to now. Although the correlation between performance and coefficient choice has often been treated, very few works have dealt with a complete analytical description of the correlation between performance, stability, converter order and the choice of the coefficients ((ai,bi)) most probably due to the complexity of the system. Hein [7] was one of the first to present a thorough description of these correlations by considering the nonlinear properties of the SD. Although his work was limited to the case of a second order SD, it has the great credit of bringing into light the need for a theoretical support in order to better understand the influence of these coefficients on the global mechanism of the modulator. It is most probably the insufficient knowledge of these influences which has made it difficult to implement stable singe loop SD of order three or more.

Interactive optimization techniques for the design of integrated circuits [8] enable performance optimization in the presence of constraints, through an adequate choice of circuit parameters. This principle is also applicable to systems and therefore to our specific problem.

This paper presents for the first time an algorithm for the determination of an optimum network scaling in single loop SD ADC of order three or more. The algorithm is based on a new mathematical description of the performance and various constraints in the SD and uses interactive optimization techniques for the determination of the optimal coefficients ((ai,bi)) of a given Nth order SD ADC.

The characterization of a stable and performant Nth order SD is presented in I. Part II describes the fundamental steps of the new algorithm. The new mathematical analysis of the stability and performance constraints and the application of interactive optimization techniques to the case of the SD is described in III. The feasibility of this method has been confirmed in behavioral and circuit level simulations of the SD,and proven through experimental results. This shall be treated in part IV.

I. Stability and performance characterisation

Figure 1 presents an ideal Nth order single loop, 1_ bit SD ADC. The latter is composed of N identical low pass analog filters represented by the ideal transfer function $H(z)=\frac{z^{-1}}{1-z^{-1}}$, the 1_bit quantizer and a 1-bit DAC. The coefficient set ((ai,bi)) represents the gain factors in the feedback and feed forward paths of the converter. X(t) is

the input signal, its allowed input range is designated by [-Xmax, Xmax]. The Nth order SD is a non-linear system because of the presence of the 1-bit quantizer. Unless specified the designation Nth order SD, SD or SD ADC shall refer to these structures.

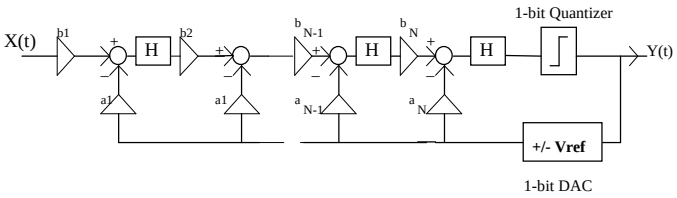


Fig.1 An Nth Order Single Loop, Single Bit SD ADC

A stable Nth order SD has to obey the following constraints :

- Linear range operation of the integrators under normal operating conditions : **Non Overload Criteria**
- The root locus of the equivalent linear system must remain inside the unit circle under normal operating conditions : **Stable Pole Criteria**
- In case of overload, the integrators must present a very fast recovery after return to normal operating conditions : **Fast Recovery Criteria**

The fast recovery behavior is an important stability characteristic and isrelated to the self control of the converter.

A performant Nth order SD must present :

- A minimization of the inband quantization noise and a wide dynamic range : **Performance Criteria**

By dynamic range we mean the positive input range [0, Xmax] for which the SD functions properly. We shall only consider the inband quantization noise reduction. Circuit noises such as switch noise, thermal and flicker noise are independent of the choice of the coefficients ((ai,bi)) which we wish to optimize and can be reduced through specific design techniques [9, 10] so that their level remains below the quantization noise level of a given SD.

II. The fundamental steps in the algorithm

Optimizing higher order SD ADCs consists in guaranteeing simultaneously the stability and performance criteria given above. Figure 3 illustrates the three fundamental steps in our design methodology.

The first step consists in defining appropriate system equations of a given Nth order SD. These equations are based on the equivalent mathematical models of the SD which are of two types : an equivalent linear model and a non-linear model.

The second step deduces from the equations above the performance and condition functions related to specified stability and performance criteria. At this stage the optimization problem is defined: with the help of these functions and inequalities, the correlation between the system stability, the system order, the system performance and the set of coefficients ((ai,bi)) of the corresponding Nth order SD is described.

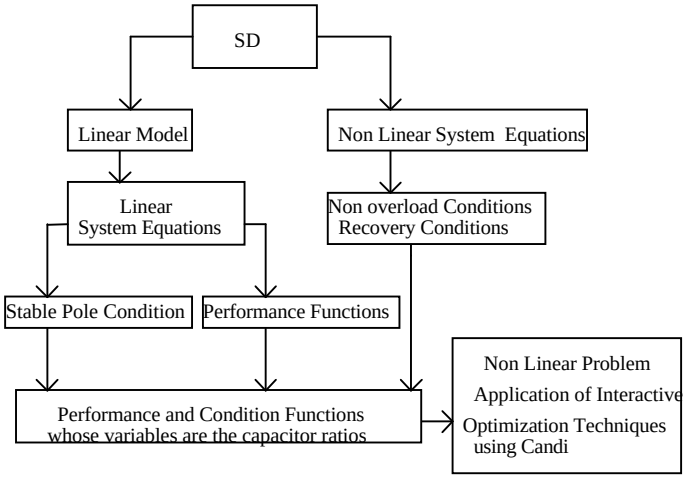


Figure 3. Algorithm of the Methodology

We shall see that stability constraints are mathematically expressed with inequalities which tend to down scale the coefficients ((ai,bi)), while performance considerations are mathematically expressed with functions whose maximization or minimization requires an upscaling of the coefficients.

A solution which best meets the conflicting requirements for stability and high performance is obtained through numerical optimization techniques[8]. Step three deals with the application of non-linear interactive optimization techniques to the case of the SD for the determination of the optimal coefficients.

III. Mathematical analysis of the stability and performance constraints

The System Equations: The behavior of the SD can be divided into two parts: a global and a local behavior. The global behavior of the SD gives a general view of the performance and pole stability in the SD. It considers the SD as a black box which links the inputs to an output via transfer functions. This behavior can be described by the equivalent linear model (figure 4) where the non-linear quantizer is modelled by a white noise source E(z) and the 1_bit DAC by a gain factor Vref.[11].

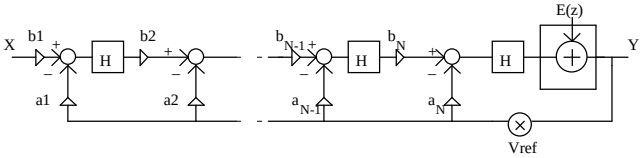


Fig. 4. Equivalent linear model of the SD

In this description the SD appears as a system with two inputs: the analog input X(z) and the quantization noise source E(z). The output Y(z) of the equivalent model is expressed in (1) and (2) where STF(Z) and NTF(z) are respectively the Signal and the Noise transfer functions

of the system. The characteristic equation of the equivalent system is defined by (2.1)

$$Y(z)=\underbrace{\frac{\prod_{i=1}^{N} b_i}{a_1\times D(z)}}_{STF(z)}\times X(z)+\underbrace{\frac{(z-1)^N}{D(z)}}_{NTF(z)}\times E(z) \quad (1)$$

with

$$D(z)=(z-1)^N+(a_N\times Vref)\times\left[(z-1)^{N-1}+\left(\sum_{j=0}^{N-2}(z-1)^j\times\prod_{i=j+2}^{N}\frac{b_i a_{i-1}}{a_i}\right)\right] \quad (2)$$

$$D(z)=0 \quad (2.1)$$

A global behavior analysis of the SD based on the equivalent linear model is insufficient for a complete understanding of the system. An observation of the local behavior of the SD gives more details about the interactions inside the system. For example recovery considerations, linear range operation of the integrators, the amplitude variations in each integrator or the existence of saturation in a specific integrator are informations which cannot be obtained from the global behavior model. It is therefore mandatory to perform local behavior analysis in order to have a better understanding of the SD.

The local behavior of the SD is described with the help of the state variable equations defined as the output states of the integrators for a given sampling time and are defined by the following non-linear series :

$$v_i(n)=v_i(n-1)+b_i v_{i-1}(n-1)-a_i Vref\times sgn(u(n-1)) \quad (3)$$

$$v_0(n)=x(n),\quad i\in[1,N]$$

$$u(n)=u(n-1)+b_N v_N(n-1)-a_N Vref\times sgn(u(n-1)) \quad (4)$$

where :

- $v_i(n)$ is the sampled value at time t= n*Ts (Ts= sampling period)of the state variable corresponding to the i_th integrator.
- u(n) is the sampled value at time t= n*Ts (Ts= sampling period) of the state variable corresponding to the Nth integrator.
- sgn(.) represents the mathematical operation of the 1-bit quantizer:

$$\begin{cases}\text{if } x\geq 0^+ & sgn(x)=+1\\ \text{if } x\leq 0^- & sgn(x)=-1\end{cases} \quad (5)$$

The integrators are limited to a certain clipping level which we shall represent by the letter L. The equations defined in (1) to (5) form the system equations.

Performance functions: We shall consider the performance of the SD from the resolution point of view. That is, high resolution is synonymous of good performance. High resolution is obtained when the inband quantization noise is minimized and the dynamic ranged is maximized. The performance functions are deduced from the noise contribution at the output of the converter and the Signal to Noise Ratio peak value defined as follows:

- Noise in baseband [0, fb]

$$N_o=\int_0^{fb}|NTF(f)\times E(f)|^2\,df \quad (6)$$

- The Signal to Noise Ratio Peak Value

$$SNR_{peak}=\frac{Max\left(|STF(f)\times X(f)|_{f\in[0,f_b]}\right)}{N_0}=\frac{b_1 X_{max}}{a_1 V_{ref}}\times\frac{1}{N_o} \quad (7)$$

In which NTF, STF are defined by the z-transformed expressions given in (1) and (2).

The calculation of (6) and (7) gives

$$N_o=\left(e_{RMS}\frac{\pi^N}{\sqrt{2N+1}}M^{-(N+1/2)}\right)\times\left(a_1 V_{ref}\prod_{i=2}^{N}b_i\right)^{-1} \quad (8)$$

$$SNR_{peak}=\left(X_{max}\frac{\sqrt{2N+1}}{e_{RMS}\pi^N}M^{N+\frac{1}{2}}\right)\times\left(\prod_{i=1}^{N}b_i\right) \quad (9)$$

Where :

- $M=\frac{f_s}{2*f_b}$ is the Oversampling ratio and N the order of the SD.
- $e_{RMS}=\frac{\Delta}{\sqrt{12}}$ is the mean square value of the quantization error (Δ= quantizer step size)
- Xmax represents the maximum input amplitude that the SD can support.

The frequency and order dependent terms in the first parentheses of relations (8) and (9) are well-known [5]. The terms in the second parentheses of (8) and (9) reveal new relations linking the inband quantization noise and the signal to noise ratio peak value to the order and the coefficients in the SD. This implies that performance is dependent on the choice of the network scaling ((ai,bi)). We see that the quantization noise is minimized and the signal to noise ratio peak value is maximized when the terms $a_1\left(\prod_{i=2}^{N}b_i\right)$ and $\left(\prod_{i=1}^{N}b_i\right)$ are maximized. This means that the coefficients in the feed forward path of an Nth SD order must be maximized as well as the coefficient in the first feedback path. Our performance functions are therefore defined as:

- $f_1(a_1,b_2,..b_{N-1},b_N)=a_1\left(\prod_{i=2}^{N}b_i\right)$ (10.1)
- $f_2(b_1,b_2,..b_{N-1},b_N)=\left(\prod_{i=1}^{N}b_i\right)$ (10.2)

In the past the coefficients were chosen such that these functions were equal to one so that the relations (8) and (9) were only dependent on M and N. Realized structures of order three or more which had this property were instable [10]. We see that maximization of (10.1) and (10.2) is bounded by stability constraints.

Stable pole condition : The poles of the equivalent linear system are thezeroes of the characteristic equation

defined in (2). In discrete time systems the conditions for pole stability can be obtained by applying the Jury stability test [12] to (2.1). Another possibility is the use of Routh-Hurwitz Criteria [12], which is applicable to the bilinear transformation of (2.1) .We have chosen this method. The reason for our choice was the possibility of applying the Lienard Chipart principle [13] to the equivalent Routh Hurwitz matrix of the polynome defined in (2).This has enabled us to reduce the number of inequalities which must be verified by the Routh Hurwitz criteria by 1/4, due to relations linking certain sub determinants of the Routh Hurwitz Matrix with each other.

The bilinear transformation is defined by :

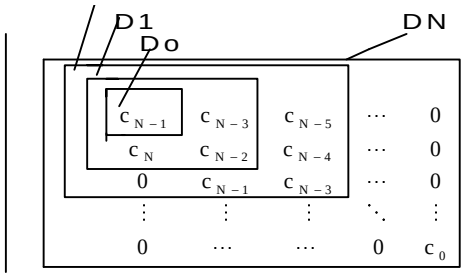
$$z = \frac{1+\frac{T}{2}w}{1-\frac{T}{2}w} \qquad (11)$$

The transformed characteristic equation is given by :

$$D(z)=0 \xrightarrow{z=f(w)} D(w) = c_N w^N + c_{N-1} w^{N-1} + \ldots c_1 w = 0 \qquad (12)$$

Where the coefficients ci are function of the variables ((ai,bi)).

The equivalent Routh Hurwitz Matrix and its sub determinants Di of the equation defined in (12)are :



(13.1)

According to the Routh Hurwitz Criteria, the poles of the equivalent linear system are stable if the following inequalities are respected :

$$\bullet\ \forall i \in [0,N],\ c_i > 0 \qquad (14.1)$$

$$\bullet\ \forall i \in [0,N], D_i > 0 \qquad (14.2)$$

The Lienard Chipart modified criteria reduce the inequalities in (14.2) by testing only the sign of the even (or odd) sub determinants. The stable pole criteria are therefore defined by :

$$\bullet\ \forall i \in [0,N],\ c_i > 0 \qquad (15.1)$$

$$\bullet\ \forall (2\times i) \in [0,N],\ D_{2i} > 0 \text{ or } \forall (2\times i+1) \in [1,N],\ D_{2i+1} > 0 \qquad (15.2)$$

Non overload and recovery criteria : These conditions are deducted from the local behavior of the SD which is described by the state variable equations given in (3) and (4). We recall that in a stable SD, the integrators outputs must lie below the clipping level L under normal operating conditions. Clipping is a sign of instability in the global system and occurs when one or more state variables present amplitudes larger than the maximum allowed output swing L. The integrator clips this amplitude to the value L. Linear range operation and clipping behavior of a given integrator are respectively summarized by expressions (16) and (17):

$$\forall n \in IN,\ \text{if } \left|v^*_i(n)\right| \le L \Leftrightarrow v_i(n) = v^*_i(n) \qquad (16)$$

$$\forall n \in IN,\ \text{if } \left|v^*_i(n)\right| > L \Leftrightarrow v_i(n) = L \times \text{sgn}(v^*_i(n)) \qquad (17)$$

where $v_i^*(n)$ is the value of the state variable defined in (3) or (4) at sampling time t= n*Ts and $v_i(n)$ represents the value actually present at the output of the i-th integrator in an Nth order SD.

Non overload under normal operating conditions implies that relation (16) be satisfied by the state variables defined in (3) and (4). That is, the state variables must vary in the range [-L, L].

A linearization of (3) and (4) and a study of upper and lower bounds of the state variables was performed. The consideration of worse cases for which a state variable reaches an extreme (-L, L or 0) have lead to a set of inequalities which link the coefficients of the system. These relations form the non overload and recovery criteria. As an example we shall treat the basic steps in the study of the state variable equation of the last integrator defined in (4).

We recall the state variable equation u(n) of the last loop:

$$u(n) = u(n-1) + b_N v_{N-1}(n-1) - a_N Vref \times \text{sgn}(u(n-1)) \qquad (4)$$

Let us consider the case for which u(n-1) = L.

According to (5) we get sgn(u(n-1))=+1 and u(n) becomes : $u(n) = L + b_N v_{N-1}(n-1) - a_N Vref$ (I)

The state variable v_{N-1} is bounded by the clipping level L : $-L \le v_{N-1}(n-1) \le L$ (II)

Therefore relation (I) can be bounded as follows : $L - (b_N L + a_N Vref) \le u(n) \le L + (b_N L - a_N Vref)$ (III)

The state variable u(n) must obey the relation : $-L \le u(n) \le L$, therefore the upper and lower boundaries, which are values that u(n) can take, must satisfy :

$$\left|L - (b_N L + a_N Vref)\right| \le L \text{ and } \left|L + (b_N L - a_N Vref)\right| \le L \qquad (1V)$$

Relation (IV) is satisfied if : $b_N L + a_N Vref \le 2L$ and $b_N L - a_N Vref \le 0$ (V)

A similar study for the case u(n-1) = -L and the case u(n-1) = 0 is done. The resulting inequalities are summarized below :

$$b_N L \pm a_N Vref \le L,\ b_N L - a_N Vref \le 0,\ a_N Vref \le \frac{L}{2} \qquad (VI)$$

The common region to all the inequalities defined in (VI) is graphically represented in Fig. 5. We see that the plane is divided in two regions: an overload and a non overload region. Clipping is avoided when the coefficients (a_N,b_N) are chosen in the non overload region.

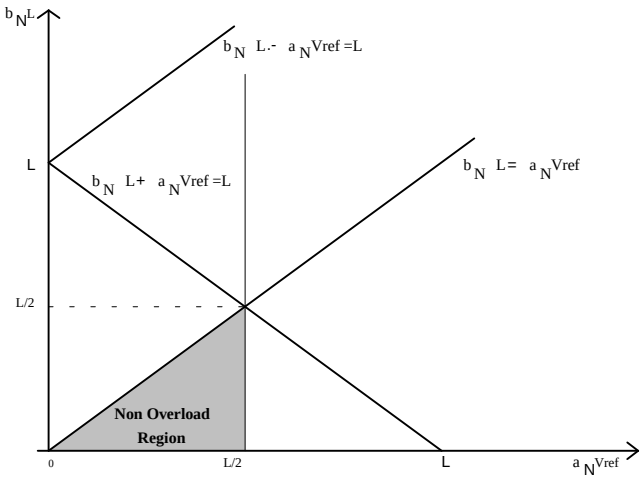


Fig.5 Parameter limitation due to non overload considerations

The study of the state variable equations defined in (3) has lead to similar results for the coefficients ((ai,bi)), leading to triangular shaped regions with different summits and base values. A common result to (3) and (4) is that the feedback signal of a given inner loop must be greater in amplitude than the maximum corresponding feed forward signal. That is :

$$b_1 X_{max} < a_1 V_{ref} \quad \text{and} \quad \forall i \in [2, N], \quad b_i L < a_i V_{ref} \qquad (18)$$

In case of overload in the system the feedback signal must be large enough to reduce the increase of amplitude in the feed forward paths. The larger the feedback signal amplitude in comparison to the feed forward signal, the stronger the control of the quantizer on the global system, therefore the faster the recovery after an overload. Recovery speed in the inner loops and in the system as a whole is therefore dependent on the ratio of the corresponding feed forward signal to the feedback signal in the same way as is the stability. This means that if the stability constraints are met, a fast recovery is obtained at the same time.

Existence of conflicting constraints: According to (10.1) and (10.2),high performance requires large feed forward coefficients and a large feedback coefficient in the first loop. By considering the non overload and recovery constraints, the maximization of (10.1) and (10.2) requires to choose the values of the coefficients close to the peak of the triangle regions defined as in Fig. 5. However, the closer we get to the peak the tighter become the stability and recovery constraints. Moving away from the peak results in looser stability and recovery constraints but also performance degradation. We realize that the stability and performance constraints scale the coefficients in contradictory directions. Stability, however, is a necessary condition. A system which is instable is not usable and therefore the notion of performance is useless when stability is not guaranteed.

Application of interactive optimization techniques: We see that we are confronted to a typical nonlinear problem. In order to find a solution which best meets the stability and performance requirements in higher order SD ADCs, a nonlinear optimization tool can be applied associated with a simulator whose role is to analyze the dynamic behavior of a SD for a given set of parameters. For our purpose we have used CANDI[14] which is based on nonlinear interactive optimization. The simulator which we have written computes the dynamic behavior of a given SD with the help of the state variable equations defined in (3) and (4) as well as the performance and condition functions obtained in the mathematical analysis described in part II. The optimization problem was described in a specification file integrated in CANDI. Through successive interactive approximations the difference between the specified goal and the state of the given Nth order SD is minimized and an optimum value which best meets our specifications is obtained. Figure 6 illustrates the basic steps of the interactive optimization. The various analysis methods in CANDI enabled us to determine coefficients with a minimum sensitivity to the parameter deviations present in practice.

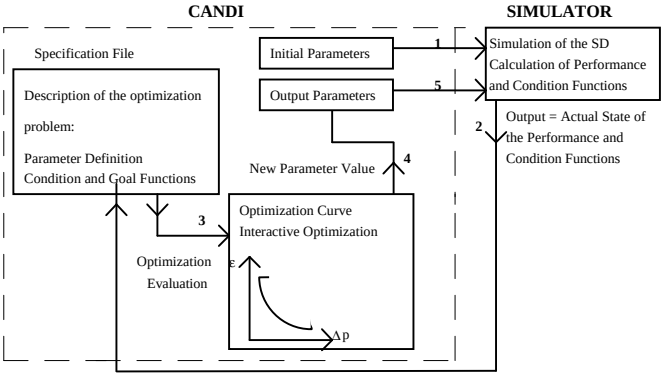


Figure 6: Interactive Optimization in Candi

Performance comparison: A stable higher order SD must present superior performance than a lower order SD for it to be competitive. This may not be evident since the functions defined in (10.1) and (10.2) decrease with the order of the SD due to stability constraints. In other words the down scaling of the coefficients in higher order must not cause performance degradation of a higher order system in comparison to a lower order SD. This means that once the optimal coefficients of a given order are obtained we must calculate the minimum value of the oversampling ratio M for which the given Nth order SD is advantageous as compared to a lower order.

For this we have considered the ratio of the inband quantization noise in an Nth Order SD to the inband quantization noise in an N+1th order SD defined by the function h :

$$h = \frac{N_o(\text{SD of order N})}{N_o(\text{SD of order N}+1)} \propto \frac{a_1 \prod_{i=2}^{N+1} b_i}{a'_1 \prod_{i=2}^{N} b'_i} xM = RxM \qquad (19)$$

The N+1th order SD reduces the quantization noise in the baseband more than an Nth order SD when h is greater than 1. This implies that M must be greater than

1/R. Similarly the SNR_{peak} of an N+1th order is greater than that of an Nth order when M is greater than a factor 1/Q :

$$g = \frac{SNR_{peak}(\text{SD of order } N+1)}{SNR_{peak}(\text{SD of order } N)} \propto \frac{\prod_{i=1}^{N+1} b_i}{\prod_{i=1}^{N+1} b'_i} xM \qquad (20)$$

This implies that an N+1 order SD is more performant than an Nth order SD for values of the oversampling ratio M which are greater then a value P defined as the maximum of 1/R and 1/Q.

IV. Results

The results on 3rd, 4th and 5th order SD which have been optimized using the method proposed here.

Performance and stability constraints: Figure 7 compares the inband quantization noise reduction (represented here by the inverse of the inband quantization noise), for the different structures, as a function of the oversampling ratio M. The plane is separated in two regions, a non performant region and a performant region. We see that higher order SD are interesting only when the oversampling ratio M is greater than a critical value M_{crit}~30. This value is much greater than 2 which is predicted for the noise term of higher order SD given in [5]. The reason of this shifting is related to stability constraints which have down-scaled the coefficients of the higher order SD and therefore limited the value of the terms (10.1) and (19) below one. This results in performance degradation in higher order SD for oversampling ratios smaller than 30. In practice however, the typical values of M are between 64 and 128, so the use of our optimized higher order SD is still attractive.

We have mentioned in the performance considerations that the coefficient terms in (10.1) and (10.2) were non-existent in the noise and signal to noise ratio peak value calculations present in the literature. This was basically due to the fact that these factors were taken equal to 1. Figure 8 shows the difference in noise reduction in our optimized stable 3rd order SD and the one described in the literature for which (10.1) is equal to 1[5]. The noise reduction in a conventional 2nd order SD (SD2) is taken in Fig. 8 as a reference. Due to stability constraints, the noise reduction calculations given in the literature are unrealistic because they lead to instable structures[1]. Thus the noise reduction in a third order SD which verifies the stability constraints is 20dB less than the level predicted by the noise expression in [5] and the performant zone is shifted from values of M greater than 2 (point A in Fig. 8) to values of M greater than 25 (point B in Fig. 8).

The Signal-to-Noise Ratio curves of the optimized 3rd, 4th and 5th order structures for an Oversampling ratio of M=128 are presented in figure 9. The simulations were done using Tosca [15] which simulates the behavior of SD ADCs. The graph shows that for M= 128, the Signal-to-Noise-Ratio (SNR) peak value of the new 3rd, 4th and 5th order SD are 107dB, 121dB and 132dB respectively and correspond to resolutions of 18, 20 and 22 bits.

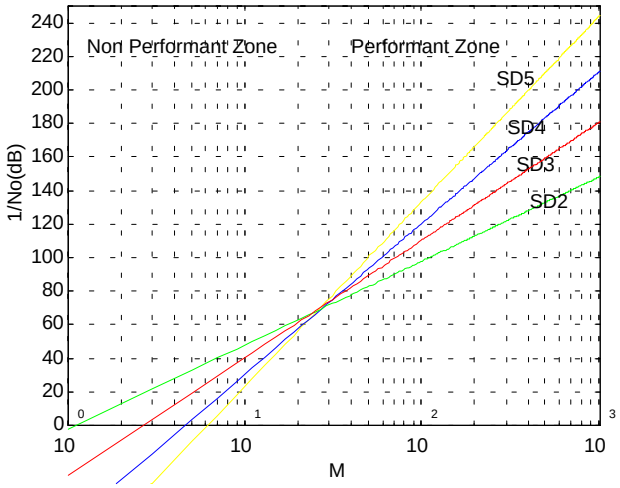


Figure 7 : Inband quantization noise reduction for SD ADCs optimized with the new algorithm

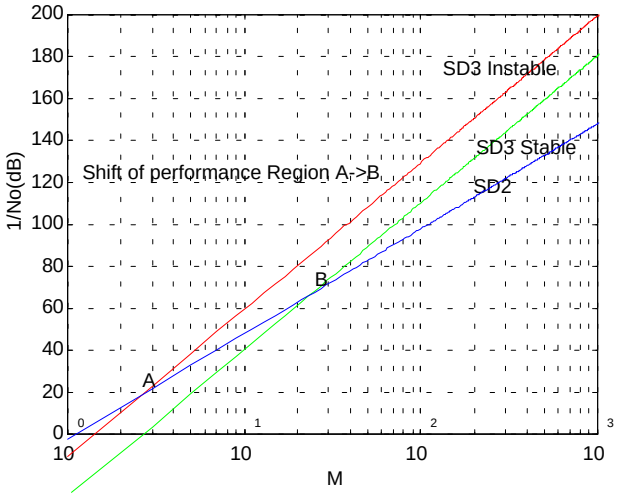


Figure 8:Noise reduction comparisson

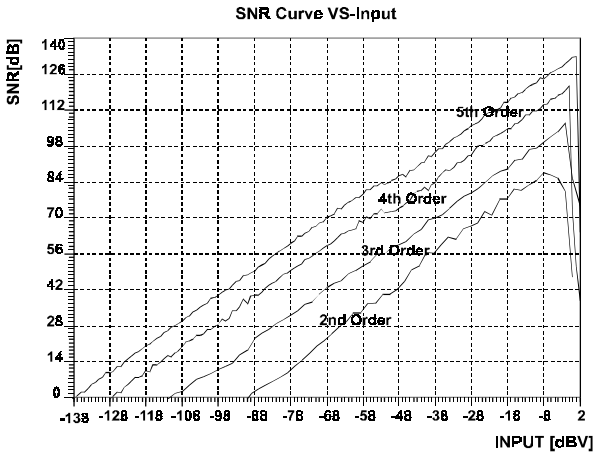


Figure 9 : SNR Curves for M=128

Non overload and recovery behaviors: Our 3rd, 4th and 5th order SD ADCs have similar local behaviors. The case of our 4th order SD is presented here. Only one

concrete example of a single loop 4th order SD has been described in the recent literature [6]. We shall compare the behavior of both converters under the same operating conditions. From Fig.9 we have seen that for M=128, our 4th order SD has a Signal-to-Noise- Ratio peak value of 121dB. This is 6dB (1 bit extra resolution) of improvement in our 4th order SD as compared to [6] under the same conditions. We shall now show that significant improvements in the recovery behavior are also visible in our new structure. We shall from now on designate the 4th order SD of [6] by sd4s and our 4th order by sd4.

We have simulated under Matlab_Simulink [16] the behavior of both converters under normal operating conditions, during an overload and during the recovery phase after an overload. The observation is done at the output of the four integrators which compose the SD. The integrator clipping level is defined by L= 2V. We shall designate the input of sd4s and the consecutive output of its four integrators by 'ins', 'ins1', 'ins2', 'ins3' and 'ins4'. In the same manner, we shall designate by 'in', 'in1', 'in2', 'in3' and 'in4' respectively the input of sd4 and the outputs of its four integrators. Due to the symmetrical behavior of the converter we only consider positive variations at the input. A worse case configuration has been considered for the test. The input signal is initially set to the maximum amplitude Xmax the SD can support without overloading. We shall call this phase the normal operating phase which lasts till sampling time t= 300*Ts (Ts= sampling period). From t = 300*Ts to t= 500*Ts an overload signal of 2V is forced at the input of the converters. This phase is designated as the overload phase. The overload phase is followed by a normal operating phase where the input signal returns to Xmax. The results are plotted in Figures 10a and 10b.

The simulations show that the output of the integrators in both converters stay below their clipping level in the normal operating phase. During the overload phase all integrators in sd4s remain frozen at the clipping level. The overload behavior of our structure is different. The first three integrators clip frequently but do not remain in a frozen state, as for the last integrator, saturation does not occur. Looking at the recovery behavior after t= 500*Ts, we observe an immediate recovery of sd4 (after t= 6*Ts) as compared to sd4s, where normal operation occurs after 50 sampling periods. We explain the difference in recovery by the difference in clipping behavior during overload in the two structures and by the behavior of our last stage which never saturates as opposed to the one in sd4s. Since the last integrator never saturates, the input to the 1-bit quantizer will never overload. This implies that the 1-bit quantizer maintains a continuous control of the system via the feedback paths and therefore enables a quicker recovery in the previous stages of the SD after the overload phase. Behavioral simulations of both ADCs after powerup have been done: the highest dc input Xmax is injected at the input of the SD and the integrators are initially set to 2V. The simulations have shown similar recovery behaviors as in fig. 10b. and confirmed the fast recovery in our structure.

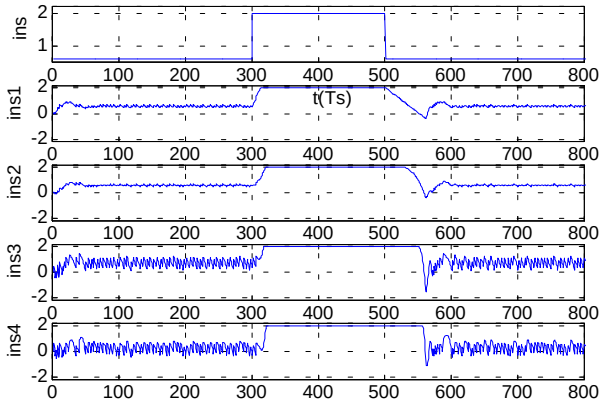


Figure 10a

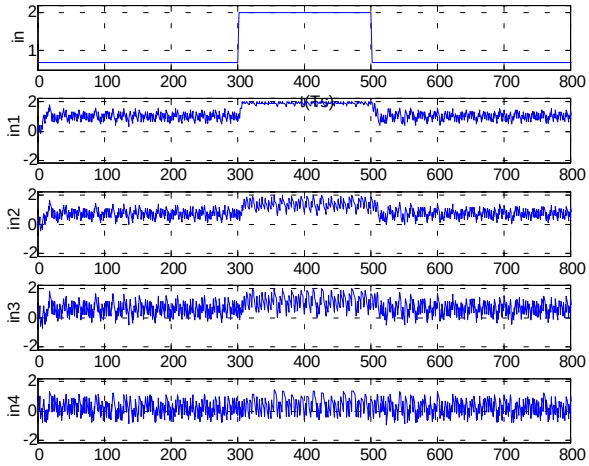


Figure 10b
Behavior of the integrators under different input conditions in (10a) sd4s (10b) sd4

Practical realization: In practice a third order SD whose coefficients were determined with our methodology has been realized in a 5V, 1µm p-well CMOS process, to demonstrate the feasibility of our method. Circuit level simulations under SABER [17] confirmed the behavior of the internal nodes as shown in fig. 10b. The integrators were realized with Switched Capacitor Integrators[18]. Due to strong thermal and flicker noise present in the operational amplifiers of these integrators our resolution was limited by circuit noise rather than by quantization noise. However the main reason for our implementation was to demonstrate the reliability of our method from the stability point of view, since the stability problem in higher order SD was the main reason for which these structures were not used up to now. No reset circuits were used in our SD so that the control of the stability was left to the converter itself. The measured spectrum of the designed SD is presented in Figure 11. The form of the spectrum is characteristic of a stable 'noise shaping' operation in a SD ADC. The converter showed no instability for worse case conditions in the allowed operating range and exhibited immediate recovery after overload.

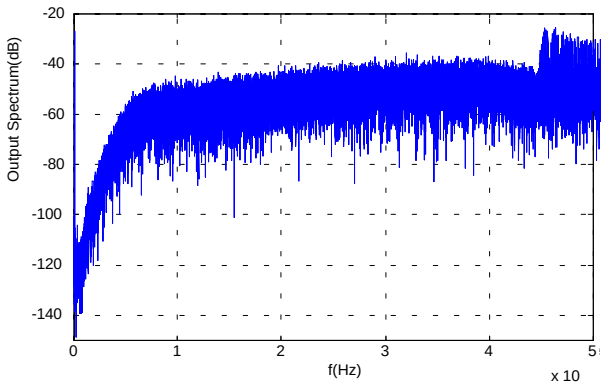


Figure 11 Measured Output Spectrum of the 3rd order SD

V. Conclusion

A new algorithm has been described for the determination of an optimum network scaling in SD ADCs of order three or more. This method brings new insight into the correlations linking internal parameters with the stability and performance in higher order SD ADCs and has shown that instability in higher order SD found in the past was due to inadequate network scaling. It has also shown that performance predictions made until now are unrealistic due to stability constraints. We believe that the application of this methodology to cascaded SD could also bring more insight to the understanding of the correlation between the performance of these structures and the network scaling and thus help the designer to choose a solution which best meets its specification. It also appears promising to apply this method to higher order SD ADCs based on filter topologies since it may eliminate the need for additional reset circuitries. The reliability of our method has been confirmed in simulations and through a practical implementation of a third order SD, whose network scaling was based on this method.

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