Expected Current Distributions for CMOS Circuits*

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Abstract

The analysis of CMOS VLSI circuit switching current has become an increasingly important and difficult task from both a VLSI design and simulation software perspective. This paper presents a new static switching current estimation algorithm based on the idea of "Expected Current Distributions" (ECDs). Unlike previous "expected waveform" approaches, ECDs model not only the expected value of switching current waveforms over all time, but also the variances and covariances of all waveform segments as well. This extra information allows a switching current waveform to be modeled by a random process with both first and second order ensemble statistics. This specification provides the power spectral density of the switching current and allows the use of traditional frequency domain noise analysis to simulate the behavior of the switching current in the electrical supply network. An ECD simulation procedure is described and results are presented for the ISCAS85 combinational benchmark circuits. Estimated quantities include total average and RMS VDD current, the autocorrelation function of the total VDD current waveform, and per-gate average and RMS VDD currents. The results show speedups of up to 100x and good agreement with respect to figures obtained using dynamic logic simulation and statistical mean estimation.

1. Introduction

Many issues of integrated circuit reliability related to CMOS switching current are gaining importance as technology improvements cause VLSI wires to have both increased current densities and dominant electrical effects. These issues include dynamic power dissipation, electromigration, false switching due to "ground bounce" or capacitive signal coupling, and noise coupling between analog and digital circuits. Unfortunately, attempts to accurately model such effects are forced to fight a war on two fronts: not only must designers simulate the *logical behavior* of the digital circuit to ascertain its many switching currents, but they must also simulate the *electrical effects* of these currents as they pass through complex VLSI metallization structures.

This paper presents a new static switching current estimation algorithm based on the idea of "Expected Current Distributions" (ECDs). In contrast to previous "expected waveform" approaches, ECDs model not only the expected value of switching current waveforms over all time, but also the variances and covariances of all waveform segments as well. This extra information allows a switching current waveform to be modeled by a well defined *random process* with both first and second order ensemble statistics [7]. Such a specification provides the *power spectral density* of the switching current and allows the use of traditional *frequency domain noise analysis* to simulate the behavior of switching current in the electrical supply network. Due to space limitations, this paper concentrates solely on ECD simulation. An ECD-based frequency domain approach to supply network analysis is described in [4].

2. The Expected Current Distribution (ECD)

The Expected Current Distribution (ECD) is a statistical waveform model for digital logic gate switching currents. In this model, time is divided into clock-cycle-width portions and the ensemble of possible waveform shapes that can occur in any one cycle are modeled by the ECD. To limit the complexity of the modeling data, the ECD assumes waveforms are discretized with a fixed timebase and contain piecewise constant (PWC) segments within each discrete time region. Such a model of CMOS circuit VDD switching current is shown in Figure 1. An ECD is also shown which models the entire waveform using statistics of all possible segment heights within each single cycle period. Segments in different cycles are assumed to vary independently, which is a valid assumption for combinational circuits operating with random inputs but may not hold for sequential circuits due to the correlation of the present state bits. The ECD stores the following statistics

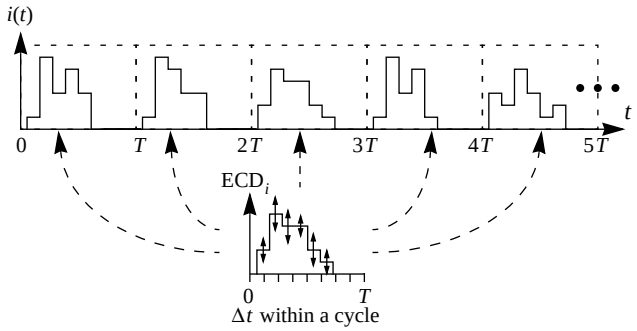

Figure 1. Basic ECD concept. A waveform is conceptually divided into clock-cycles and all possible shapes in any cycle are modeled by statistics in the ECD. The arrows shown in the ECD depict knowledge of segment height (co)variances.

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about each segment height $w(t_i)$ within a single clock cycle:

$$\begin{aligned} w(t_i) &= \text{r.v. for waveform segment height at time offset } t_i \\ \mathrm{E}[w(t_i)] &= \text{expected value of segment height } w(t_i) \\ \mathrm{Var}[w(t_i)] &= \text{variance of segment height } w(t_i) \\ \mathrm{Cov}[w(t_i), w(t_j)] &= \text{covariance of segment heights } w(t_i) \text{ and } w(t_j) \\ f_{w(t_i)} &= \text{Boolean occurrence func. for segment height } w(t_i) \end{aligned} \quad (1)$$

Each collection of information about the random variable $w(t_i)$ is called "the ECD component at time t_i." Of particular importance is the concept of a "Boolean occurrence function." These functions describe when a segment height is non-zero in terms of logical circuit quantities and provide a means to compare the behavior of switching currents at different times within a cycle and/or in different circuit modules.

2.1. Approximating ECD Component Covariances

What separates the ECD from an "expected waveform" is the covariance data it can contain. This information may be explicitly specified by a numeric covariance matrix or approximated using the Boolean occurrence functions of each component. If neither the covariance matrix nor any Boolean occurrence functions are specified in the ECD, all covariances are assumed to be zero.

The Boolean occurrence function $f_{w(t)}(\vec{v})$ describes when the waveform segment height at time t is non-zero in terms of logic circuit quantities, $\vec{v}$. The function $f_{w(t)}(\vec{v})$ may be specified exactly using its OBDD [2] or approximately using its BAM cofactor probabilities [10]. An approximate correlation coefficient between two segment heights may be found by considering the probability of each occurrence function as the parameter for a Bernoulli distribution [5] and using the standard definition of covariance:

$$\begin{aligned} X &= \text{r.v. equal to } f_X(\vec{v}), \text{ Bernoulli param } p_X = P(f_X(\vec{v}) = 1) \\ Y &= \text{r.v. equal to } f_Y(\vec{v}), \text{ Bernoulli param } p_Y = P(f_Y(\vec{v}) = 1) \\ XY &= \text{r.v. equal to product of r.v.s } X \text{ and } Y, \\ &\quad \text{Bernoulli param } p_{XY} = P(f_X(\vec{v}) \wedge f_Y(\vec{v}) = 1) \\ \mathrm{E}[XY] &= \mathrm{E}[X]\mathrm{E}[Y] + \mathrm{Cov}[X, Y] \\ &= \mathrm{E}[X]\mathrm{E}[Y] + \hat{\rho}\sqrt{\mathrm{Var}[X]\mathrm{Var}[Y]} \\ \hat{\rho}_{X,Y} &= \frac{p_{XY} - p_X p_Y}{\sqrt{(p_X - p_X^2)(p_Y - p_Y^2)}} \end{aligned} \quad (2)$$

$\hat{\rho}_{X,Y}$ may then be used to approximate the covariance between two actual segment height values:

$$\mathrm{Cov}[w(t_i), w(t_j)] \approx \hat{\rho}_{w(t_i), w(t_j)}\sqrt{\mathrm{Var}[w(t_i)]\mathrm{Var}[w(t_j)]} \quad (3)$$

3. ECD Simulation

The VDD current of a CMOS logic gate is a strong function of the logical switching activity of its output node. Therefore, circuit VDD current may be simulated by first estimating gate level switching activities and then hierarchically combining these results to form gate, module and circuit ECDs. Three previously published combinational circuit switching activity estimation algorithms have been implemented for this express purpose [6][9][10]. All gates are given integer delays and each switching activity simulation algorithm has been programmed to produce a *probabilistic waveform* [8][9], PW_N, for each circuit node N. PW_N summarizes the switching activity of node N with a set of probabilities $\{\mathrm{up}_N(t_i), \mathrm{dn}_N(t_i) \mid i = 1 \ldots k\}$ which denote the chance of an upward or downward transition on that node at time offset t_i within a clock cycle. Depending the particular simulation algorithm, varying degrees of underlying functional information may also stored for each probability. Further discussion of these methods is found in [4].

3.1. Building Gate ECDs

The ECD for a single gate G with output node N is constructed using PW_N. Each upward transition on N is assumed to generate a user-specified, PWC current pulse $z_G(t)$ on the gate VDD pin [1]. (Downward transitions can also generate VDD pulses but this effect, which can be handled easily, is currently ignored.) In this manner, the ECD for a single gate is constructed from a sum of random current pulses, one for each up transition in the gate output node probability waveform.

The ECD for a single transition probability waveform

Figure 2 illustrates the ECD calculation for a gate G with a single possible output transition. Each ECD component $w(t)$ has a Bernoulli distribution with mean and variance:

$$\begin{aligned} \mathrm{E}[w(t + \Delta t)] &= z_G(\Delta t)\mathrm{up}_N(t) \\ \mathrm{Var}[w(t + \Delta t)] &= \mathrm{E}[w(t + \Delta t)^2] - \mathrm{E}[w(t + \Delta t)]^2 \\ &= z_G(\Delta t)^2[\mathrm{up}_N(t) - \mathrm{up}_N(t)^2] \end{aligned} \quad (4)$$

Any underlying functional information available for the up transition probability is also saved as $f_{w(t+\Delta t)}$ (*e.g.*, its OBDD or its BAM cofactor probabilities).

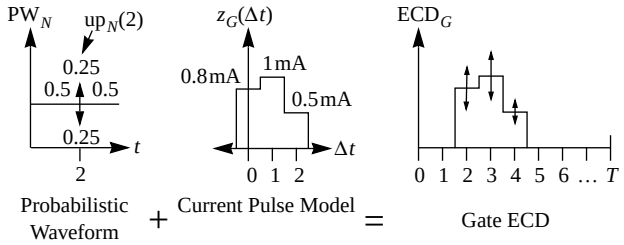

Figure 2. Constructing a gate ECD from the output node probabilistic waveform and a VDD current pulse model. All components in this ECD are necessarily 100% correlated.

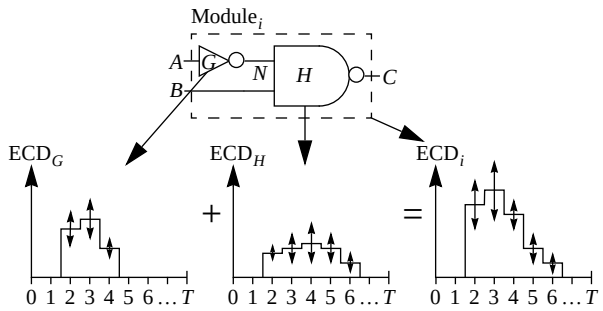

Figure 3. Module ECD composed by sum of gate ECDs.

Summing ECDs for a multi-transition probability waveform

If a probability waveform has more than one transition time, one "sub-ECD" is generated for each transition and all sub-ECDs are summed to form the gate ECD. All unique sub-ECD component times are retained and sums of sub-ECD components are treated as a sum of random variables (Boolean occurrence functions are logically OR-ed):

$$\begin{aligned} \mathrm{E}[w(t_i)] &= \mathrm{E}[w_1(t_i)] + \mathrm{E}[w_2(t_i)] + \mathrm{E}[w_3(t_i)] \\ \mathrm{Var}[w(t_i)] &= \mathrm{Var}[w_1(t_i)] + \mathrm{Var}[w_2(t_i)] + \mathrm{Var}[w_3(t_i)] \\ &\quad + 2\mathrm{Cov}[w_1(t), w_2(t)] + 2\mathrm{Cov}[w_2(t), w_3(t)] \\ &\quad + 2\mathrm{Cov}[w_1(t), w_3(t)] \\ f_{w(t_i)}(\hat{v}) &= f_{w_1(t_i)}(\hat{v}) \vee f_{w_3(t_i)}(\hat{v}) \vee f_{w_3(t_i)}(\hat{v}) \end{aligned} \quad (5)$$

Covariances in (5) are calculated according with equation (3). If no functional information is available, a pre-specified numeric correlation coefficient is used in (3), *e.g.*, $\rho = 0$.

3.2. Building Module ECDs

Module ECDs are simply sums of gate ECDs and/or other module ECDs. A module ECD summation is depicted in Figure 3. It is important to note that this procedure assumes a perfectly conductive, single root VDD current supply network within the module.

4. Using the ECD as a Random Process Model

Since ECD_i describes the *single cycle* statistics of a random current waveform $i(t)$, an *N-cycle* statistical description of the waveform is formed by appending N copies of ECD_i. This operation assumes events in different cycles are independent and is illustrated in Figure 4. As $N \to \infty$, the expected value and variance of the random variables in the concatenation completely specify the first-order ensemble statistics for a stochastic process $\boldsymbol{i}(t)$ [7].

Since all random processes analyzed in this research begin at a known time offset (*i.e.*, simulation time $t = 0$), they are *stationary* and afford the use of single-parameter auto- and cross-correlation functions, $R_{ij}(\tau)$, to describe their second-order statistics [7]. The general shape for $R_{ij}(\tau)$ is

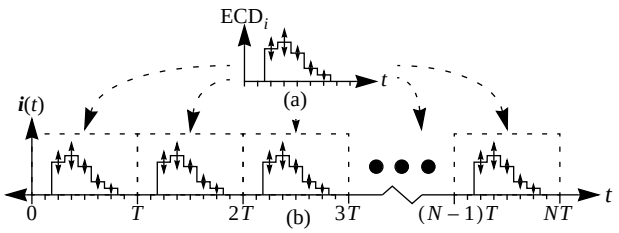

Figure 4. Construction of the ensemble statistics for a stochastic VDD current waveform $\boldsymbol{i}(t)$ described by ECD_i.

deduced by exploiting the cyclic structure of the product $\boldsymbol{i}(t)\,\boldsymbol{j}(t)$. Specifically, at any given t, $\boldsymbol{i}(t)\,\boldsymbol{j}(t)$ has the same distribution as the product of random variables $w_i(t \bmod T)w_j(t \bmod T)$. After a bit of effort [4], this idea leads to the following definitions:

$$\begin{aligned} R_{ij}(\tau) &= q(t) \otimes \sum_{m=0}^{T\Delta t-1} \left[b_m \delta(\tau - m\Delta t) + \sum_{k=-\infty}^{\infty} a_m \delta(\tau - m\Delta t + kT) \right] \\ q(t) &= \text{triangle function centered at origin with base width } 2\Delta t \\ \Delta t &= \text{circuit timebase} \\ a_m &= \text{weight of periodic impulse train in } R_{ij}(\tau) \text{ with shift } m\Delta t \\ &= \sum_{t_2 - t_1 = m\Delta T} \mathrm{E}[w_i(t_1)]\mathrm{E}[w_j(t_2)] \\ b_m &= \text{weight of single impulse in } R_{ij}(\tau) \text{ at } |\tau| = m\Delta t \\ &= \sum_{t_2 - t_1 = m\Delta t} \mathrm{Cov}[w_i(t_1), w_j(t_2)] \end{aligned} \quad (6)$$

A typical autocorrelation function is depicted in Figure 5. In general, $R_{ii}(\tau)$ is a symmetric, T-periodic function with some aberration near $\tau = 0$ due to any non-zero covariance produced by correlation between pairs of segment heights.

5. Results and Analysis

The algorithm detailed above has been applied to the ISCAS85 combinational benchmark circuits. All gates are given integer delays and piecewise constant VDD current pulses as a function of gate fanout. Two different gate switching activity simulation algorithms were used, AI and BAM. AI is based on [9] and assumes all logic signals are *independent*. BAM is based on [10] and approximates the correlation between signal probabilities using probabilities of function cofactors. AI and BAM results are benchmarked against figures found using Monte Carlo logic simulation [3][4] with identical gate models. With this technique, simulations of 50-200 random vectors were repeatedly performed until each result was estimated to within 5% accuracy with 99% confidence.

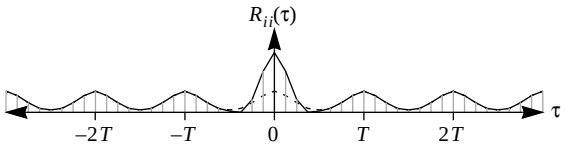

Figure 5. Typical autocorrelation function derived from an ECD.

	Logic Simulation vs. ECD Simulation Runtimes			Total Avg. Current ECD Prediction Errors		Total RMS Current ECD Prediction Errors		Per-Gate Average VDD Current Absolute ECD Prediction Errors			
	seconds		speedup					AI		BAM	
Circuit	LOGSIM	AI	BAM	AI	BAM	AI	BAM	Mean	Max	Mean	Max
c432	133.3s	71x	9x	-5%	-1%	-17%	9%	11%	42%	4%	21%
c499	94.38s	90x	10x	-1%	-1%	-2%	-2%	1%	9%	1%	9%
c880	432.7s	92x	5x	-5%	-5%	-9%	-5%	10%	51%	6%	32%
c1355	626.8s	60x	4x	-26%	-5%	-24%	18%	17%	66%	12%	54%
c1908	2569s	114x	9x	-40%	-26%	-37%	3%	28%	64%	17%	52%
c2670	1429s	88x	1x	-23%	-13%	-24%	-8%	20%	75%	10%	65%
c3540	3575s	83x	4x	-26%	-21%	-28%	-10%	19%	94%	13%	82%
c5315	4309s	69x	*	-34%	*	-28%	*	24%	78%	*	*
c6288	12850s	18x	*	-30%	*	-33%	*	31%	64%	*	*
c7552	4951s	37x	*	-34%	*	-32%	*	26%	84%	*	*

Table 1. ECD simulation results versus logic simulation results. * indicates BAM-PS simulation exceeded 256M memory limit.

Simulation results are given in Table 1. RMS results are generally better than average results due to the conservative nature of the covariance calculation described in section 2.1. That is, overestimates of the covariances tend to offset underestimates of averages. The quality of gate current estimates varies. As a rule, AI error distributions are lop-sided with many more under-estimates than over-estimates. Furthermore, these distributions commonly have a tail running out to -80% or even -100% error, indicating that assumed signal independence may be too severe of an approximation for gate-level current estimates. In contrast, BAM error distributions are more symmetric and narrow with a higher peak for small errors. Such behavior is promising and provides impetus for further research into improving the memory and time requirements for BAM ECD simulation.

Typical ECD predictions of total VDD current are shown in Figure 6(a,b). In general, ECD predictions are accurate for small values of t and tend to deviate from Monte Carlo results at higher t due to inaccurate estimates of the switching activity at the deepest gates in the circuit. Typical ECD predictions for the autocorrelation of total VDD current are shown in Figure 6(c,d). For efficiency, Monte Carlo estimates were found only over the first period of the positive symmetric half of each function. Therefore, even though ECD simulation predicts the entire autocorrelation function, Figure 6 shows $R_{ii}(\tau)$ only for $0 \le \tau \le T$ (*cf.* Figure 5). It is revealing to study the variation of each function. Near $\tau = 0$, the value of the function measures the covariance between closely spaced pulses in the current waveform. Values at increasing τ measure the covariance between current pulses that occur farther apart. The autocorrelation function results can also be used to infer the quality of their associated power spectral density predictions. The prediction error of each curve near $\tau = 0$ is an indication of how well that correlation function will predict the *continuous* components in the power spectral density (PSD) of the waveform. In contrast, the accuracy of the correlation function at $\tau = T$ is a measure of how well the function will model the *periodic impulse* components in the PSD.

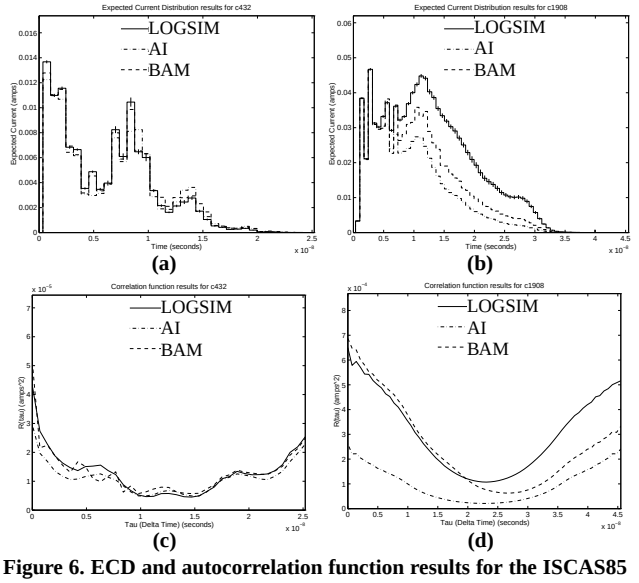

Figure 6. ECD and autocorrelation function results for the ISCAS85 c432 (a,c) and c1908 (b,d) circuits.

It should be noted that ECD simulation produces more information, as well as more flexible information, than comparable logic simulations. For example, while Monte Carlo simulations can be used to estimate average or RMS gate currents, ECD simulations estimate the complete ECD of gate switching currents, which is capable of predicting not only average and RMS gate currents, but also autocorrelation functions and power spectral densities as well.

6. Summary

This paper has presented a new method for CMOS switching current analysis. This method, based on the idea of "Expected Current Distributions," models the ensemble statistics of per-cycle current waveforms and facilitates the link between static switching current analysis and subsequent electrical simulation of the current supply networks.

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