# Accelerating Polynomial Modular Multiplication with Crossbar-Based Compute-in-Memory

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Abstract—Lattice-based cryptographic algorithms built on ring learning with error theory are gaining importance due to their potential for providing post-quantum security. However, these algorithms involve complex polynomial operations, such as polynomial modular multiplication (PMM), which is the most time-consuming part of these algorithms. Accelerating PMM is crucial to make lattice-based cryptographic algorithms widely adopted by more applications. This work introduces a novel highthroughput and compact PMM accelerator, X-Poly, based on the crossbar (XB)-type compute-in-memory (CIM). We identify the most appropriate PMM algorithm for XB-CIM. We then propose a novel bit-mapping technique to reduce the area and energy of the XB-CIM fabric, and conduct processing engine (PE)-level optimization to increase memory utilization and support different problem sizes with a fixed number of XB arrays. X-Poly design achieves  $3.1 \times 10^6$  PMM operations/s throughput and offers 200× latency improvement compared to the CPU-based implementation. It also achieves  $3.9 \times$  throughput per area improvement compared with the state-of-the-art CIM accelerators.

#### I. INTRODUCTION

Post-quantum cryptography (PQC) represents a critical area of research in the field of cryptography, driven by the impending threat posed by quantum computing to current cryptographic systems [1]. Many of these cryptosystems are currently being considered potential PQC candidates to address the challenges posed by quantum computing. Among these cryptosystems, lattice-based cryptography has attracted significant interest from the research community owing to its robust security guarantees and relatively low computational complexity [2], [3]. Lattice-based cryptographic algorithms rely on the mathematical concept of a lattice, which is an intricate structure formed by repeating patterns of points in a multi-dimensional space.

One of the fundamental building blocks of lattice-based cryptographic algorithms is polynomial operations, specifically, polynomial modular multiplication (PMM). PMM is a critical operation in ring learning with error (RLWE) theory, a key concept in lattice-based cryptographic algorithms. Moreover, PMM is the most time-consuming part of these algorithms. For example, recent studies show that PMM represents more than half of the computational workload for lattice-based homomorphic encryption (HE) on the cloud side [4], and more than 90% on the edge side [5]. Though algorithmic optimizations like Number-Theoretic Transform (NTT) [6] can decrease computation complexity, PMM latency is still

high [4], [5], [7]. As such, accelerating PMM is essential to improve the efficiency and practicality of lattice-based cryptographic algorithms.

Currently, there have been significant efforts to accelerate PMM, particularly through the use of NTT. NTT-based solutions, including those implemented on application-specific integrated circuits (ASICs) [8]–[10], field-programmable gate arrays (FPGAs) [11], and compute-in-memory (CIM) architectures [12]-[15], have demonstrated promising results in accelerating PMM. CIM-based PMM accelerators have gained attention for their effectiveness in reducing data transfer overheads by moving computation inside the memory [5], [14]. Work in [14] builds a Resistive RAM (ReRAM) based NTT accelerator that supports bit-wise computation inside the memory. Alternatively, [15] presents an in-SRAM NTT accelerator with bit-serial arithmetic operations. Crossbar arrays (XBAs) [16] is another popular CIM fabric that can support highly efficient vector-matrix multiplication (VMM) and is also actively being exploited for supporting high-throughput NTT-based PMM implementations [12], [17].

Existing research efforts to accelerate PMM using XBAs have primarily focused on using NTT-based approaches [12], [17]. Such solutions claim to achieve improvements of over  $50 \times$  compared to other CIM NTT accelerators. However, supporting PMM on XBAs comes with its own set of unique challenges. These challenges differ notably from those associated with the application of XBAs for the well-studied case of convolutional neural networks (CNNs). On the one hand, the high bitwidth and the large polynomial degree required for cryptographic applications result in a huge number of shiftadd operations, which incur high area and energy overhead. On the other hand, it remains an open question whether NTTbased solutions are the most suitable for XBA-based CIM architectures. Existing NTT-based PMM implementations on XBAs suffer from high area costs and limited scalability. These challenges restrict existing XBA-based solutions from achieving high performance for lattice-based cryptographic algorithms. Therefore, exploring alternative approaches to accelerate PMM to overcome these limitations is crucial.

This paper proposes a novel XBA-based PMM accelerator, X-Poly. Our solution distinguishes itself from existing XBAbased CIM methods by focusing on the non-NTT-based PMM. Our specific contributions are as follows:

- We present observations revealing that NTT-based PMM may not be the most suitable choice for XBA-CIM. Our extensive studies show that the convolution 1D (Conv1D) solution holds potential advantages regarding area, latency, and noise over NTT when implementing PMM on XBAs.
- We propose a new XBA bit mapping technique for highbitwidth, large polynomial degree data. The technique significantly reduces the overhead by removing most finegrained shift-add operations.
- We optimize data mapping at the processing engine (PE) level to support different problem scales with a fixed number of XBAs while maximizing throughput.

Our proposed X-Poly offers significant improvements in throughput and area consumption, making it a competitive solution for accelerating PMM in lattice-based cryptographic algorithms. Specifically, X-Poly achieves  $200 \times$  latency improvement compared with a CPU implementation. It also leads to  $3.9 \times$  throughput per area improvements compared with the state-of-the-art (SOTA) CIM accelerators for PMM.

## II. BACKGROUND

In this section, we discuss the role of PMM in cryptography, describe various PMM methods, review existing strategies for accelerating PMM, and review the concept of XBA.

## A. PMM in Cryptography

The RLWE problem [18], foundational to lattice-based cryptography [19], and specifically to HE schemes [20], leverages polynomials over a specific ring for its operations. HE, which enables arbitrary computations on encrypted data without prior decryption, ensures secure computation in untrusted environments while preserving data privacy. The primary computational bottleneck in HE arises from the need to perform polynomial arithmetic, particularly PMM [21]–[23]. Consequently, enhancing PMM's performance with respect to latency and energy consumption becomes critical in cryptography.

# B. PMM

Polynomial modular multiplication (PMM) is a fundamental operation in various applications, including cryptography, error correction codes, and polynomial arithmetic. It involves multiplying two polynomials and reducing the result modulo a given polynomial, resulting in a polynomial of a lower degree. By performing PMM, it becomes possible to efficiently compute large polynomial expressions while maintaining the desired modulus properties.

PMM can be accomplished using various methods, including the Conv1D approach and more optimized solutions like NTT as shown in Fig. 1(a). The Conv1D approach for PMM follows a straightforward procedure (Fig. 1(a)(1)). Two polynomials A(x) and B(x), with polynomial degree n and modulo q, are multiplied by summing the corresponding terms, akin to Conv1D computation with time complexity of  $O(n^2)$ . Then, the product undergoes modular reduction by dividing

#### (a) PMM Computation Flow (1) Conv1D (2) NTT



Fig. 1. (a) PMM computation flow using two implementations: (1) Conv1D (2) NTT. (b) PMM operation mappings on XBA: Conv1D mapping; (c) NTT mapping.

it with a modulus polynomial. The remainder is extracted polynomial long division to get the final result P(x).

NTT, alternatively, is proposed to reduce the computational complexity of PMM, particularly when the modulus polynomial satisfies specific properties, such as being irreducible and having a specific degree [6]. As depicted in Fig. 1(a)(2), the NTT approach involves transforming the polynomials into a different domain through NTT. During the NTT transformation, butterfly computations are performed by combining pairs of coefficients and multiplying them with twiddle factors, which are complex values associated with the modulus polynomial, resulting in the frequency-domain representation of the polynomial [6]. The process has a time complexity of  $O(n \log n)$ . Then in this transformed domain, element-wise multiplication is performed, followed by the inverse NTT (INTT) to convert the result back to the original domain to obtain the final polynomial P(x). Modular reduction is applied after each domain transformation.

The computational complexity of PMM in hardware is primarily influenced by two key factors: the polynomial degree n, which represents the number of coefficients in a polynomial, and the bitwidth k of modulo q, which signifies the size of these coefficients. In real-world applications, such as HE in privacy-preserving machine learning inference, these parameters can be quite substantial. For instance, the polynomial degree n in these applications can range from 256 to 8192, while the bitwidth k can vary from 16 bits to 64 bits [4], [24]. The magnitude of these degrees and bitwidths significantly intensifies the computational complexity of a single PMM, presenting a considerable challenge in the field.

# C. Related Work

In this section, we briefly review existing efforts to accelerate PMM. As existing work primarily employs NTT-based solutions, we focus our review accordingly, discussing both traditional ASIC and FPGA solutions, as well as CIM-based accelerators.

1) ASIC and FPGA solutions: Nejatollahi, H., et al. [11] proposed an innovative FPGA solution by designing two high-throughput systolic array polynomial multipliers, one based on NTT and the other on convolution. Their sequential NTT-based multiplier yielded a  $3 \times$  speedup over the SOTA FPGA implementation of the polynomial multiplier in the NewHope-Simple key exchange mechanism on an Artix7 FPGA [25].

ASIC implementations of lattice-based cryptographic protocols have also been actively studied. LEIA [9], a highperformance lattice encryption instruction accelerator, and Sapphire [10], a configurable processor for low-power embedded devices, both demonstrate substantial performance improvements and energy efficiency compared to prior ASIC designs.

There are also a number of works that directly accelerate HE, inherently accelerating PMM [4], [5], [7], [26], [27]. These works, which also typically use NTT, aim to create large-scale accelerators for privacy-preserving computations. Since this paper focuses on PMM, we will not compare it to these works. It suffices to say that an efficient PMM accelerator will directly help HE implementations.

2) Compute-in-Memory solutions: Previous research has introduced a variety of CIM kernels, including crossbars and general-purpose CIM. Ranjan et al. [28] have demonstrated that XBAs excel at performing VMM. Reis et al. [29] have discussed the general-purpose CIM enabling Boolean logic and arithmetic operations to be executed directly within the memory. Additionally, ongoing researches focus on exploring different underlying technologies for implementing these CIM kernels, including CMOS, ReRAM, and Ferroelectric FET (FeFET) [30]. These technologies are actively studied due to their potential to provide higher density and lower latency/energy overhead in CIM architecture. Several research efforts have explored the use of CIM architectures for the acceleration of the NTT, including CryptoPIM [14], MENTT [15], RMNTT [12] and BPNTT [13]. We compare X-Poly against these established researches, so we concisely introduce these approaches in the following discussion.

CryptoPIM, MENTT, and BPNTT proposed efficient NTT accelerators based on general-purpose CIM kernels. CryptoPIM [14] and MENTT [15], built on ReRAM and SRAM respectively, both introduced unique mapping strategies to streamline the data flow between NTT stages, leading to significant reductions in latency, energy, and area overheads. BPNTT presented an in-SRAM architecture using bit-parallel modular multiplication, significantly improving throughput-per-watt.

RMNTT [12] proposed an NTT accelerator using ReRAMbased XBAs. RMNTT stores the modified twiddle factor



Fig. 2. (a) XBA structure: a C columns x R rows array and the corresponding WL/BL driver. A p-bit ADC is used for converting analog signals to digital signals. (b) Illustration of the current summing scheme in XBA computation.

matrix in the XBAs and employs a modified Montgomery reduction algorithm to perform modular reduction on the VMM results. The evaluation results in [12] show that RMNTT outperforms other NTT accelerators in terms of throughput but incurs a large area overhead.

#### D. Crossbars

Given the competitiveness of XBA-based NTT accelerators, we consider leveraging XBAs to accelerate PMM. We briefly review the XBA basics below.

XBA [31] is one representative CIM kernel in which every input signal is connected to every output signal through their cross-points consisting of memory elements and selectors. XBAs can efficiently implement VMM and have been widely studied for CNNs. In particular, XBA implemented with nonvolatile memory (NVM) devices such as ReRAM [32] have gained popularity due to their high storage density, nonvolatility, and low energy consumption. However, XBAs face challenges stemming from the underlying memory devices and circuits. In-situ memory device nonidealities, e.g., non-linearity, thermal noise, and variations, impact computed accuracy.

Fig. 2(a) illustrates a general XBA structure. For each column, we adopt the current summing model as shown in Fig. 2(b). In this work, both input voltage  $(V_j)$  and memory cell states  $(G_{i,j})$  assume binary values, i.e.,  $I_i = \sum_{0}^{R-1} G_{ij} V_j$ , where  $V_j$  and  $G_{ij}$  are either 0 or 1. Binary XBAs exhibit greater robustness to device and circuit nonidealities, and offer improved scalability.

#### III. NTT vs. Conv1D

The choice of PMM algorithm is critical to achieving high performance in terms of speed, noise, and area in the context of the CIM computing paradigm as discussed in Sec. II-B. Two commonly used methods for performing PMM are Conv1D and NTT. Recent efforts utilizing XBAs for PMM have primarily focused on accelerating NTT-based methods [12] [17]. However, there is no systematic comparative study of which method, Conv1D or NTT, is a better fit for leveraging XBAs to accelerate PMM. We fill this gap with an in-depth investigation below. Our study reveals three key insights which favor the Conv1D over the NTT-based approach. First, data mapping complexity is higher when using NTT. Second, the Conv1D method potentially offers a better performance trade-off in terms of area and throughput, providing more opportunities for design scalability. Third, the noise growth is generally higher in the NTT approach than Conv1D, which can negatively impact the performance and accuracy of the system. Below, we elaborate on these insights.

## A. The Impact of Data Mapping to XBAs

To use XBAs for PMM, both NTT-based and Conv1Dbased PMM approaches require converting their respective operands into matrices and performing VMM on XBAs [12]. In the NTT-based approach, the twiddle factor of NTT must be converted into a matrix. In the Conv1D approach, one of the polynomials is transformed into a matrix, while the other remains a vector, facilitating the execution of VMM. Data mapping to XBAs in NTT and Conv1D can be better visualized in Fig.1(b) and (c). The figures show that the same number of memory cells are needed for both methods; thus, NTT does not provide benefits over Conv1D in terms of the XBA area. Also, due to the butterfly computation involved in NTT, converting the twiddle factors into a matrix is significantly more complex than converting a polynomial into a matrix for Conv1D [12].

The end-to-end computational complexity of NTT-based PMM on XBAs is actively higher than directly mapping Conv1D into XBAs. As depicted in Fig. 1(a), NTT-based PMM involves three main steps: NTT computation  $(O(n \log n) \text{ complexity})$ , element-wise multiplication  $(O(n) \cos n) \text{ complexity})$ , and INTT computation  $(O(n \log n) \text{ complexity})$ . In contrast, Conv1D-based PMM has a complexity of  $O(n^2)$ . However, when utilizing XBA acceleration, the complexity of Conv1D-based PMM can be reduced from  $O(n^2)$  to O(1). By employing similar data mappings, NTT and Conv1D exhibit the same time complexity on XBA. Therefore, Conv1D-based PMM on XBA demonstrates a lower end-to-end complexity compared to NTT-based PMM, as it requires fewer operations—Conv1D only necessitates O(1) operations, while NTT involves O(1) + O(n) + O(1) operations.

## B. Performance Analysis

NTT-based PMM requires that the twiddle factors be stored for NTT and INTT in the XBAs (See Fig 1(c)). The stored twiddle factors approach necessitates either frequent updates to the twiddle factors stored in the XBAs or the use of additional XBAs to store all twiddle factors needed for NTT. As a result, this leads to either higher latency and energy consumption or increased area. Alternatively, Conv1D-based PMM has numerous identical values that, when stored in XBAs, can be reused repeatedly. This provides the opportunity to devise intelligent data reuse schemes (see Sec. IV-C), ultimately leading to more efficient and optimized solutions in terms of area and energy consumption. Therefore, Conv1D-based PMM can be a more promising method for accelerating PMM with XBAs.



Fig. 3. Hierarchical structure of the proposed X-Poly design: (1) Tile level design and data mapping, (2) PE level design and data mapping, and (3) XBA structure.

# C. Noise

As discussed in Sec II-D, XBAs are susceptible to accuracy degradation stemming from the intrinsic nonidealities of the memory cells, and the limitation of ADC precision. As a result, using XBAs inevitably introduces a certain amount of noise (i.e., error) in VMM results. When implemented on XBAs, Conv1D-based PMM incurs less noise than NTT-based PMM. The primary reason is that in Conv1D-based PMM, the entire computation can be completed in one step in XBAs, which helps control the magnitude of the noise. However, in NTT-based PMM, the NTT, element-wise multiplication, and INTT must be performed, which increases the noise introduced by XBAs multiplicatively (See Fig 1(a)). In applications such as HE, higher noise levels are not tolerable, making NTT-based XBA PMM unsuitable for such applications.

Based on the observations in this section, we believe that Conv1D-based PMM is a better approach for accelerating PMM with XBAs. We thus focus on the design and optimization of the XBA fabric to accelerate Conv1D-based PMM.

### IV. X-POLY

Design and optimization of Conv1D-based PMM on XBAs for long polynomials must solve several key problems. These include mapping data to XBAs to efficiently use the resources, enhancing memory utilization at the Processing Element (PE) level, and effectively implementing modular reduction strategies. We present X-Poly for accelerating the Conv1D-based PMM and provide tailored solutions to address the aforementioned challenges.

## A. Overview

The high-bitwidth long polynomials employed in cryptographic algorithms like HE propose challenges for the design of XBA-based architecture. One specific issue relates to the limited size of the XBA. For instance, an array with 128 rows and 128 columns falls short in accommodating high-bitwidth polynomials with a degree exceeding 256.

To address the challenge, X-Poly utilizes a hierarchical approach to address computational complexity. Fig. 3 illustrates the overall structure and data mapping of X-Poly, consisting of the tile, PEs, and XBAs. The tile (Fig. 3(1)) contains multiple PEs, an accumulator, and a specifically designed reduction unit for modular reduction. Each PE holds one-bit weights and shares the same input. Thus, k PEs can store k-bit polynomials from the most significant bit (MSB) to the least significant bit (LSB), working in parallel.

The PE (Fig. 3(2)) is composed of multiple XBAs working on different parts of the polynomials simultaneously, as well as an adder tree and a shifter. The XBAs (Fig. 3(3)) are used for coefficient multiplication, while the adder tree and shifter within each PE accumulate partial results from each XBA and perform shift-add operations.

## B. Bit Mapping

The high bitwidth and large polynomial degree required for cryptographic applications need a large number of shiftadd operations, which may not be efficiently supported in a CIM architecture. Due to the limited precision of a memory cell in an XBA, we need to map the bits of weight into multiple memory cells. Fig. 4(a) illustrates the conventional approach for mapping the high bitwidth weight to multiple XBAs. All bits of weight are stored in multiple columns of the XBA. When input arrives at the XBA, each column conducts a multiplication operation. Immediately following this, shift-adders carry out the shift-add operations after the XBA computation. This XBA-level shift-add operation requires lots of shift-adders and is expensive in terms of both time and energy.

As such, in this work, we propose a new bit mapping (BM) technique that groups the same bit of all weights together, as shown in Fig. 4(b). For example, in the case of 4x4 2-bit weights distributed among 2 PEs (4 XBAs per PE), each PE process one bit of each weight. After all PEs process one input bit, the shift operation is performed at the PE level, thereby avoiding a costly array-level shift-add operation. Comparing the conventional mapping (Fig. 4(a)) and the bit mapping (Fig. 4(b)) in the example, the number of shift-adders is reduced from 8 to 2.

As will be seen, this bit mapping strategy can significantly improve both the area and speed for processing high-bitwidth polynomial-based workloads in XBAs. In addition to its benefits for shift operations, the BM technique also simplifies the design of the PE. Since each PE handles a bit of each



Fig. 4. Example of the proposed bit mapping technique: mapping 2bit 4x4 weights to 2x2 XBA with binary cells: (a) Conventional mapping. (b) Bit mapping.

polynomial, the data patterns are captured at the polynomial coefficient level. We can simultaneously perform mapping optimization for all PEs. Thus, this technique can be easily extended to accommodate polynomials with different degrees or bitwidths, making it a flexible solution for performing polynomial operations in XBAs.

#### C. Polynomial Mapping

In our PMM approach (utilizing VMM in XBAs), we first map polynomials into matrices to facilitate computation. Each polynomial is converted into a matrix by horizontally shifting the coefficients of the polynomial across each row, with any remaining gaps filled with zeros. This procedure results in a matrix structure that supports the critical shift-add operations intrinsic to PMM.

Mapping the matrices into XBAs in our PMM approach using VMM is straightforward. However, in an effort to further optimize this mapping scheme, we noted that for any given polynomial degree n and XBA row length x, there is a consistent pattern of repeated XBAs. Specifically, in every instance, we require n/x identical XBAs to represent the polynomial matrix.

This aspect of our design stands in contrast with NTTbased XBA designs [12], which often find themselves confined to specific polynomial parameter settings. As such, X-Poly offers a significant increase in flexibility. For example, consider two application scenarios for privacy-preserving machine learning (PPML) inference as shown in [24]. On server-side inference, where performance is prioritized, and energy or area constraints are less critical, X-Poly can leverage a larger count of XBAs for high-throughput PMM in HE of PPML. For edge-device inference, where area and energy efficiency are paramount, X-Poly can efficiently handle a variety of large polynomial degrees and bitwidths with a smaller number of XBAs. A detailed study of the scalability of our design, referred to as X-Poly, is provided in Sec. V-E.

#### D. Modular Reduction

Modular reduction is a crucial step in PMM, which ensures that the resulting polynomial remains within a specified degree and coefficient bounds. The essential steps in the reduction process include selecting an appropriate modulus for the ring and performing the modulo operation on the degree and coefficients of the resulting polynomial.

In X-Poly, we utilize a variant of the Barrett reduction [33] technique for efficient modular reduction. This method is known for its effectiveness in cryptographic applications and modular arithmetic, as it can compute the remainder of a division operation without performing the division itself. No-tably, to minimize computation overhead in reduction, we strategically pre-compute specific parameters. This strategy transforms the complex, time-consuming multiplication and division operations into shift operations, effectively reducing computation time and optimizing the overall reduction process.

#### E. Computation Flow

Assuming polynomial A is mapped onto XBAs in X-Poly, PMM can be accomplished as follows. (1) **Input processing**: We begin by bit-slicing each element in the new polynomial B, separating it into its individual bits. (2) **PE computation**: Within each PE, different arrays handle distinct sections of the polynomial and perform multiplications with corresponding sections of the input. The results are then summed and shifted at the PE level. This bit-by-bit input process continues until all input bits have been addressed. (3) **Tile accumulation**: Afterward, the results from all PEs are accumulated at the tile level, and the partial results obtained from each PE are combined. (4) **Tile reduction**: Finally, a tile-level reduction operation is applied for efficient modular reduction.

We also prioritize maximizing throughput in our design by incorporating a three-stage pipeline into the X-Poly workflow to enhance the PMM process. This pipeline, which encompasses the PE computation, tile accumulation, and tile reduction stages, enables efficient synchronization and overlapping operations.

# V. EVALUATION

In this section, we present the evaluation of X-Poly. We begin by discussing our implementation setup and evaluation tools and follow with a comparison with both the CPU-based solutions as well as other hardware accelerators. We will quantitatively assess the performance benefits from X-Poly. We then evaluate our bit mapping technique, with a focus on energy and area savings. Then we study the throughput per area performance of X-Poly, demonstrating its superior performance over other SOTA CIM accelerators. Finally, we assess the scalability of X-Poly and highlight its versatility in handling diverse polynomial degrees and bitwidths.

## A. Implementation Setup

To verify the functionality of X-Poly and evaluate performance characteristics such as latency, energy, and area, we have assembled a comprehensive evaluation framework.

This framework considers the simulation of hardware components, including the modular reduction unit, shift-adders, accumulators and XBA arrays. We implemented the reduction unit, shift-adder, and accumulator using RTL, coded in Verilog and evaluated the energy consumption and area of these components using the RTL synthesis tool Cadence Encounter, paired with the 45nm CMOS predictive technology model (PTM) [34]. We used Neurosim [35] to estimate the latency, energy, and area of the ReRAM-based XBAs, as well as successive-approximation-register (SAR) ADCs assuming the same 45nm technology node. The size of each XBA is 128 rows  $\times$  128 columns and one ADC is shared by 8 columns.

We then incorporated the aftermentioned simulation-based results into our Python-based cycle-accurate simulator. This simulator tracks the pipeline stages for a given PMM operation and computes the cycle count and total energy consumption by emulating the operations of each hardware component on a cycle-by-cycle basis. This evaluation framework allows us to generate a holistic and precise assessment of the overall performance of a PMM in X-Poly.

## B. Comparison with SOTA Solutions

1) Comparison with CPU: We first compared our X-Poly implementation with a CPU implementation that performs PMM with a SOTA C++ library (Number Theory Library version 11.5.1 [36]). An Intel(R) Xeon(R) CPU E5-2680 v3 operating at 2.50GHz was used for the CPU implementation. The results are shown in Table I (col 3). The latency of the X-Poly design is  $200 \times$  better than the CPU implementation. Performance enhancement is primarily due to the parallel compute capability and fast multiplication inherent in the XBAs in our CIM-based architecture, allowing for a much more efficient PMM execution.

2) Comparison with other accelerators: Next, we compared X-Poly with other SOTA accelerators. As current accelerators for PMM only use NTT, we compare our approach to SOTA accelerators that support NTT given a polynomial degree of 256. That said, NTT solutions require additional multiplications and the INTT to obtain final PMM results. Compared to X-Poly, this may increase overall latency and energy consumption by  $2\times$ . Moreover, with X-Poly, we can generate PMM results in a single step without the need for additional multiplication or INTT.

**XBA solutions:** We first compared our implementation with other CIM solutions, specifically with ReRAM implementations. We scaled the latency and energy of [12] to 45nm for a fair comparison to X-Poly, following the methodology outlined in [13]. Given that the study in [12] did not provide area results, we carried out an estimation using the mapping methodology introduced in their publication. We assume the same area for XBAs and peripheral components as X-Poly. Although our design exhibited similar latency to RMNTT, our improved mapping technique results in a significantly reduced area. That is mainly because we reduce the footprint of shift-adders to just 20% of the original area by using the proposed BM technique, thereby leading to a  $3.9 \times$  improvement in the throughput-per-area ratio.

**Compute in SRAM solutions:** We also compared our implementation with in-SRAM solutions. The X-Poly approach also improves throughput and throughput-per-area. Again, this can be attributed to both the parallel computing capability and the fast multiplication feature of our XBA-type mapping technique, which enables us to perform multiple computations simultaneously. More specifically, throughput is improved by  $11 \times$ , and throughput-per-area is improved by up to  $3 \times$ .

**Non-CIM solutions:** Finally, we compared X-Poly with non-CIM solutions. The X-Poly design is advantageous as it can store entire polynomial coefficients inside the XBAs. This feature eliminated the need for frequent access to on-chip memory for coefficients in long polynomials, which reduces data movement between the computing unit and the on-chip memory. This results in a reduction in both latency and energy consumption. Overall, X-Poly outperformed ASIC and FPGA solutions in terms of throughput and energy efficiency. Compared to SOTA FPGA implementations, X-Poly can achieve a remarkable 75× throughput improvement. When compared against SOTA ASIC implementations, X-Poly can achieve a  $2\times$  throughput improvement.



Fig. 5. Comparison of area and energy breakdown for ADCs and shift-adders in X-Poly and RMNTT [12].

## C. Bit Mapping Study

We now evaluate the energy and area benefits of the proposed BM technique, discussed in Sec.IV. To evaluate performance, we consider two scenarios: (1) conventional mapping as the implementation of RMNTT, the SOTA XBA-based NTT accelerator, and (2) our proposed BM technique. Fig.5 illustrates the shift-adder area/energy and ADC area/energy given various polynomial degrees for each mapping. Results suggest that due to the large polynomial degrees and high bitwidths associated with the PMM, the peripherals (such as the shift-adders) in the design with conventional mapping consume a significant proportion of the energy and area. Moreover, this escalates with polynomial degrees. However, our proposed BM technique decreases the area for shift-add operations by 80%, leading to an additional  $3 \times$  reduction in overall area. Moreover, compared to conventional mapping, our design has lower latency and energy consumption.

Fig. 6 illustrates the area and energy breakdown of our proposed design. This analysis further reveals that the majority of the energy consumption and area is spent on ADC operations, with the proposed mapping technique reducing the energy and area consumption for other peripherals significantly.

	PMM Solutions		NTT Solutions (CIM)				NTT Solutions (Non-CIM)		
Design	X-Poly	CPU	RMNTT	BPNTT	MENTT	CryptoPIM	FPGA	LEIA	Sapphire
Device	ReRAM	CMOS	ReRAM	SRAM	SRAM	ReRAM	CMOS	CMOS	CMOS
Frequency (MHz)	400	2.5k	400	3.8K	218	909	164	267	64
Bit width	16	16	14	16	14	16	16	14	14
Area $(mm^2)$	0.27	-	0.76*	0.063	0.173	0.152	-	1.77	0.354
Latency $(us)$	0.32	56	0.44	61.9	15.9	68.7	24.3	0.6	20.1
Energy $(nJ)$	308.07	-	429.91	69.4	47.8	2.6k	3.1k	44.1	236.3
Throughput\$ (KOP $/s$ )	3.1k	-	2.2k	258.6	62.8	553.3	41.2	1.7k	49.7
Throughput/Area $(KOP/s/mm^2)$	11.4k	-	2.9k	4.1k	364	3.6k	-	940.6	140.1

 TABLE I

 Comparison between X-Poly and other SOTA solutions on a 256-point polynomial. Technology size: 45nm

\* We estimate the area for RMNTT based on the information reported in the paper. We utilize the same XBA area and peripheral components as X-Poly for the sake of comparison.

\$ We evaluate the throughput based on the type of operations performed in the corresponding accelerators. We report the throughput of PMM for both X-Poly and CPU as well as the throughput of NTT for other accelerators as reported in the literature.



Fig. 6. Area and energy breakdown for components of X-Poly with polynomial degree 256 and bitwidth 16.



Fig. 7. Throughput per Area (KOP/s/mm2) comparison with the SOTA CIM solutions (RMNTT and BPNTT) under different polynomial degrees and bitwidths. Y-axis is using log-scale for better illustration.

# D. Throughput per Area Study

Table I shows that the XBA-based solutions (X-Poly and [12]) achieve higher throughput but require a larger area than the in-SRAM solution [13]. This is due to the inherent design of XBA-based solutions: they require a more expansive area to accommodate an increase in both polynomial degree and bitwidth [12]. In-SRAM solutions can support larger parameter sizes within a similar area. However, this is accompanied by a substantial reduction in throughput. However, X-Poly reduces XBA area while maintaining its high throughput.

To further understand the trade-off between throughput and area, we conducted an analysis of the throughput per area performance and compare the results with other SOTA CIM solutions. We consider a range of polynomial degrees and bitwidths, to generate a comprehensive perspective regarding the strengths of our design.

Fig. 7 illustrates the throughput per area performance of our design, as well as the SOTA XBA design in [12] and the in-SRAM design in [13]. Our results show that X-Poly can achieve significantly better throughput-per-area performance than both of these solutions, even as the parameter size increases. This highlights how X-Poly can lead to decreased area consumption of the XBA-based solution without compromising the throughput.

## E. Scalibility of X-Poly

Modern applications like HE in privacy-preserving machine learning often choose polynomials with a large degree and bitwidth [7], [24]. Storing these entirely within XBAs demands



Fig. 8. Scalibility study shows the throughput of X-Poly under different polynomial degrees and bitwidths given a fixed total XBA number.

a high number of arrays, leading to significant area usage and energy consumption.

Our polynomial mapping scheme (Sec IV-C) allows us to reuse arrays. This enables us to employ a smaller number of XBAs to accommodate larger polynomials. However, reusing XBAs could potentially affect our design's latency. To address this, we conducted an experiment where given a fixed number of XBA arrays, we assessed the capability of X-Poly to adapt to various polynomial degrees and bitwidths. The objective here was to determine how we could optimize X-Poly to maximize design throughput under different polynomial degrees and bitwidths constraints.

The left graph in Fig. 8 depicts the maximum throughput of X-Poly using different numbers of XBAs. We considered polynomial degrees ranging from 256 to 2048, with a fixed bitwidth of 16. The right graph demonstrates the maximum throughput for different bitwidths ranging from 8 to 64, while maintaining a constant polynomial degree of 512. Our experiments highlight that our design is capable of managing a wide array of polynomial degrees and bitwidths while maintaining a fixed number of XBAs. As anticipated, higher degrees and bitwidths require longer computation times due to the necessity for reuse of the same arrays within the pipeline. By modifying the number of XBAs, we can manage the balance between area and throughput. Overall, our design showcases robust scalability, effectively adapting to a broad spectrum of polynomial degrees and bitwidths.

# VI. CONCLUSION

In summary, this paper proposes a novel PMM accelerator based on XBA-type CIM for accelerating the most timeconsuming part of lattice-based cryptography algorithms. The proposed X-Poly design achieves 3.1 MOP/s throughput and offers  $200 \times$  latency improvement compared to CPU-based implementations. It also achieves  $3.9 \times$  throughput per area improvements compared with the SOTA CIM accelerators. The suitability of NTT-based solutions for CIM-based PMM acceleration is evaluated, and a novel bit mapping technique is proposed to reduce area and energy overhead. PE-level optimization is conducted to increase memory utilization and support different scales of problems with a fixed number of XBAs.

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