

FuNToM: Functional Modeling of RF Circuits Using a Neural Network Assisted Two-Port Analysis Method

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Abstract—Automatic synthesis of analog and Radio Frequency (RF) circuits is a trending approach that requires an efficient circuit modeling method. This is due to the expensive cost of running a large number of simulations at each synthesis cycle. Artificial intelligence methods are promising approaches for circuit modeling due to their speed and relative accuracy. However, existing approaches require a large amount of training data, which is still collected using simulation runs. In addition, such approaches collect a whole separate dataset for each circuit topology even if a single element is added or removed. These matters are only exacerbated by the need for post-layout modeling simulations, which take even longer. To alleviate these drawbacks, in this paper, we present FuNToM, a functional modeling method for RF circuits. FuNToM leverages the two-port analysis method for modeling multiple topologies using a single main dataset and multiple small datasets. It also leverages neural networks which have shown promising results in predicting the behavior of circuits. Our results show that for multiple RF circuits, in comparison to the state-of-the-art works, while maintaining the same accuracy, the required training data is reduced by 2.8x - 10.9x. In addition, FuNToM needs 176.8x - 188.6x less time for collecting the training set in post-layout modeling.

Index Terms—Functional modeling, RF circuits, two-port analysis, neural network, post-layout.

I. INTRODUCTION

The growing demand for analog and Radio Frequency (RF) circuits, due to their broad applications, has led to a crucial need for automated circuit synthesis [1]. There are two classical automated synthesis approaches for analog and RF circuits, *i.e.* simulation- and model-based, which both need a circuit modeling tool. In the simulation-based approaches, the circuit modeling tool is invoked multiple times to evaluate the circuit and generate new parameter candidates to meet the desired specifications [2]. In addition, the modeling tool is used to generate the training set of the model-based approaches. Since both methods invoke the modeling tool frequently (especially the simulation-based), using the common modeling tool, *i.e.* SPICE simulation, is drastically time-consuming. Furthermore, technology scaling has caused much longer run times in both schematic and post-layout simulations [3].

Artificial Intelligence (AI) methods are an alternative to SPICE because of their speed and relative accuracy [4]. However, current approaches require a large amount of training data, which are still collected using simulation runs. So, they face the same time-consuming problem during training.

Bayesian Model Fusion (BMF) is one of the common analog circuits functional modeling methods [5]–[7]. Neural Networks (NNs) also have shown promising results in all circuit design levels such as single-board computer, sizing, layout, System-on-Chip (SoC) design, and performance modeling [8], [9], [11]–[13].

Despite all these advances in functional modeling of circuits, current works [2], [5]–[7], [13]–[17] train directly from circuit design parameters (capacitance value of capacitors, size of transistors, etc.) to Performance of Interests (PoI). Therefore, such conventional modeling approaches require a unique training set for each topology, because design parameters change if the topology changes. This means their whole training process needs to be redone even if a single element is added or removed from the circuit. Moreover, they assign an individual feature to each design parameter, which makes their models high-dimensional for modern complex analog and RF circuits. The matter is only exacerbated by the post-layout modeling, where collecting data takes longer.

To combat all the aforementioned challenges in circuit functional modeling, we propose an NN-assisted two-port analysis-based method, FuNToM. The goals of FuNToM are threefold: (a) decreasing the required number of new training sets after modifying a circuit topology; (b) further reducing the number of training sets for each topology; (c) achieving a fast, accurate RF functional modeling method.

In order to decrease the required number of new training sets after modifying a circuit topology, we propose a method to properly model multiple topologies while using a single main dataset and multiple small datasets. For this purpose, we divide the circuit into multiple Electrical-networks (E-networks) and analyze them modularly via NNs. An E-network is a collection of electrical components, *e.g.* capacitors, resistors, etc., that are interconnected [18]. To modularly analyze E-networks, we leverage the Scattering parameters (S-parameters) concept. The S-parameter is a well-known powerful concept in RF circuits that is defined using two-port analysis and describes the circuit behavior of E-networks. In other words, in two-port analysis, the S-parameter is a 2×2 matrix that summarizes the circuit behavior of the associated E-network, such as input/output return losses, and insertion loss/gain [19]. Therefore, the S-parameter can be replaced with the associated E-network in the circuit analysis.

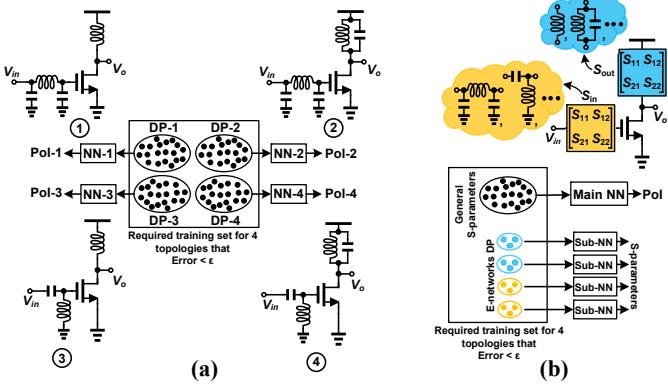


Fig. 1. An overview, concept, and the impact on the training set of (a) the conventional analog and RF circuits functional modeling method vs (b) the proposed modular S-parameters-based approach. The conventional method needs a whole separate dataset and model for each circuit topology while the proposed approach works properly for many circuit topologies with a single general format E-networks' S-parameters dataset.

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}: \text{S-parameter matrix.}$$

DP: Design parameters.

The main advantage of modularly modeling the circuit is its generality. In our case, by passing the S-parameters to the NN, the NN learns the relationships between the general format of E-networks' S-parameters and the PoI. Since the S-parameter works as a wrapper around the E-networks, the NN accurately determines the functionality of the circuit with any E-networks' topology. In other words, training via S-parameters is a one-time process which works properly for many circuit topologies because of its modularity.

There are two types of NN models in our approach: 1) One main circuit NN for determining the PoI using S-parameters of E-networks; 2) multiple sub-NNs that each determines the S-parameters of the associated E-network using the circuit design parameters within such E-network. Creating new datasets for sub-NNs is the only required modification in the dataset of the proposed approach when the circuit topology changes as the training set of the main NN works for all topologies. However, since the circuit is divided into multiple E-networks and each E-network has a separate dataset, the size of such datasets is small because each deals with only a few design parameters. This dividing of the circuit is another advantage of the proposed method that is especially prevalent when going from schematic to the post-layout modeling. Instead of collecting a new large dataset by running time-consuming post-layout simulations for the whole circuit with many design parameters, it is only needed to gather small datasets for the E-networks, each with only a few design parameters. Fig. 1(a) demonstrates the conventional modeling method using NNs, while Fig. 1(b) shows the big picture of the proposed approach. As it is shown, our approach requires much less training data than the conventional method to have the same accuracy in modeling of four different topologies. Note that the circuit elements (design parameters) that are not part of E-networks,

e.g. the transistor in Fig. 1(b), are also considered in our proposed model as explained with more details in Section III-A. FuNToM supports all RF circuits, including active and passive components, as multiple of them are evaluated in Section IV.

We use the Circuit-Connectivity-Inspired-NN (CCI-NN) structure [2] in our main model to further reduce the number of training sets for each topology. As stated by Hassanpourghadi *et al.* [2], CCI-NN structure requires less training data in comparison with the Fully-Connected NNs (FC-NNs). Moreover, by condensing the design parameters using S-parameters, we may have a smaller design space than the conventional approach. If the number of design parameters in each E-network is more than the indexes in the S-parameter matrix, the NN model of the proposed approach will have fewer features than the conventional method and hence, less training sets will be required to have the same accuracy. This mainly has an impact on large circuits.

To validate our proposed method, FuNToM is tested by modeling the functionality of multiple phase shifters at the schematic level as well as multiple two-stage Low-Noise-Amplifiers (LNAs) at both schematic and post-layout levels. Our results show that using FuNToM, the required training set is reduced by a factor of 2.8x - 10.9x while maintaining the same accuracy in comparison to the state-of-the-art works. Also, the time for collecting the training set in the post-layout modeling using FuNToM is 176.8x - 188.6x faster. The results illustrate that FuNToM achieves an average R2-score of 0.95 when tested on 3,200 samples.

The main contributions of this paper can be summarized as follows:

- Proposing FuNToM, an efficient RF functional modeling method which achieves an average R2-score of 0.95 when it is tested on 3,200 samples with different topologies and specifications.
- Reducing the number of required training set points compared to the state-of-the-art works by 2.8x - 10.9x by using two-port analysis and dividing the circuit into multiple E-networks.
- Decreasing the time for collecting the training set in the post-layout modeling by 176.8x - 188.6x compared to state-of-the-art works.

II. BACKGROUND & RELATED WORK

A. Analog and RF Circuits Functional Modeling

The goal in analog and RF circuits functional modeling is to approximate a PoI vector (y) of a given circuit by a function (\hat{f}) of the design parameters vector (x), while the modeling error (e) is minimized. For this purpose, the SPICE is invoked as the ground truth function (f). In other words,

$$y = f(x, t) \quad (1)$$

$$\left\{ \begin{array}{l} y = \hat{f}(x, t) + e, \\ \text{subject to: minimize } e. \end{array} \right.$$

Note that t is used to account for time/frequency variant PoIs. Power gain is an example of a PoI for an LNA, while resistance values of resistors are examples of the design parameters

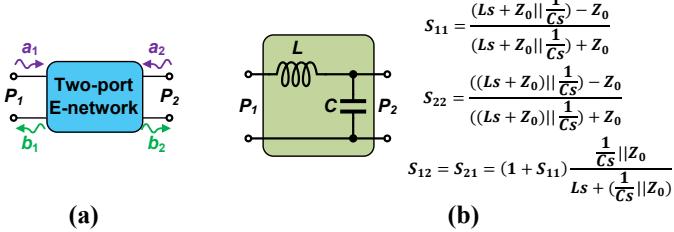


Fig. 2. (a) Excited and incident waves in a two-port E-network which are used for calculating S-parameters. (b) An example of a simple L-C network with the calculated S-parameters. $s = j2\pi f$ where f is the frequency. Z_0 is the reference impedance (the impedance of excitation ports) which equals to 50Ω in most cases.

vector. The advantage of the functional modeling methods over SPICE is that once they get trained, they can determine the functionality of circuits, even when the design parameters change, in near zero time. This is because the circuit behavior is stored as weights for the functional modeling methods.

For minimizing the modeling error, different models, such as posynomials regression, genetic programming, BMF, and NN, have been studied [5], [13]–[15]. The fusion in BMF means passing information (prior knowledge) from the schematic model to the post-layout model to reduce the expensive post-layout performance modeling cost [1]. This passed information is then combined with a few post-layout training data points to solve the model coefficients via Bayesian inference [20].

The other goal of the functional modeling methods is to minimize the number of times that SPICE is invoked since it is time-consuming. Several studies have attempted to reduce the number of training samples while maintaining the same error, such as sparse regression, Co-Learning BMF (CL-BMF), hierarchical CL-BMF, and Circuit-Connectivity-Inspired NN (CCI-NN) [2], [16], [17]. In hierarchical Co-Learning BMF, the circuit is partitioned into multiple stages and CL-BMF is applied to each stage [17]. In this regard, they consider lower dimensional models and as a result the training set size is decreased. Among all aforementioned works, NNs have shown the lowest modeling error however, they need a large training set [2]. Similar to [17], Hassanpourghadi *et al.* [2] break down a circuit into multiple stages, but they apply NN instead of CL-BMF for modeling. Zhao *et al.* [21] first, model the transistor using NNs. By leveraging such a model, they perform DC and AC modeling for the circuit. Despite of the accuracy and efficiency, there is no word about the post-layout modeling.

B. Two-port Analysis & S-parameters

The two-port analysis is used to determine the response of a two-port E-network against the applied signals to its terminals. The circuit behavior of E-networks is determined using two-port analysis [19]. Using two-port analysis, an S-parameter matrix is derived which is used for characterizing circuits. Fig. 2 shows the procedure of determining S-parameters for a two-port E-network: each port is excited by incident waves, a_1 and a_2 , and the reflected voltage waves, b_1 and b_2 , are

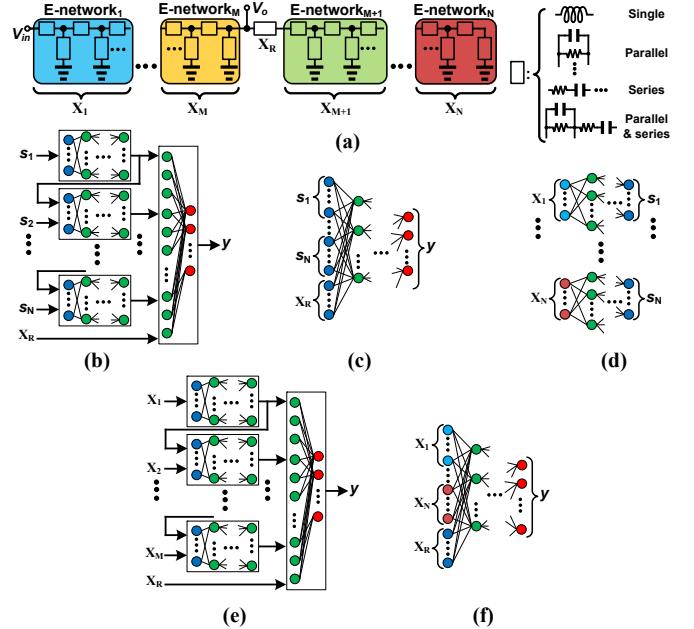


Fig. 3. (a) General circuit division into E-networks. Each rectangle is either a single element, parallel/series of elements, or a combination of parallel and series elements. (b) Main NN in the proposed approach for determining the PoI from S-parameters of E-networks (Equation (4a)) with CCI-NN structure. (c) Main NN in the proposed approach for determining the PoI from S-parameters of E-networks (Equation (4a)) with FC-NN structure. (d) Sub-NNs in the proposed approach for determining S-parameters from the design parameters of E-networks (Equation (4b)). (e) The original CCI-NN model structure [2] with the circuit design parameters as inputs. (f) The conventional FC-NN model in the analog and RF functional modeling with the circuit design parameters as inputs.
 s_i : S-parameters of the i^{th} E-network.
 x_i : Design parameters vector of the i^{th} E-network.
 x_R : A vector of the circuit's design parameters that are not included in any E-networks.

measured. The reflected voltage waves are a function of the incident waves:

$$\begin{aligned} b_1 &= S_{11}a_1 + S_{12}a_2, \\ b_2 &= S_{21}a_1 + S_{22}a_2, \end{aligned} \quad (2)$$

where $S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$ is called the S-parameter matrix.

S-parameters are calculated by setting a_1 and a_2 in Equation (2) to zero one by one and getting the ratios of the reflected waves over the incident waves as follows:

$$\begin{aligned} S_{11} &= \frac{b_1}{a_1}|_{a_2=0}, S_{12} = \frac{b_1}{a_2}|_{a_1=0}, \\ S_{21} &= \frac{b_2}{a_1}|_{a_2=0}, S_{22} = \frac{b_2}{a_2}|_{a_1=0}. \end{aligned} \quad (3)$$

It is noteworthy that setting $a_i = 0$ means that the i^{th} port is terminated with a Z_0 impedance so that the reflection from that port (a_i) becomes zero. Z_0 equals 50Ω in most cases. Fig. 2(b) demonstrates an example of S-parameters extraction of a simple L-C E-network. Based on the reciprocity theorem, $S_{12} = S_{21}$ for almost all passive E-networks such as the network mentioned in Fig. 2(b). Moreover, for the symmetric E-networks (see Fig. 6(b)), $S_{11} = S_{22}$.

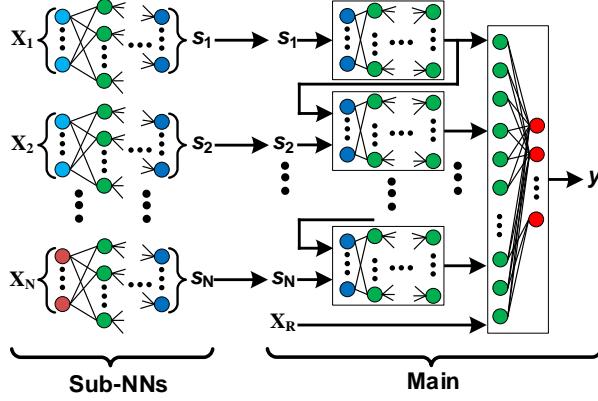


Fig. 4. Final FuNToM model by concatenating the sub-NNs and the main NN.

s_i : S-parameters of the i^{th} E-network.

x_i : Design parameters vector of the i^{th} E-network.

x_R : A vector of the circuit's design parameters that are not included in any E-networks.

III. PROPOSED APPROACH

A. Neural Network Models

Breaking down the top-level circuit into multiple stages is used for simplifying f in Equation (1) and decreasing the number of training sets [2]. In our approach, we have gone further and we break down the circuit into multiple E-networks. There are two types of models in our approach: 1) One main model for determining the PoI using S-parameters of E-networks and design parameters that are not included in any E-networks; 2) multiple sub-models that each determines the S-parameters of the associated E-network using the circuit design parameters within such E-network. In other words:

$$y = \hat{g}([s_1, \dots, s_N, x_R], t) + e_1, \quad (4a)$$

$$s_i = \hat{h}_i(x_i, t) + e_{2,i} \quad i = 1, \dots, N, \quad (4b)$$

where s_i and x_i are the S-parameters and design parameters vector of the i^{th} E-network ($s_i = [S_{11,i}, \dots, S_{22,i}]$), respectively assuming there are N E-networks. Indeed, x_i represents the value of circuit elements *e.g.* capacitors, inductors, etc., inside the i^{th} E-network. x_R is a vector of the circuit's design parameters that are not included in any E-networks *e.g.* the transistor in Fig. 1(b).

Fig. 3(a) shows a general circuit division into multiple E-networks while Fig. 3(b) and (c) illustrate two structures for our proposed main NN model. Both of them depict the NN representation of Equation (4a). Fig. 3(b) and Fig. 3(c) have CCI-NN and FC-NN structures, respectively. As it is shown, the CCI-NN structure [2] breaks a giant NN into smaller chunks while considering the sequential paths and concatenating all at a final 1-layer NN. It should be mentioned that the CCI-NN is trained with the same dataset as the FC-NN *i.e.* $[(s_1, \dots, s_N, x_R); y]$. We analyze both FC-NN and CCI-NN structures for our main NN and select the one which gives the best results. As stated by [2], CCI-NN requires less

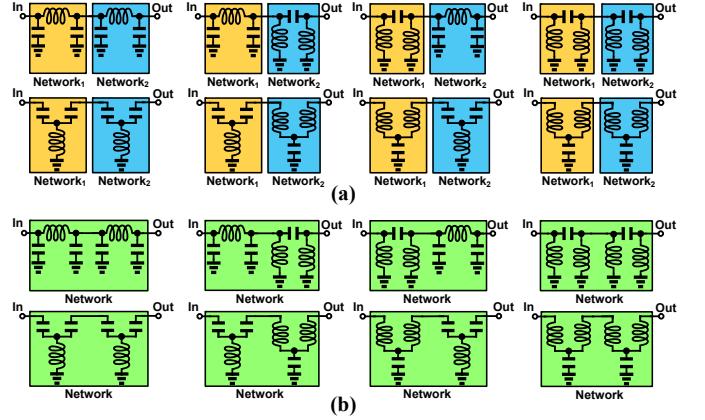


Fig. 5. Different ways for partitioning 8 topologies. (a) First scenario: each is divided into two E-networks. (b) Second scenario: there is only one E-network.

TABLE I
REQUIRED NUMBER OF TRAINING DATA COMPARISON BETWEEN TWO SCENARIOS OF FIG. 5 FOR THE MAIN NN, SUB-NNs, AND TOTAL.

Scenario	Main NN	Sub-NNs	Total
First scenario (Fig. 5(a))	1,800	400	2,200
Second scenario (Fig. 5(b))	450	3,200	3,650

training data. Fig. 3(d) depicts our sub-NN structures which are representations of Equation (4b).

Our approach can be summarized as follows. The E-networks are identified and we assign a sub-NN to each. Then, the design parameters of each E-network are fed as inputs to the corresponding sub-NN for determining their S-parameters. In parallel, general S-parameters of E-networks are fed as an input to the main NN to determine the PoI. By combining these models (Equations ((4a)) and (4b), *i.e.* $\hat{g}([\hat{h}_1(x_1, t), \dots, \hat{h}_N(x_N, t), x_R], t)$), the PoI is determined based on the circuit design parameters. It should be noted that \hat{g} in Equation (4a) is a function of s_1, \dots, s_N in general, not specifically for the s_i in Equation (4b). In other words, Equation (4a) finds the relationship between the PoI and general S-parameters, and in parallel Equation (4b) maps the design parameters to S-parameters in the desired circuit.

Equation (4a) is independent of the design parameters of E-networks. Therefore, it does not change if E-networks change, proving the generality and re-usability of our model for different E-networks. Furthermore, since each of the sub-NNs (Equation (4b)) takes a subset of design parameters as inputs, they are simpler than the conventional NN model (Fig. 3(e)). This significantly eases the collection of datasets for sub-NNs if E-networks change or during the post-layout modeling. Moreover, even in analyzing one specific circuit (without considering different E-networks), \hat{g} may be simpler than \hat{f} as S-parameters condense design parameters. This attribute is more pronounced in large RF circuits with many design parameters in each E-network. In addition, as mentioned in

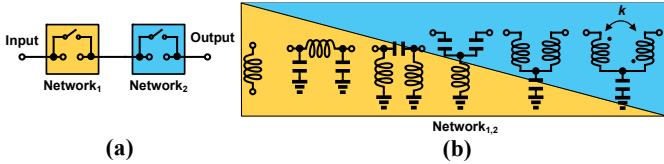


Fig. 6. Phase shifters tested on FuNTOM. (a) General structure. (b) Network₁ and network₂ topologies.

TABLE II
STATISTICS OF PERFORMANCE OF INTERESTS FOR PHASE SHIFTERS.

Specification	Min	Max	Average	SD
Input return loss [dB]	-117	0	-4.87	-10.12
Insertion loss [dB]	-133	0	-3.17	-10.26
Insertion phase [degree°]	-180	180	-23.02	84.5
Output return loss [dB]	-117	0	-4.87	-10.12

Section II-B, $S_{12} = S_{21}$ for almost all passive E-networks and $S_{11} = S_{22}$ for the symmetric ones. These cause having even simpler \hat{g} . So, in such cases, the required training set is further reduced compared to the conventional method.

To summarize, in our proposed approach by concatenating the sub-NNs and the main NN, we determine the PoI by getting the circuit design parameters as inputs as shown in Fig. 4. As illustrated, sub-NNs determine the S-parameters of the associated E-network by getting the circuit design parameters within such E-network as inputs while the main NN determines the PoI by getting S-parameters of E-networks as inputs. Two structures (CCI-NN in Fig. 3(b) and FC-NN in Fig. 3(c)) are analyzed for the main NN. As explained and our evaluations show, the CCI-NN structure gives the best results. The original CCI-NN structure proposed by [2] is shown in Fig. 3(e) where the circuit design parameters are given as inputs and the PoI is the output. The conventional FC-NN model in the analog and RF functional modeling is also illustrated in Fig. 3(f).

B. Circuit Partitioning into E-networks

There are multiple ways for partitioning a circuit into E-networks that each has some pros and cons. With decreasing the number of E-networks, the number of circuit elements at each increases as the total number of circuit elements is constant. So, the number of sub-NNs decreases while each gets more complicated. Usually, the required number of training data for a big complicated NN is more than the training data of multiple simple NNs. Moreover, with decreasing the number of E-networks, there would be fewer chunks in the CCI-NN structure of the main NN and since the input number of each chunk ($s_i = [S_{11,i}, \dots, S_{22,i}]$) is almost fixed, the width of the main NN intuitively reduces. However, in order not to lose the accuracy, it may get deeper.

Similar to all machine learning techniques, to find the best results, different scenarios need to be tested. As an example to show different ways for partitioning a circuit, we consider

TABLE III
AVERAGE R2-SCORE OF FUNTOM MODELS TESTED ON DIFFERENT SPECIFICATIONS OF PHASE SHIFTERS SHOWN IN FIG. 6.

Model	Sub-NNs	main NN				
		Input return loss	Insertion loss	Insertion phase	Output return loss	
R2-score		0.967	0.995	0.989	0.941	0.997

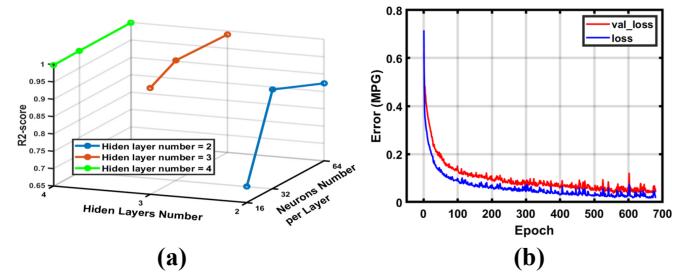


Fig. 7. Main model results for phase shifters. (a) R2-score comparison with different hyperparameters used for training. Three hidden layers with 32 neurons at each layer is the simplest model that gives a high R2-score of 0.99. (b) Loss vs. epoch diagram while three hidden layers with 32 neurons at each layer model is used for training.

two scenarios. To this end, we consider 8 different topologies. In the first scenario, each of these topologies is divided into two E-networks as shown in Fig. 5(a). In the second scenario, the whole circuit is considered as one E-network as illustrated in Fig. 5(b). Table I compares the required number of training data between these two scenarios for the main NN, sub-NNs, and total to have the same accuracy. As it is summarized, the first scenario (Fig. 5(a)) requires more data for the main NN while it needs less training data for sub-NNs and in total. Note that using such analysis and trying different scenarios, currently the circuit partitioning is done manually, but it can be replaced with an automated approach going forward.

IV. EVALUATION

In this section, we model the functionality of two different RF circuit types using FuNTOM and compare the results with the state-of-the-art modeling methods. We model multiple phase shifters at the schematic level, and multiple two-stage LNAs at both schematic and post-layout levels. The design parameters include all transistor widths as well as capacitor and inductor values. The inductors and capacitors are used from PDK models of 55nm BiCMOS library, *i.e.* quality factor and self-resonance of the inductors and capacitors are taken into account. All the SPICE simulations are run on a server with an NVIDIA TITAN V GPU and the frequency range for the simulations is 1 Hz-15 GHz. Also, all the NN models are built using the TensorFlow platform with the Adam optimizer and a learning rate of 0.001 and mean absolute error as the loss function. Moreover, all hidden layers have the RELU activation function. In order to avoid overfitting, the idea of early stopping [22] with the patience parameter of 125 is implemented. For this purpose, 10% of the data are used for validation during the training phase. In order to validate the

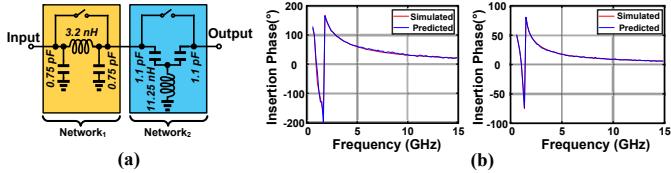


Fig. 8. An example of a phase shifter tested on FuNToM. (a) Topology. (b) The simulated (ground truth) and the predicted insertion phase by FuNToM over frequency. Left: when both switches are open; right: when both switches are closed.

TABLE IV

REQUIRED NUMBER OF TRAINING DATA, PER FREQUENCY, COMPARISON BETWEEN THE STATE-OF-THE-ART WORKS TO ACHIEVE AN AVERAGE R2-SCORE OF 0.95. ALL MODELS ARE TESTED ON 1600 DIFFERENT PHASE SHIFTERS WITH THE GENERAL STRUCTURE OF FIG. 6 IN 36 TOPOLOGIES.

Work	[13]	[2]	FuNToM FC-NN (Fig. 3(c))	FuNToM CCI-NN (Fig. 3(b))
Training data number	57,600	19,500	17,000	7,000

results properly, a random separate test set with the size of 10% of the training set is used. As a default, all the results of FuNToM are based on the CCI-NN structure for the main NN unless that is mentioned.

A. Phase Shifter

Fig. 6(a) depicts the general structure of the phase shifters tested on FuNToM. All combinations of E-networks shown in Fig. 6(b) are used for both networks_{1,2}. Therefore, in total, FuNToM is trained and tested on $6 \times 6 = 36$ different phase shifter topologies. There are on average 8 design parameters at each topology. The tested specification statistics are listed in Table II. In total, 6,600 and 400 simulations are performed for the training set of the main NN and sub-NNs, respectively, per frequency. Since most of the specifications change with frequency, different datasets are needed to properly model the specifications over the frequency.

The number of hidden layers and neurons per layer for the main model varies between 2-4 and 16-64, respectively. Fig. 7(a) demonstrates a comparison between the R2-score achieved by different hyperparameters used for training the

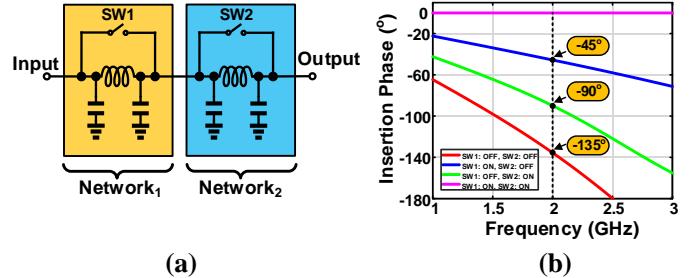


Fig. 9. Using FuNToM as the simulator in circuit sizing by NSGA-II algorithm to meet the desired specification in Table V. (a) The given phase shifter topology. (b) Insertion phase results over frequency for different switch conditions.

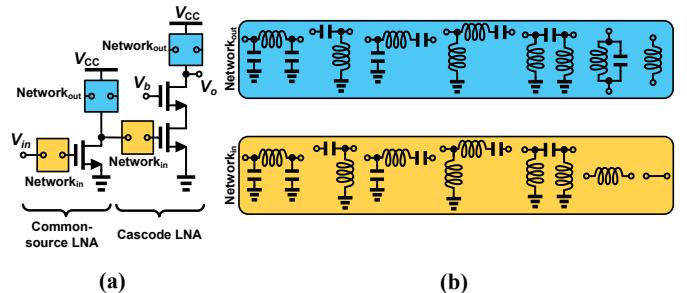


Fig. 10. Two-stage LNAs tested on FuNToM. (a) General structure; 1st stage is a common-source LNA while the 2nd stage is a cascode LNA. (b) Input and output matching networks for each stage.

main model. Fig. 7(b) also shows the loss vs. epoch of training and validation data of the main model. As it is shown, the training stops before overfitting happens. All sub-NNs have two hidden layers with 32 nodes at each layer.

Table III summarizes the average R2-score of sub-NNs and main NNs tested on different specifications of phase shifters. The average R2-score of all models is around 0.97. Moreover, Fig. 8(a) depicts an example of a phase shifter tested on FuNToM. Fig. 8(b) shows the predicted insertion phase as an example modeling specification by FuNToM over frequency compared to the simulated values.

The required number of training data per frequency is compared with the state-of-the-art works [2], [13] while all achieve the same average R2-score of 0.95. We also consider both CCI-NN (Fig. 3(b)) and FC-NN (Fig. 3(c)) structures for the main NN of FuNToM. 1600 different phase shifters with the general structure of Fig. 6 in 36 topologies are given to all approaches for testing. Moreover, a wide range of design parameters is given to cover Table II. As summarized in Table IV, [13], and [2] need 8.2x and 2.8x more training data than FuNToM, respectively. Moreover, FuNToM with FC-NN structure requires 2.4x more training data than FuNToM with CCI-NN structure.

In order to further demonstrate the functionality of FuNToM, we apply it as the circuit simulator to a circuit sizing method. For this purpose, we employ the well-known multi-objective genetic algorithm NSGA-II [23] to optimize the phase-shifter shown in Fig. 9(a). An example of desired

TABLE V

AN EXAMPLE OF USING FUNTO M VS. SPICE AS THE CIRCUIT SIMULATOR FOR SIZING FIG. 9(A) CIRCUIT. DESIRED VS. GENERATED SPECIFICATIONS AT 2 GHZ FREQUENCY FOR DIFFERENT SWITCH CONDITIONS ARE COMPARED.

SW1	SW2	Specification	Simulator result	
			FuNToM	SPICE
ON	OFF	Insertion phases = -45°	-45.61°	-45°
OFF	ON	Insertion phases = -90°	-89.95°	-89.96°
ON	OFF	Input return loss < -35 dB	-43.5 dB	-70.6 dB
OFF	ON	Input return loss < -35 dB	-37.8 dB	-61.3 dB
Runtime			180s	3,600s

TABLE VI
STATISTICS OF PERFORMANCE OF INTERESTS FOR LNAs.

Specification	Min	Max	Average	SD
Transducer gain [dB]	-183.7	10.73	-20.04	14.73
Power gain [dB]	-169.4	69.1	-9.1	14.6
Available gain [dB]	-169.4	14.58	-8.17	12.93
Noise Figure [dB]	0.06	3082	17.15	18.48
Input return loss [dB]	-60	0	-4.58	-10.75
Output return loss [dB]	-60	0	-4.58	-11.06
Rollett's stability factor	-2.4×10^5	10×10^{19}	4.2×10^{12}	4.5×10^{15}
Stability factor	2.1×10^{-4}	2.01	0.36	0.33
Maximum power gain frequency [GHz]	0.3	1.89	1.4	0.78
DC power [mW]	2.4	2.7	2.54	0.15

TABLE VII
AVERAGE R2-SCORE OF FUNTOOM MODELS TESTED ON DIFFERENT SPECIFICATIONS OF LNAs SHOWN IN FIG. 10.

Model	Sub-NNs	Common-source LNA main NN	Cascode LNA main NN
R2-score	0.987	0.975	0.982

specifications at 2 GHz frequency is listed in Table V. In the NSGA-II algorithm, the population size and number of generations are set to 30 and 30, respectively. The results when FuNTOM and SPICE are used as the simulator in the sizing are summarized in Table V. It should be mentioned that the FuNTOM results are obtained when the generated circuit using FuNTOM is verified by SPICE. FuNTOM is 20x faster than SPICE, while both meet the desired specifications. The insertion phase over frequency of the sized circuit using FuNTOM is shown in Fig. 9(b) for different switch conditions. The network₁ and network₂ are designed to have an insertion phase of -45° and -90°, respectively, at 2 GHz based on Table V. As expected, the phase shifter insertion phase is 0° when both switches are ON (meaning input and output are short-circuited). On the hand, when both switches are OFF, the insertion phase is -45°+(-90°) = -135°.

B. Two-stage LNA

Fig. 10(a) demonstrates the general structure of the two-stage LNAs tested on FuNTOM. All combinations of E-networks shown in Fig. 10(b) are used for input and output matching. So, in total, FuNTOM is trained and tested on $7 \times 7 = 49$ different LNA topologies at each stage which results in $49 \times 49 = 2401$ total topologies. There are, on average, 14 design parameters at each topology. The tested specification statistics for the two-stage LNAs are summarized in Table VI. In total, 14,000 and 600 simulations are performed for the training set of the main NN and sub-NNs, respectively, per frequency.

The number of hidden layers and neurons per layer for the main model varies between 2-4 and 32-128, respectively. Our results show that three hidden layers with 32 neurons at each layer is the simplest model that gives a high R2-score of

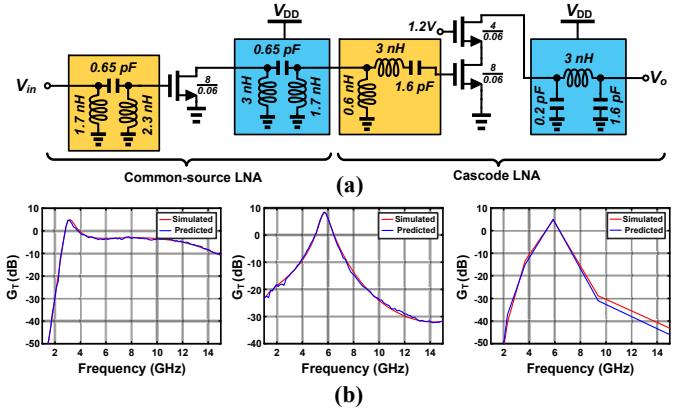


Fig. 11. An example of a two-stage LNA tested on FuNTOM. (a) Topology; size of transistors are shown as $\frac{W}{L}(\mu)$. (b) Schematic modeling: The simulated (ground truth) and the predicted transducer gain (G_T) by FuNTOM over frequency. Left: Common-source (1st) stage; middle: Cascode (2nd) stage; right: the whole LNA (two-stage).

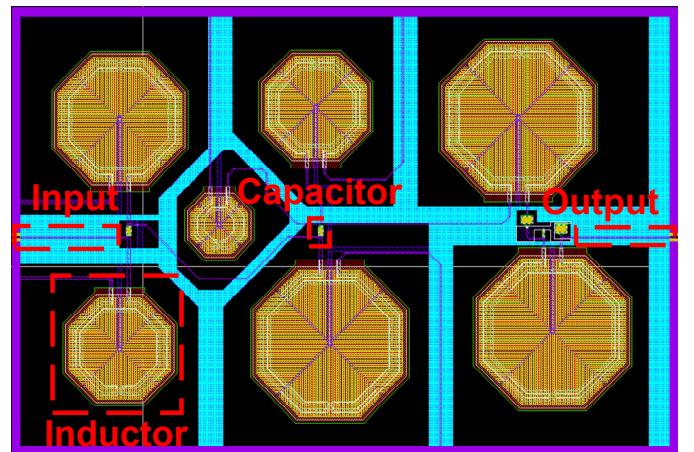


Fig. 12. The layout of Fig. 11(a).

0.97. Table VII summarizes the average R2-score of sub-NNs and main NNs while tested on two-stage LNAs. Fig. 11(a) shows an example of a two-stage LNA tested on FuNTOM. Fig. 11(b) illustrates the predicted transducer gain (G_T) as a sample modeling specification by FuNTOM in the schematic modeling over frequency compared to the simulated values for each stage as well as the whole circuit.

Fig. 12 demonstrates the layout of Fig. 11(a) which is used for post-layout modeling. As mentioned earlier, for the post-layout modeling we only need to gather training sets for sub-NNs, while the training set of the main NN is the same as what has been gathered for the schematic analysis. Moreover, the idea of transfer learning [3] can be used to further reduce the number of training samples when going from schematic to the post-layout modeling. Fig. 13 shows the predicted transducer gain (G_T) in the post-layout modeling by FuNTOM over frequency compared to the simulated values for each stage as well as the whole circuit.

The required number of training data per frequency as well

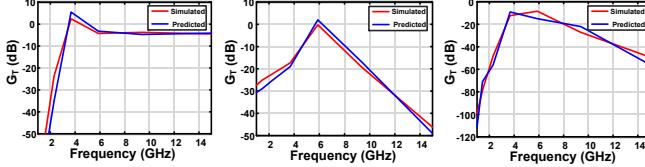


Fig. 13. Post-layout modeling of Fig. 12: The simulated (ground truth) and the predicted transducer gain (G_T) by FuNToM over frequency. Left: Common-source (1st) stage; middle: Cascode (2nd) stage; right: the whole LNA (two-stage).

TABLE VIII

REQUIRED NUMBER OF TRAINING DATA PER FREQUENCY AS WELL AS THE AVERAGE TIME FOR COLLECTING THE TRAINING SET IN POST-LAYOUT MODELING PER SAMPLE COMPARISON BETWEEN THE STATE-OF-THE-ART WORKS TO ACHIEVE AN AVERAGE R2-SCORE OF 0.95. ALL APPROACHES ARE TESTED ON 1600 DIFFERENT TWO-STAGE LNAs WITH THE GENERAL STRUCTURE OF FIG. 10 THAT ARE SELECTED FROM 2401 AVAILABLE TOPOLOGIES.

Work	[13]	[2]	FuNToM FC-NN (Fig. 3(c))	FuNToM CCI-NN (Fig. 3(b))
Training data number	7,200,000	160,000	48,100	14,600
Average time for collecting the training set in post-layout modeling per sample	5,790s	5,430s	30.7s	30.7s

as the post-layout modeling training time of FuNToM are also compared with [2], [13] while all are achieving the same average R2-score of 0.95. 1600 different two-stage LNAs with the general structure of Fig. 10 that are selected from 2401 available topologies are given to all approaches for testing. Moreover, a wide range of design parameters is given to cover Table VI. As summarized in Table VIII, [13], and [2] need 493.1x and 10.9x more training data than FuNToM, respectively. Moreover, FuNToM with FC-NN structure requires 3.3x more training data than FuNToM with CCI-NN structure. Furthermore, the average time for collecting the training set in the post-layout modeling of FuNToM is 188.6x and 176.8x less in comparison with [13] and [2], respectively.

To calculate this average time, we measure the average post-layout simulation time for generating each training sample needed in each approach. In [2], [13], the post-layout simulation is run on the whole and half of the circuit, respectively, for generating each sample which is very time-consuming considering 4-8 inductors are included. However, in FuNToM, 14,000 of the required data are for the main NN which their post-layout simulations are very fast as they include only transistors and modular S-parameters. Moreover, the 600 training data for sub-NNs are gathered by simulating the E-networks that include only one or two inductors which are relatively fast. So, as the results show, the average time for running each simulation for FuNToM is much less than the other approaches. We save around 240,000 hours ($160,000 \times 5,430s - 14,600 \times 30.7s = 240,000h$) by using FuNToM instead of [13] in such a post-layout training.

V. CONCLUSION

This work presents a novel RF functional modeling method, FuNToM. FuNToM divides circuits into multiple E-networks and analyzes them modularly via NNs. Leveraging such a modular analysis using the concept of S-parameters has made the NN models used in FuNToM general enough that work for multiple circuit topologies. To validate our work, FuNToM is tested on more than 1,600 phase shifters and 1,600 two-stage LNAs. The results indicate that FuNToM reduces the size of the required training data by 2.8x - 10.9x in comparison with the state-of-the-art works while maintaining the same accuracy. Moreover, FuNToM needs 176.8x - 188.6x less time for collecting the training set in post-layout modeling.

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