# QFlow: Quantitative Information <u>Flow</u> for Security-Aware Hardware Design in Verilog

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Abstract—The enormous amount of code required to design modern hardware implementations often leads to critical vulnerabilities being overlooked. Especially vulnerabilities that compromise the confidentiality of sensitive data, such as cryptographic keys, have a major impact on the trustworthiness of an entire system. Information flow analysis can elaborate whether information from sensitive signals flows towards outputs or untrusted components of the system. But most of these analytical strategies rely on the non-interference property, stating that the untrusted targets must not be influenced by the source's data, which is shown to be too inflexible for many applications. To address this issue, there are approaches to quantify the information flow between components such that insignificant leakage can be neglected. Due to the high computational complexity of this quantification, approximations are needed, which introduce mispredictions. To tackle those limitations, we reformulate the approximations. Further, we propose a tool QFlow with a higher detection rate than previous tools. It can be used by nonexperienced users to identify data leakages in hardware designs, thus facilitating a security-aware design process.

*Index Terms*—hardware security, hardware Trojans, quantitative information flow, vulnerability, confidentiality

### I. INTRODUCTION

Many security issues are either caused accidentally by inexperienced hardware designers or by malicious modifications, such as hardware Trojans [1] [2]. In the rest of this work, those issues are referred to as vulnerabilities. The vulnerabilities should be identified and removed at an early design stage, as later modifications result in higher costs or a longer timeto-market. They can be identified using suitable test models, but the required test models become more computationally extensive with the increasing design complexity [3], thus not all test cases can be elaborated in a reasonable time. Additionally, theorem provers [4], property checkers, and formal approaches give more certainty, but often require special expertise to be used properly and suffer from scalability issues.

One of the critical features of hardware security is the confidentiality of data. Vulnerabilities endangering the confidentiality of sensitive signals, such as cryptographic keys, can be implemented easily and stay undetected in common test cases, as the trigger might not be present in the program code and data. Therefore, we focus on protecting the confidentiality in this work. Information flow analysis is an evolving research area and used as a method to detect hardware vulnerabilities concerning the confidentiality of data carried by digital circuits. A variety of solutions exist working on virtual prototypes [5] or Register-Transfer Level (RTL) [6]–[8] to analyze the flow of information of marked signals, either dynamically (tracking) or statically (analysis). As dynamic elaborations analyze the information flow at runtime, they can only guarantee the security of a hardware design for given test

cases [5]. Most of these tools rely on analyzing the flow of information for the non-interference property. But this property, which forbids the communication between trusted and untrusted hardware components, can often not be implemented, as many applications rely on such a communication. Stateof-the-art methods, such as QIF-Verilog [9], use Quantitative Information Flow (QIF) analysis, which allows a quantification of the actual leakage using developed metrics that have been shown to be suitable to detect leakages in digital systems [10] [11]. This analysis allows a new classification of leakage paths supporting the identification of data leakages. However, in this work, QIF-Verilog is shown to be unreliable in the identification of certain design vulnerabilities. Therefore, we introduce a more suitable methodology, QFlow, capable of detecting even the new vulnerabilities.

The major contributions of this paper are: i) An operational tool that uses a suitable QIF metric, called QModel, to quantify the trustworthiness of a Verilog hardware description regarding the protection of its sensitive signals, e.g., cryptographic keys or user data, ii) A secure approximation of state-of-the-art QIF formulas that removes the possibility of false negative predictions, while only enabling false positives, as shown empirically and iii) User-adjustable input probabilities for the information theory equations on bit level.

# II. PRELIMINARIES

# A. Attack Model

We focus on vulnerabilities that are implemented during the RTL-design process. Those vulnerabilities can be exploited by an adversary after production. In this work, we assume that the attacker can observe the outputs and the non-secret inputs of the selected hardware modules at a random moment in time. These outputs might leak signals carrying sensitive information, such as user data, via leakage paths. Whether those observations are obtained by physical access to the design or via other untrusted hardware in the System-on-Chip (SoC) is not considered. Additionally, the intruder cannot set any of the input values of the module under attack. During the attack, the complete design structure is known to the adversary.

## B. Information Flow Analysis

The designer is interested in protecting certain parts of the hardware carrying sensitive data. For this purpose, previous works used labels to classify the sensitivity of hardware models and the data that is carried in them [12]. In most information flow models the system of interest is separated into two partitions: High (H) and Low (L). The H label is commonly used to describe trusted hardware components processing sensitive data. When labeling the hardware components, the trusted components would be labeled H, while the remaining components are labeled L. These are abstract labels, but the labels are commonly applied by marking the component's hardware description with their respective label [6]. The labels H and L are propagated throughout the system related to the dependency of the signals.

#### C. Quantitative Information Flow

In many previous works [13] [14], the vulnerability, a metric for the weakness or simplicity to guess the secret, has shown to be a reliable function when quantifying the information flow. The Bayes Vulnerability represents a special case of the g-vulnerability, when the adversary has only a single guess of the secret after one observation of the outputs and is only rewarded for a correct guess [15] [10]. For a secret H with a probability distribution of  $\pi_H$ , the vulnerability is

$$V_1[\pi_H] = \max_{h \in \mathcal{H}} \pi_h,\tag{1}$$

where  $\pi_h$  is the probability of the symbol  $h \in H$ . In this work, we are interested in the leakage caused by an information flow from a secret H to the outputs of a system O. Therefore, the Posterior Bayes Vulnerability  $V_1[\pi_H \triangleright C]$  (PBV) has to be considered as well. The posterior vulnerability shows the vulnerability after observing the outputs O, if the secret bits H have been applied to the deterministic channel  $C(\pi_H \triangleright C)$ :

$$V_1[\pi_H \triangleright C] = \sum_{o \in \mathcal{O}} \max_{h \in \mathcal{H}} J_{o,h}.$$
 (2)

Here, J represents the joint distribution for the variables in the index. The channel is an abstract definition of the hardware system. When combining the two Bayes Vulnerabilities, the so-called Multiplicative Bayes Leakage  $\mathcal{L}_1^{\times}$  is computed as:

$$\mathcal{L}_1^{\times} := \frac{V_1[\pi \triangleright C]}{V_1[\pi]}.$$
(3)

As the leakage computation for a complete hardware description would be infeasible, approximations are needed.

# III. QFLOW

# A. Basic Functionality

Our QIF-metrics are used to quantify the information flow from the 'High' sources, the marked signals, via all the operations that are applied on the secret, to the 'Low' targets. All output ports of the top design are automatically marked as 'Low'. In contrast to QIF-Verilog, we preprocess the abstract syntax tree to allow a bit-wise analysis to track the information flow in more detail. We compute the leakages in several steps. First we build channels consisting of Boolean equations representing the partitioned hardware. Next, the input probabilities and PBV for the channels are computed and combined with the input leakages of the channel to compute the total leakages for every single secret bit.

#### **B.** Approximation Assumptions

Certain assumptions are needed to reduce the amount of computations needed to determine leakage values for the secrets: i) The secret and known bits are independent of each other, ii) Compute Probabilities: The inputs of every channel are independent of each other, iii) Compute Posterior Vulnerability: The inputs of every channel are independent of each other. Additionally for COMPARISON, ADDITION, and SUBTRACTION operations, the high inputs are assumed to be uniformly distributed and iv) Compute Leakage: The dependency of input leakages is appraised with Eq. (8). As the low inputs can be observed by the adversary as well, they need to be integrated into the equation for the PBV.

## C. QModel

The assumptions and appraisals lead to our mathematical model, called QModel, implemented in our tool QFlow. This model is further explained below. As mentioned before, we modified the equation for the PBV (Eq. (2)) to include the low input signals L. They are added to the equation as additional observable parameters—similar to the outputs O:

$$V_1[\pi \triangleright C|L] := V_1[H|L, O] := \sum_{\substack{o \in \mathcal{O} \\ l \in \mathcal{L}}} \max_{h \in \mathcal{H}} J_{o, l, h}, \qquad (4)$$

with the joint probability distribution  $J_{o,l,h}$ ,

$$J_{o,h,l} = \pi_{o|h,l} \cdot \pi_{h,l}.$$
(5)

A feasible way to compute the leakage in a channel cascade is needed. Thus, we derived the following statement for the leakage  $\mathcal{L}_{X \to Z}$  (in bit) of a Markov chain:

$$\mathcal{L}_{X \to Z} := \mathcal{L}_{X \to Y} \cdot \frac{\mathcal{L}_{Y \to Z}}{\mathcal{L}_{Y \to Z, max}}.$$
 (6)

For a Markov chain of channels  $X \to Y \to Z$ , the input values X are converted to the output Z with Y as an intermediate value. The data processing inequality states that no processing of Y can increase the information that Y has about X [15]. Thus, we weigh the leakage of channel  $X \to Y$  with the leakage of the second channel, scaled with its maximum possible leakage. When inserting the multiplicative Bayes Leakage (Eq. (3)) and the maximum leakage for the second channel, the reciprocal of the Prior Bayes Vulnerability (Eq. (1)), we derive the following equation:

$$\mathcal{L}_{X \to Z} = \mathcal{L}_{X \to Y} \cdot \frac{\frac{V_1(\pi_Y \triangleright C_{Y \to Z})}{V_1(\pi_Y)}}{\frac{1}{V_1(\pi_Y)}}$$
$$= \mathcal{L}_{X \to Y} \cdot V_1(\pi_Y \triangleright C_{Y \to Z}).$$
(7)

The input leakage into a channel (now in bit) can be further approximated as stated before in the Section III-B using [16]

$$\mathcal{L} \leq \sum_{i \in \text{Inputs}} \mathcal{L}_i,$$
 (8)

resulting in our final equation for the leakage of a secret bit  $H_j$  in a channel cascade  $\mathcal{L}_{C,H_j}$ . The probability distribution of the secret channel inputs is represented by  $\pi_{HI}$  and is used to compute the overall PBV of that channel:

$$\mathcal{L}_{C,H_j} := \sum_{i \in \text{Inputs}} \mathcal{L}_{i,H_j} \cdot V_1(\pi_{HI} \triangleright C).$$
(9)

# D. Toolflow

## The general toolflow of QFlow is illustrated in Fig. 1.

1) ParseArgs: Some parameters and the Verilog code are passed to the program. The signal that is supposed to stay secret is marked as 'High'.

2) *QIF-Parser:* The QIF-parser integrates the open-source tool PyVerilog, which is responsible for parsing Verilog and returning a graph of binds. A bind in such a graph mostly represents a single line of RTL code with terminal symbols,

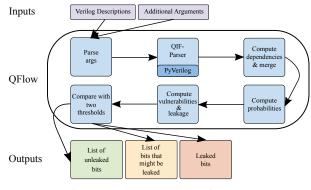


Fig. 1: General toolflow of QFlow.

such as signals and constants as its leaves. As we intend to work on the bit level of the design, we need to process the bind tree. Then, each tree has an output bit as the root and only input signals and constants can be leaves. An example for such a tree can be found in Fig. 2. For the given circuit in Fig. 2a, the tree structure is illustrated for the first bit of the output in Fig. 2b. The leaves (green) consist of the inputs of the circuit and constants. Operations (yellow) are connected to their outputs (orange) until an output, the root (red), is reached.

3) Compute Dependencies & Merge: Afterwards, the tool computes the dependencies and starts merging nodes. The dependencies are needed to find loops in the tree structure to avoid merging them infinitely. Merging is done to increase the channel sizes, thus reducing the number of channels that are cascaded. Every cascade of channels introduces an error in the computed leakage, due to the approximations done with the equations presented before. A negative error can be introduced due to the assumption of independent channel inputs, whereby the simple addition of input leakages introduces a positive error. In this paper, it is shown empirically that the positive error outweighs the negative one. The merging is stopped when the maximum number of input bits in the Boolean expression (max channel inputs) is reached. This is done to reduce the complexity for the next step, computing the probabilities. Furthermore, sequential branches are not merged as this may result in a security risk and misinterpretation of hardware vulnerabilities, which introduces an additional positive error. The example's tree was merged with max channel inputs=3, as shown in Fig. 2c.

4) Compute Probabilities: The merged trees are forwarded to the 'Compute Probabilities' function. Here, the output probabilities of every channel input bit are computed. The probability of the outputs is calculated by multiplying the input probabilities for a given case because of the assumed independence. An example for the computation of the probabilities is shown in Fig. 2c with uniform input probabilities.

5) Compute Vulnerability & Leakage: All the computed probabilities are written into the respective nodes. Next, it is possible to compute the posterior vulnerabilities for every channel using Eq. (4). All the example's computed probabilities are illustrated in Fig. 2c. For the computation of the PBV, the joint probability distributions need to be computed with Eq. (5) for every channel. Furthermore, the leakage of the input bits is set for every secret bit. If multiple inputs hold information about a secret bit, their leakage is added

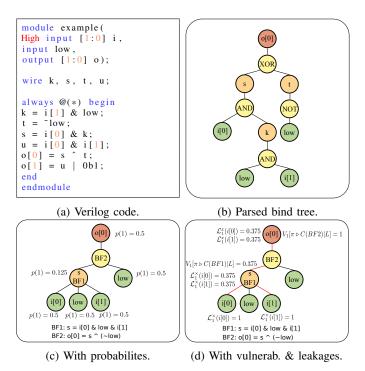


Fig. 2: Example for the computational steps for a small circuit.

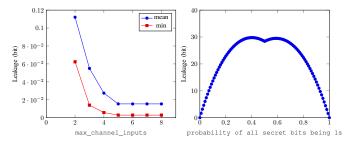
beforehand to appraise possible dependencies. From that point on, the leakage of every secret bit is multiplied with the PBV of the current channel. For every output bit, the leakages for all secret bits that influence it are computed by using the Eq. (9) over all channels starting at the leaves. Finally, the total leakage for every secret bit is computed by adding their leakage from every output bit.

6) Compare with two Thresholds: Now that the leakage values for the different secret input bits are computed, we need to determine, which of the data paths are actually a vulnerability in the system. We determine a threshold and compare our computed value for every secret bit to it.

7) *Classification:* After the accumulated leakages for every bit that is labeled with 'High' is computed and they have been compared to the thresholds, the leakage paths can be written out. This is done in three groups: Paths that leak (higher than detection threshold), paths that might leak (warning threshold), and paths that do not leak (below both thresholds). For the example, this is shown with the red connections in Fig. 2d.

# IV. EVALUATION

For the evaluation, multiple open-source benchmarks were used to show the efficiency and flexibility of QFlow in detecting security vulnerabilities concerning the confidentiality of data. During the design process, the hardware designer is capable of elaborating the security of certain signals by marking them with 'High' inside his code. A second parameter that we alternate during the experimentation is the probability of the high input bits. This is done to show the influence of the probability on the leakage and illustrates the capability of the tool to emphasize the detection of hardware Trojans using controllable triggers. The same benchmarks are used to elaborate QIF-Verilog as well, thus they allow a comparison. In the beginning, the required thresholds were determined by



(a) Minimum and mean leakage. (b) Leakage over probabilities.

Fig. 3: Leakage for two pipelined AES rounds varying max\_channel\_inputs (left). Leakage for AES-T100 AES varying probabilities max\_channel\_inputs=5 (right).

applying QFlow to two pipelined rounds of AES. This was done for uniformly distributed inputs, as they allow the highest leakage, leading to a more general threshold, while varying max\_channel\_inputs. For most of the elaborations, AES and RSA benchmarks from Trust-Hub [17] are used, which offer cryptographic accelerators in Verilog (and VHDL [18]). They offer a variety of Trojans using either triggers or continuously write out the keys over additional output ports. Furthermore, we implemented additional benchmarks to prove QFlow's functionality compared to QIF-Verilog.

### A. Results

At first, we analyzed a single AES benchmark for varying high input probabilities to illustrate the flexibility of QFlow and show the meaning of leakage. For the analysis, the probability of the 128-bit key was altered from 0 to 1 for all secret bits equally. The results (Fig. 3b) show that although the leakage for the system is 0 for the higher and lower probabilities, the attacker can still guess the keys as the Prior Bayes Vulnerability is at 1 bit. Even a solid hardware implementation cannot protect an insecure secret.

As mentioned before, the threshold was determined by applying QFlow to a Verilog implementation of two pipelined rounds of AES (by reducing one of the AES benchmarks). Two complete rounds of AES are supposed to lead to a full diffusion [19]. Fig. 3a shows the minimum and average value of the 128-bit leakages for the keys with a varying max channel inputs value. As expected, the leakage drops, when more operations are merged into a single channel, reducing the error introduced by Eq. (8) and the assumed independence of inputs. The smallest mean and min leakages that were computed were chosen as the threshold for the warning (min,  $2.89154 \cdot 10^{-3}$ ) and threat (mean,  $1.53939 \cdot 10^{-2}$ ) for the toolflow. The leakage did not drop after setting the maximum number of input values during the merge to 5. Thus, the value for max channel inputs is set to 5 for all following elaborations. After the threshold was determined, the first analyses on the AES benchmarks were conducted. The results of these experiments can be seen in Fig. 4, illustrating the computed leakage for two different Trojans over the 128bit key. The T-1200 benchmark leaks the first 8 bit of the key, which was XOR-ed with a value that can be determined by the intruder value. Thus, the XOR is not reducing the information content. Additionally, the Trojan is triggered continuously.

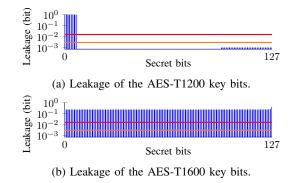


Fig. 4: Leakages (Thresholds: Det. (Red) and Warn. (Orange)).

This behavior is shown in Fig. 4a. The first 8 bits are leaked completely, while the other bit's leakages are low, due to the 10 rounds of AES. A second Trojan leaks the entire 128-bit key sequentially, when a certain condition is set. This condition and the sequential communication, reduces the likelihood of the attacker to gain information reducing the leakage to around 0.22 bits. For both benchmarks all leakages are detected and can be assigned to the actual secret bits. Table I gives a summary of the experimental results for the AES and RSA benchmarks each containing a variety of Trojans. All leakages are detected, but one false positive detection and warning are given out for the RSA benchmarks. A short runtime of around 145 to 250s supports the claim that QFlow can assist designers in combination with their electronic design automation tools to allow a fast, yet security-aware design process. If secret bits are leaked entirely, it is detected as such with a leakage value of 1. If additional operations are executed on the values, or triggers reduce the probability of them being leaked, their leakage value also reduces, as they are less likely to be leaked, posing a smaller threat for the given attack scenario.

#### B. Additional Benchmarks

As mentioned before, we implemented some benchmarks and used the designs of the AES-T series from Trust-Hub as a basis. The modifications to the designs are explained in Fig. 5, staying with the naming convention and introducing T2100, T2200, and T2300. As QIF-Verilog ignores data dependencies and increases its uncertainty value depending on what operation is conducted on the secret, disregards which signals are combined, certain vulnerabilities are introduced. We rebuilt OIF-Verilog [9] and tested it on those benchmarks. The results can be seen in Fig. 5 d). Trojans that use operations that deconcatenate the key with itself followed by a concatenation, are not detected, as the tool identifies the operation as an increase in the uncertainty caused by the deconcatenation, although the value is not changed at all. The other Trojans are not explained further but are described in detail in Fig. 5a-c. QFlow was able to detect all those Trojans using the adapted equations and the merging approach to identify dependencies and quantify the leakage more accurately. Limitations: As mentioned before, the attack model for the designed QIFmodel states that the attacker cannot set any input values, but can only observe the output once at a random moment. Knowing that the designer is not aware or certain about the design's vulnerability, they cannot know the inputs or

TABLE I: AES- and RSA-Trojan benchmark leakages [20] [17]("AL" = Average leakage).

Benchmark	#Detected /#Actual	Avg. Det. Leakage	#FP Det. /AL	#FP Warn. /AL	#Unleaked /# Actual	Avg. Sec. Leakage	Time (s)	Trojan Type leaking information	
AES-T100	8/8	1	0/-	0/-	120/120	$2.66 \cdot 10^{-4}$	246	Trigger:always; Payload:covert channel	
AES-T200	8/8	1	0/-	0/-	120/120	$2.66 \cdot 10^{-4}$	214	Trigger:always; Payload:covert channel	
AES-T400	128/128	0.183	0/-	0/-	0/0	-	245	Trigger:input; Payload:RF signal	
AES-T700	8/8	1	0/-	0/-	120/120	$2.66 \cdot 10^{-4}$	236	Trigger:input; Payload:covert channel	
AES-T800	8/8	1	0/-	0/-	120/120	$2.66 \cdot 10^{-4}$	232	Trigger:input; Payload:covert channel	
AES-T900	8/8	1	0/-	0/-	120/120	$2.66 \cdot 10^{-4}$	231	Trigger:counter; Payload:covert channel	
AES-T1000	8/8	1	0/-	0/-	120/120	$2.66 \cdot 10^{-4}$	232	Trigger:input; Payload:covert channel	
AES-T1100	8/8	1	0/-	0/-	120/120	$2.66 \cdot 10^{-4}$	238	Trigger:input; Payload:covert channel	
AES-T1200	8/8	1	0/-	0/-	120/120	$2.66 \cdot 10^{-4}$	233	Trigger:counter; Payload:covert channel	
AES-T1600	128/128	0.222	0/-	0/-	0/0	-	234	Trigger:input; Payload:RF signal	
AES-T1700	128/128	0.295	0/-	0/-	0/0	-	148	Trigger:counter; Payload:RF signal	
RSA-T100	33/32	0.5	1/0.023	1/0.006	30/32	$6.3 \cdot 10^{-5}$	196	Trigger:input; Payload:via Ciphertext	
RSA-T300	33/32	0.5	0/0.023	1/0.023	30/32	$6.3 \cdot 10^{-5}$	191	Trigger:counter; Payload:via Ciphertext	

//In TSC.v	// In TSC.v	//In top.v
module TSC(	module TSC(	TSC Trojan (rst, clk,
input rst,	input rst,	key, state,
input clk,	input clk,	Capacitance);
input [127:0] key,	input [127:0] key,	//In TSC.v
output [63:0] load	output [63:0] load	module TSC(
);	);	input rst,
reg [63:0] load;		input clk,
reg [63:0] tmp0, tmp1,	reg [63:0] load;	input [127:0] key,
tmp2, tmp3;	reg [63:0] tmp0, tmp1;	input [127:0] in,
	reg [63:0] tmp2, tmp3;	output [63:0] load
genvar i;	reg [63:0] tmp4, tmp5;	);
generate		reg [63:0] load;
for $(i=0; i < 64; i=i+1)$		reg [127:0] tmp0, tmp1;
begin	always @ (posedge clk)	reg [127:0] tmp2, tmp3;
always @ (posedge clk)	begin	reg [127:0] tmp4;
begin	$tmp0 \le key[63:0]$	
$tmp0[i] \le key[i];$	& key[63:0];	always @ (posedge clk)
<pre>tmp1[i] &lt;= tmp0[i];</pre>	$tmp1 \le key[63:0]$	begin
tmp2[i] <= tmp1[i];	key[63:0];	tmp0 <= in ^ key;
tmp3[i] <= tmp2[i];	$tmp2 \leq tmp0 \uparrow tmp1;$	tmp1 <= tmp0 ^ in;
load[i] <= tmp3[i];	$tmp3 \leq tmp0   tmp1;$	tmp2 <= tmp1 ^ in;
end	$tmp4 \leq tmp2 \ tmp3;$	tmp3 <= tmp2 ^ in;
end	tmp5 <= tmp3 & tmp3;	tmp4 <= tmp3 ^ in;
endgenerate	load <= tmp4   tmp5;	load <= tmp4[63:0];
	end	end
endmodule	endmodule	endmodule

	AES-Benchmarks							
	T2100	T2200	T2300					
QIF-Verilog (rebuilt)								
Time (s)	24.2	23.7	22.1					
Accu. Uncertainty	379	320	384.0					
Threshold	318.72	318.72	318.7					
Detec.?	No	No	No					
QFlow								
Time (s)	298	297	292					
Total Leakage	64.03	64.03	64.03					
Detec.?	Yes	Yes	Yes					

(a) AES-T2100

00 (b) AES-T2200

(c) AES-T2300

(d) Leakages of new benchmarks.

Fig. 5: New benchmarks to show the vulnerabilities in QIF-Verilog. Three Trojans leaking 64 bit.

triggers that make the circuit most vulnerable. This reduces the computed leakage compared to the actual leakage for highly unlikely leakage paths. Furthermore, hardware Trojans or unintentional vulnerabilities that leak a low amount of information over a longer period of time might not be detected.

## V. CONCLUSION

In this publication, we introduced QFlow, a tool allowing the hardware designer to create a more security-aware design process using Quantitative Information Flow. It was shown that by using a suitable approximation, the hardware design can be separated into several channels to reduce the computational complexity, when independence of the channel's inputs is assumed. However, this dependency needs to be considered for merging leakage paths. The tool was proven to be more reliable for the defined attack model than the state-of-the-art tools. A simple usage and the acceptable computation time, support the claim that QFlow allows a security-aware design process that can be conducted by inexperienced users.

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