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DESIGN OF A 3RD ORDER MICRO POWER SWITCHED CURRENT ΣΔ-MODULATOR

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ABSTRACT

This paper reports the design of a 3rd order switched current-ΣΔ-modulator. The modulator is design to have a SNR of $80dB$ with a signal bandwidth of $f_b = 6kHz$. The oversampling ratio is $R = 90$ and the sampling frequency $f_s = 1.08MHz$. Multiple input signals are used to reduce the internal signal swings, which results in reduced power consumption. The noise from the 2nd and 3rd integrator is shaped. This is used to allow the noise power from these integrators to be increased and hence saving power. The power consumption of the first integrator is $254\mu W$ and the total power consumption is $600\mu W$. The supply voltage is $V_{DD} = 2.7V$. A new methology is presented that allows for optimization of SI circuits for minimum power consumption with respect to process tolerances.

1. INTRODUCTION

Over the last years ΣΔ-modulators have gained increasing popularity as they have the potential for high accuracy data conversion with modest analog requirements. The reason for the popularity originates in the fact that the quantization noise is moved from the signal band $[-f_b; +f_b]$ to high frequencies (Noise Shaping). This allows for very coarse quantization, e.g., 1-bit using a simple comparator. This type of quantization does not introduce static nonlinearities and simplifies the analog circuitry.

To obtain high accuracy, e.g., $SNR > 80dB$, for second order ΣΔ-modulators it is necessary to use a very high oversampling ratio (R), e.g., $R > 128$. This problem can be overcomed by using higher order ΣΔ-modulators as the quantization noise in the signal band is reduced when the order of the ΣΔ-modulator is increased for a fixed R. For a more thorough analysis of different structures for ΣΔ-modulation see [4].

2. SYSTEM DESIGN

In figure 1 the 3rd order ΣΔ-modulator is illustrated. The signals are shown as currents as the ΣΔ-modulator is to be implemented using switched current (SI) techniques.

The quantizer in figure 1 can be modeled by replacing the comparator with a amplification factor, K_n, and a white noise source, n_q, that represents the quantization noise [2], [3]. It is a widespread misunderstanding to assume that the gain K_n equals one because if it was so then the modulator would not be invariant to variations in k_3. In fact, it is not necessary to assume anything about the gain K_n in order to design the modulator filter, i.e., b_1, b_2 and b_3.

First assume that $k_1 = k_2 = k_3 = 1$ and $a_2 = 0$, i.e., no scaling and only one input to the ΣΔ-modulator. The constants b_1, b_2 and b_3 determine the noise transfer function $NTF(z)$ for the quantization noise (the transfer function from n_q to the output y). It is easily shown that the quantization noise is shaped by a 3rd order highpass filter, i.e., the quantization noise is moved from low frequencies to high frequencies. This is illustrated in figure 2.

The ΣΔ-modulator coefficients b_1, b_2 and b_3 are determined by designing the $NTF(z)$ [2] as a 3rd order highpass

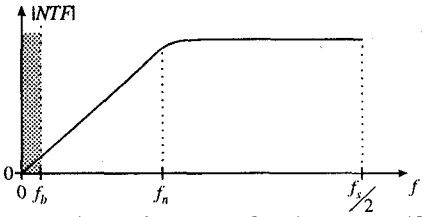

Figure 2. The noise transfer function $NTF(z)$.

Butterworth filter. It is easily shown that the transfer function from the input of the ΣΔ-modulator to the output, the signal transfer function $STF(z)$, is a 3rd order lowpass filter with a cut-off frequency much higher than f_b.

If a sinusoidal signal is forced into the ΣΔ-modulator one will observe that it becomes unstable for amplitude greater than a certain value called the maximum stability amplitude MSA [2]. The relationship between the cut-off frequency, f_n, for the designed $NTF(z)$, MSA and SNR is shown in table 1.

$\frac{f_n}{f_s}$	$\frac{SNR}{dB}$	$\frac{MSA}{I}$	$\frac{f_n}{f_s}$	$\frac{SNR}{dB}$	$\frac{MSA}{I}$
0.13	93.7	0.75	0.17	94.6	0.59
0.15	95.0	0.69	0.19	95.3	0.45

Table 1. SNR and MSA versus f_n for $R = 90$. SNR estimated by averaging 16 runs of 16384 samples.

From table 1 it can be seen that the cut-off frequency f_n has a very strong influence on the MSA whereas it has very little influence on the SNR.

If the ΣΔ-modulator is designed to have only one input ($a_2 = 0$) the internal signal swings in the integrators are very different. By forcing a sinusoidal signal with an amplitude of MSA into the ΣΔ-modulator the peak signal swing in INT1, INT2 and INT3 is approximately $5I, 16I$ and $24I$ respectively (assuming that the integrators are ideal). The internal signal swings can be adjusted to have the same peak value as the swing in the first integrator by adjusting the scaling factors k_1, k_2 and k_3. This scaling results in a constant k_3 in front of the quantizer which can be removed as a constant proceeded by a comparator does not affect the output of the comparator. This will therefore not affect the modulator filter.

The internal signal swings can be reduced further by introducing a second input, i.e., $a_2 \neq 0$. This input is added between INT1 and INT2. It was found that $a_2 = b_2$ results in an optimal reduction of the internal signal swings in the integrators by a factor of approximately 3. After introducing the second input the internal signal swings are approximately $1.7I$ for all three integrators. The reduction in the internal signal swings will substantially reduce the power consumption of the modulator, because it allows for lower bias currents in the integrators. The extra input a_2 results in a peak in $STF(z)$ at high frequencies ($\approx f_n$), that results in a slight increase of the $STF(z)$ in the signal band. At the frequency f_b the $STF(z)$ is 0.1dB larger than at DC.

In figure 1 the analog noise sources n_1, n_2 and n_3 are included too. The noise at the output of the modulator must be the sum of n_1 unfiltered, n_2 1st order highpass filtered, n_3 2nd order highpass filtered and, finally, n_q 3rd order high-

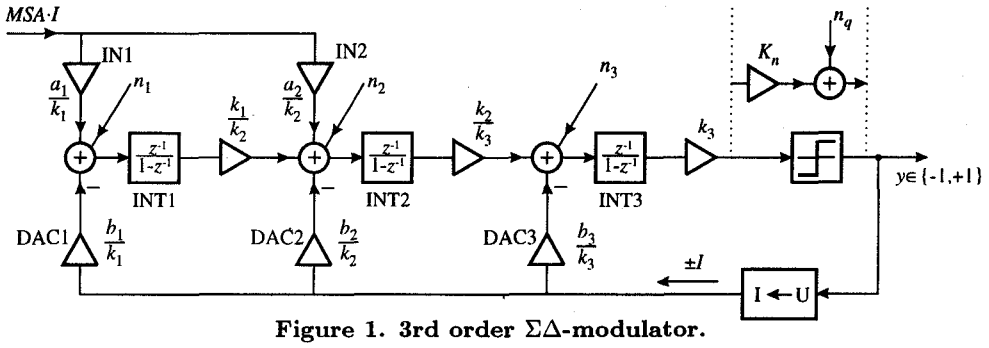

Figure 1. 3rd order ΣΔ-modulator.

pass filtered ($NTF(z)$). As the noise sources n_2 and n_3 are highpass filtered INT2 and INT3 can be allowed to generate more noise than INT1 without affecting the overall SNR at the output. In this design this technique was used to lower the internal signal swings and thereby the quiescent current in INT2 and INT3 by a factor of 2 and 4 respectively. This results in the same SNR but reduces the power consumption by a factor of $\frac{1+1+1}{1+0.5+0.25} = 1.71$.

Because the noise from INT2 and INT3 is shaped, the noise at the output of the modulator is dominated by the noise from the input section, i.e., INT1, DAC1 and IN1. The input section is therefore designed to limit the SNR to $80dB$. With an oversampling factor of $R = 90$, the quantization noise will limit the SNR to approximately $95dB$ as shown in table 1 (assuming that there is no thermal noise in the analog circuitry). By increasing the MSA we increase the signal power at the input of the modulator which allows a noisier input section for a given SNR. We utilize this to lower the power consumption. A very high MSA will result in a reduction of the SNR because the modulator begins to perform poor coding of the input signal. As a compromise we chose $MSA = 0.69I$ which equals to a $f_n = 0.15f_s$ (see table 1). The $NTF(z)$ for $f_n = 0.15f_s$ resulted in the following constants (see figure 1): $a_1 = b_2 = 1$, $a_2 = b_2 = 5.66$, $b_3 = 13.6$ and due to the scaling $k_1 = 1$, $k_2 = 17.4$ and $k_3 = 64.0$.

3. IMPLEMENTATION

The SI-integrator, shown in figure 3, is a cascode type but also a folded cascode type was considered. However, the folded cascode SI-integrator introduced extra noise due to the extra current sources needed and therefore this solution would consume more power for a given SNR.

The integrator in figure 3 has a very low input impedance as the transistors $M_{2,1}$ and $M_{2,2}$ act as current conveyors which reduce the input impedance (compared to the input impedance of a single transistor) by a factor of $L_G = (1 + \frac{g_{m2}}{g_{o2}})$ where g_{m2} and g_{o2} are the transconductance and output admittance for the M_2's. The input impedance of this circuit is therefore in the order $\frac{g_{o2}}{g_{ms}g_{m2}}$ which can be as low as 1Ω at low frequencies. This eases the interfacing to the circuit, in fact, the input devices IN1 and IN2 in figure 1 are just resistors that convert the input voltage to a current. This is indicated in figure 3.

The transfer function for the integrator is:

$$\frac{i_{out}(z)}{i_{in}(z)} = K\frac{z^{-1}}{1 - z^{-1}} \qquad (1)$$

It is important that the integrator has very little loss as any loss results in a finite DC-gain and the quantization noise will therefore be increased at low frequencies. The loss in the SI-integrator is caused by finite output resistance and the gate-drain overlap capacitances for $M_{s,1}$ and $M_{s,2}$ but the transistors $M_{2,1}$ and $M_{2,2}$ reduce these error with the same gain factor L_G as mentioned before. The loss in the SI-Integrator we have used is less than 0.1%. The scaling

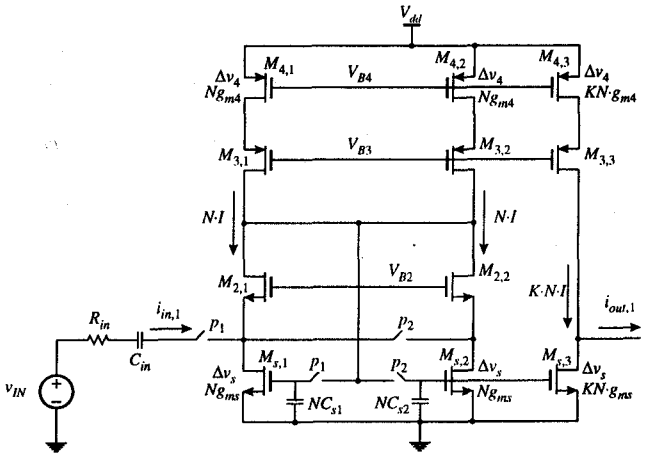

Figure 3. SI-Integrator.

factor K in figure 3 is controlled by the length and the width of MOS-transistors.

It is well known that one of the main problems using SI-circuits is the nonlinear settling behavior. This nonlinear settling behavior decreases the performance of the SI-integrator drastically, when high signal currents compared to the quiescent current are processed, and thereby, it also decreases the performance of the ΣΔ-modulator. It is, however, not possible to evaluate this problem using SPICE as the simulation time would be enormous. It was therefore necessary to evaluate this problem by other means. A 'C++'-program was written, that modeled the SI-integrator as a nonlinear component. The program models the SI-integrator as build from two current copiers (CCOP) (see, [1]). A CCOP is basically a operational transconductance amplifier (OTA) and some switches. The OTA is in the program described as a component that has a nonlinear relationship between the input voltage and the output current. For each sample the program then solves the nonlinear settling problem using the 2nd order Runge-Kutta algorithm. The program was verified by comparing its results with simulations using PSPICE, performed on relatively simple building blocks.

Simulations performed on the entire ΣΔ-modulator showed that the internal signal swings were increased from approximately $1.7I$ to $2.4I$, when the integrators were made nonlinear using a square law relationship for the OTA's in the CCOP's. Furthermore, the nonlinear settling causes a DC-component at the output of the modulator which causes nonharmonics in the signal band for small input amplitudes. To avoid this a quiescent current of $3I$, i.e., $N = 3$, is chosen.

3.1. Constraints on the Voltage Swings

The SI-integrator in figure 3 operates in class A. There are some restrictions or constraints to the operation of the circuit. These constraints are set by the fact that all transistors at any time have to be saturated to ensure proper operation of the SI-integrator. Three constraints exist for the integra-

tor shown in figure 3.

In the following Δv denotes the saturation voltage for the transistor, i.e., $\Delta v = V_{GS} - V_T$. First assume that a current of $N{\cdot}I$ (i.e., modulation index $m=1$) is stored on $C_{s,1}$ which results in $\Delta v_{s1} = \sqrt{2}\Delta v_s$, where Δv_s is the quiescent value. To ensure that the transistor $M_{s,1}$ is saturated the transistors in the first column must satisfy:

$$\text{I}: \quad V_{Ts} + \sqrt{2}\Delta v_s + \Delta v_3 + \Delta v_4 < V_{DD}$$

Second, again assume that the current $N{\cdot}I$ is stored on C_{s1}. During p_2 this current is stored onto C_{s2}. Right after clock phase p_2 goes high $M_{s,1}$ and $M_{2,1}$ are only saturated if the gate-source voltage of $M_{s,2}$ is greater than the saturation voltages of $M_{s,1}$ and $M_{2,1}$. This results in two constraints, one where the current $N{\cdot}I$ is stored onto C_{s2} (resulting in $\Delta v_{s,2} = \sqrt{2}\Delta v_s$) and one where the current $-N{\cdot}I$ is stored onto C_{s2} (resulting in $\Delta v_{s,2} = 0$):

$$\text{II}: \quad \sqrt{2}\Delta v_s + \Delta v_2 < V_{Ts} + \sqrt{2}\Delta v_s \Leftrightarrow \Delta v_2 < V_{Ts}$$

$$\text{III}: \quad \sqrt{2}\Delta v_s + \Delta v_2 < V_{Ts}$$

The saturation voltages for the cascode transistors M_2 and M_3 is kept small as these do not contribute to the noise (see, [1]). This means that II is always fulfilled.

Constraint I and III set the limitations for the choise of the saturation voltage for the circuit. How these saturation voltages are to be selected will be discussed later when the power consumption for the SI-integrator is derived.

3.2. Power consumption

In this section the *SNR* for the SI-integrator is derived. This is used to find the power needed to ensure that the performance of the integrator is sufficient. In the following it is assumed that the $1/f$-noise is insignificant compared to the white noise. This assumption is reasonable as the SI-integrator internally performs correlated double sampling (CDS), i.e., it suppresses correlated errors at low frequencies.

The power spectral density of the white noise is equal to $S_{in}^w = \frac{2}{3}2KT\sum g_m$. Here K is Boltzmanns constant, T is the temperature and $\sum g_m$ is the sum of all transconductances for transistors that contribute to the noise. The noise bandwidth of the SI-integrator is $BWN = \frac{\omega_0}{2} = \frac{g_{ms}}{2C_s} > f_s$, where $C_s = C_{s1} = C_{s2}$. The power spectrum of the sample white noise in the frequency range $\left[-\frac{f_s}{2}; \frac{f_s}{2}\right]$ can then be found as:

$$P_{in}^w = S_{in}^w \cdot BWN = \frac{2}{3}\frac{KT}{C_s} g_{ms}^2 \sum \frac{g_m}{g_{ms}} \tag{2}$$

An expression for $\sum g_m$ will be derived later. Using a sinusoidal signal with an amplitude of $MSA{\cdot}I$ as input signal to the $\Sigma\Delta$-modulator the power of the input signal is $P_s = MSA^2\frac{I^2}{2}$. Using the fact that the signal band is $f_s = 2Rf_b$, where R is the oversampling factor then the *SNR* can now be found as:

$$SNR = \frac{P_s}{\frac{P_{in}^w}{R}} = MSA^2 \frac{I^2}{2\frac{2}{3}\frac{KT}{C_s} g_{ms}^2 \sum \frac{g_m}{g_{ms}}} R \tag{3}$$

Using $\frac{I^2}{g_{ms}^2} = \frac{\Delta v_s^2}{4}$ in (3), we get:

$$SNR = MSA^2 \frac{\Delta v_s^2}{\frac{16}{3}KT\sum \frac{g_m}{g_{ms}}} RC_s \tag{4}$$

Now, the factor $\sum \frac{g_m}{g_{ms}}$ is to be evaluated. As mentioned earlier the cascode transistors, $M_{2,x}$ and $M_{3,x}$, do not contribute to the noise therefore the saturation voltages of these were set to $0.1V$. Only $M_{s,1}$,$M_{s,2}$,$M_{4,1}$ and $M_{4,2}$ contribute to the noise. Therefore $\sum g_m = 2Ng_{ms} + 2Ng_{m4}$. However the noise from these transistors is sampled on both clock phases resulting in a doubling of the noise under the assumption that it is uncorrelated (white noise). Using $g_{ms} = \frac{2I}{\Delta v_s}$ and $g_{m4} = \frac{2I}{\Delta v_4}$ the factor $\frac{1}{\Delta v_s}\sum \frac{g_m}{g_{ms}}$ in (4) can be evaluated as:

$$\frac{1}{\Delta v_s}\sum \frac{g_m}{g_{ms}} = 4N\left(\frac{1}{\Delta v_s} + \frac{1}{\Delta v_4}\right) \tag{5}$$

Equation (4) and (5) show that the *SNR* is not dependent on the bias current I but only on the saturation voltages Δv_s and Δv_4.

The power consumption, P_{sup}, is now to be calculated. First consider:

$$\omega_0 = \frac{g_{ms}}{C_s} \Rightarrow g_{ms} = \omega_0 C_s = \frac{2I}{\Delta v_s} \Rightarrow I = \frac{\omega_0}{2} C_s \Delta v_s \tag{6}$$

The power consumption can now be calculated by multiplying I with V_{DD} (class A operation). From the capacitance (4) C_s can be found and the power consumption can be expressed as $P_{sup} = V_{DD}I = \frac{\omega_0}{2}C_s\Delta v_s$:

$$P_{sup} = \omega_0 SNR \frac{4N\frac{8}{3}KTV_{DD}}{MSA^2 R}\left(\frac{1}{\Delta v_s} + \frac{1}{\Delta v_4}\right) \tag{7}$$

Equation (7) can be used to minimize the power consumption within the constraints derived earlier.

The expression in (7) was derived for the integrator INT1 alone. For the $\Sigma\Delta$-modulator in figure 1 the input noise originates from INT1, DAC1 and IN1. Therefore (7) must be modified to also describe the noise from DAC1 and IN1. This is a tedious derivation and only the result will be presented here. The expression (7) will be modified:

$$P_{sup} = K_K\left(\frac{4N + D_s}{\Delta v_s} + \frac{4N + D_4}{\Delta v_4} + \frac{3}{4}\frac{MSA}{\Delta v_{in}}\right) \tag{8}$$

where K_K is the same factor as in (7). As can be seen from (8) the noise from DAC1 can be modeled by introducing some constants (D_s, D_4) in (7). DAC1 introduces noise and therefore more power must be used to obtain a certain *SNR*. Furthermore, the noise for the input is taken into account. Calculations showed that the noise from DAC1 could been modeled with $(D_s, D_4) = (1.75, 3.75)$. Earlier it was found that $N = 3$. This means that the noise from the integrator is much larger than the one for the DAC. Furthermore, the noise from the input resistor can be reduced by increasing the input voltage swing Δv_{in} (corresponds to increasing the input resistor in IN1 which then produces less noise current).

3.3. Optimization

Now, the constraints I, III and (7) (or (8)) can be used to minimize the power consumption. In this section the expression for the power consumption (7) is used but the results are also valid for (8).

Using a program such as MATLAB it is possible to find minimum power consumption within the boundaries given by the constraints. In a typical process there are process variations on, e.g., the thickness of the oxide T_{ox}, the threshold voltage V_T, etc. If the constraints I and III were used to determine the power consumption the process variations might, however, cause the circuit to malfunction as some transistors would operate in their linear region. The the threshold voltage (ε_T) can vary $\pm 30\%$ and the saturation voltage (ε_s) can vary $\pm 20\%$. To ensure that process variations will not reduce the yield it is necessary to take these into account.

The relative process variations for the threshold voltage, V_T, and the saturation voltages, Δv_s, is called ε_T and ε_s respectively. Now, the constraints I, III can be expressed as:

$$\text{I}_\varepsilon: \quad V_{Ts}(1+\varepsilon_T) + (\sqrt{2}\Delta v_s + \Delta v_3 + \Delta v_4)(1+\varepsilon_s) < V_{DD}$$

$$\text{III}_\varepsilon: \quad (\sqrt{2}\Delta v_s + \Delta v_2)(1+\varepsilon_s) < V_{Ts}(1+\varepsilon_T)$$

Ensuring that these two constraints are fulfilled for given process variations means that the saturation voltages must be chosen smaller than then nominal values which again means that more power must be used to ensure correct operation (see (7)). The constraints I_ε and III_ε make the determination of the optimal choise of the saturation voltages difficult.

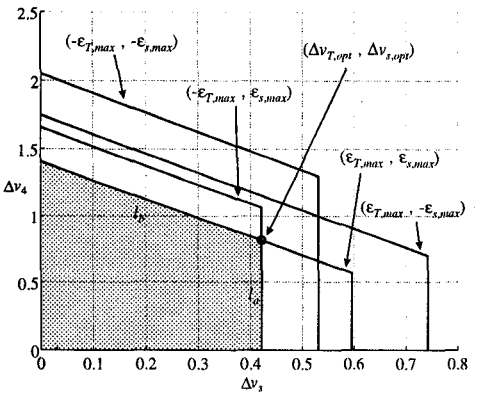

Figure 4. Boundaries.

Constraint III shows that Δv_s is limited to a value less than V_{Ts}. For large supply voltages this results in increased power consumption as can be seen from (7). Constraint I shows that Δv_s approaches zero when the supply voltage approaches V_{Ts}. This also results in increased power consumption as can be seen from (7). Therefore there exists an optimum supply voltage, that results in minimum power consumption, which for our circuit is $V_{DD} = 2.7V$. The threshold voltage is $V_T = 0.9V$.

The first step is to determine a set of limits, that limit the valid area for the saturation voltages. Four critical set of boundaries can be plotted for $(\pm\varepsilon_{T,max}, \pm\varepsilon_{s,max})$. This is illustrated in figure 4. Any set of values of $(\varepsilon_T, \varepsilon_s)$ within $(\pm\varepsilon_{T,max}, \pm\varepsilon_{s,max})$ will determine an area that encloses the shaded area in figure 4 due to the linear dependency between the saturation voltages and $(\varepsilon_T, \varepsilon_s)$.

To ensure that all transistors, for the given process variations $\varepsilon_{T,max}$ and $\varepsilon_{s,max}$, in the SI-integrator will operate in saturation the saturation voltages $(\Delta v_s, \Delta v_4)$ must therefore be chosen within the shaded area. Now, the power consumption (7) should be minimized within this area.

Finding the minima is a trivial mathematical problem which is left out for the reader. The optimal choise $(\Delta v_{s,opt}, \Delta v_{4,opt})$ is where the lines l_a and l_b in figure 4 intersect. This is marked by 'o'. The optimal choise $(\Delta v_{s,opt}, \Delta v_{4,opt})$ is the same for (8).

If process variation of $(\varepsilon_{T,max}, \varepsilon_{s,max})$=(0.3,0.3) have to be taken into account then the saturation voltages must be lowered which means that the quiescent current must be approximately 80 % larger than for the case $(\varepsilon_{T,max}, \varepsilon_{s,max})$=(0,0). Hence, a high yield is quite expensive in terms of power consumption.

As a compromise between high yield and low power consumption we choosed $(\varepsilon_T, \varepsilon_s) = (0.15, 0.10)$ which combined with (8) gives the optimal saturation voltages $(\Delta v_{s,opt}, \Delta v_{4,opt}) = (0.421V, 0.818V)$.

As discussed in section 3 high nonlinear settling error will degrade the performance of the $\Sigma\Delta$-modulator. The small signal settling error $\varepsilon = e^{-\omega_0 \frac{T}{2}}$ should be made as large as possible to reduce power consumption. Simulations showed that a small signal settling error should not exceed 0.5 %, otherwise it would show up as reduction of SNR. With $f_s = 1.08MHz$ this results in $\omega_0 = 5.72Ms^{-1}$. From (8) we get that the quiescent current is $I = 15.7\mu A$ and from (6) we get that $C_s = 6.5pF$.

The power consumption of the first integrator is approximately $254\mu W$. The total power consumption is approximately $600\mu W$.

4. SIMULATION RESULTS

In figure 5 the simulated output from the $\Sigma\Delta$-modulator with full scale input ($MSA = 0.7I$) is shown. The bottom curve represents the output spectrum of the $\Sigma\Delta$-modulator when ideal integrators are used. This results in a $SNR \approx 95dB$. The middle curve is the result of a simulation using the 'C++'-program to model the square law relationship for the transistors. This simulation shows that the quantization noise in the signal band increases and a DC-component appears. If the small signal settling error is reduced (N increased) then the middle curve approaches the ideal curve. The top curve is the same as the middle one with the exception that a noise source is added at the input to model the analog noise.

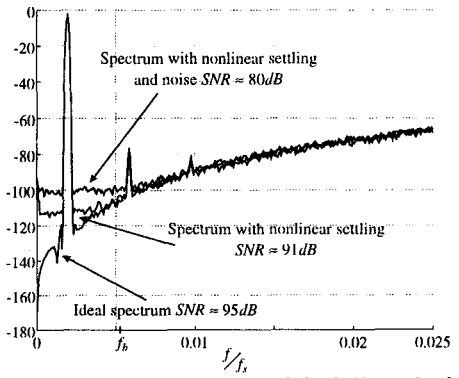

Figure 5. Output spectrum with full scale input.

All three simulations show a large 3rd harmonic component, even when linear integrators are used. This is due to the large input amplitude. If the amplitude of the input signal is lowered slightly this 3rd harmonic is reduced significantly.

The $\Sigma\Delta$-modulator is currently being fabricated in a $2.4\mu m$ CMOS process provided by MIETEC. Measurement results will be presented at the conference.

5. CONCLUSION

A 3rd order switched current-$\Sigma\Delta$-modulator is presented. The modulator is design to have a SNR of $80dB$ with a signal bandwidth of $f_b = 6kHz$ and an oversampling ratio of $R = 90$. The $NTF(z)$ for the modulator is designed as a 3rd order Butterworth highpass filter. Power consumption is lowered by using multiple input signals for reduction of the internal signal swings. The shaping of the noise from the 2nd and 3rd integrator is used to allow the noise power from these integrators to be increased by a factor of 2 and 4 respectively. This effectively lowers the power consumption by a factor of 1.71. The power consumption of the first integrator is $254\mu W$ and the total power consumption is $600\mu W$.

A new methology is presented that allows for optimization of SI circuits for minimum power consumption with respect to process tolerances. It is shown that a deviation of 30% in the threshold voltage and in the saturation voltages increases the power consumption by 80% in order to maintain the performance. The modulator is optimized for a supply voltage of $V_{DD} = 2.7V$.

6. ACKNOWLEDGEMENTS

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