1.5V CMOS Bootstrapped Dynamic Logic Circuit Techniques (BDLCT) Suitable for Low-Voltage Deep-Submicron CMOS VLSI for Implementing 482MHz Digital Quadrature Modulator and Adder

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Abstract

This paper reports 1.5V CMOS bootstrapped dynamic logic circuit techniques (BDLCT) suitable for low-voltage deep-submicron CMOS VLSI. Using BDLCT, the maximum operating frequency of a digital quadrature modulator is 482MHz at 5V and 68MHz at 1.5V. Compared to the circuit without BDLCT, the 12-bit delay time of in a 16-bit adder with BDLCT is improved by 56% at 1.5V.

Summary

Introduction

For next-generation VLSI circuits using deep-submicron CMOS technology, low supply voltage is the trend. Designing CMOS circuits using low supply voltage is a challenge. Recently, a 1.5V full-swing bootstrapped CMOS static driver circuit was reported [1]. To enhance the speed performance of CMOS dynamic logic circuits using low supply voltage is also important. A theoretical concept of a 1.5V CMOS dynamic logic circuit using the bootstrapped technique was reported [2]. In this paper, BDLCT suitable for low-voltage deep-submicron CMOS VLSI— the bootstrapped dynamic logic circuits and all-N-logic true-single-phase bootstrapped dynamic logic circuits have been used in an adder and a digital quadrature modulator.

1.5V BDLCT

Fig. 1 shows the 1.5V CMOS bootstrapped dynamic logic circuit techniques (BDLCT) in terms of (a) the 1.5V bootstrapped dynamic logic (BDL) circuit and (b) the 1.5V all-N-logic true-single-phase (TSP) BDL circuit.

(a) 1.5V BDL

As shown in Fig. 1(a), the BDL circuit is composed of the input stage and the bootstrapper stage. When the input to the bootstrapper circuit (V_{do}) is high, MPB is off and MN is on. Therefore, the output of it is pulled to ground. V_I is low, hence MP is on and V_b is pull high to V_{dd}. The bootstrap device MPC, which is made of a PMOS device with its source and drain tied together, stores an amount of $(V_{dd} - |V_{TP}|)C_{ox}WL$ charge. When the input to the bootstrapper (V_{do}) switches from high to low, MN turns off and MPB turns on. Meanwhile, V_I changes to high and MP turns off. Since the bootstrap device MPC turns off, the holes evacuated from MPC make V_b go up to exceed V_{dd}— the internal voltage overshoot. Therefore, the output (V_{out}) will also go up to surpass V_{dd}. The voltage overshoot at the output of the bootstrapper circuit enhances the driving capability of the next stage hence the speed performance can be improved.

(b) 1.5V TSP BDL

As shown in Fig.1(b), the 1.5V all-N-logic true-single-phase (TSP) BDL circuits: the n1-block and the n2-block have been created. The n1-block is identical to the BDL circuit except MCN1. When CK is low, MCN1 is off and the output of n1-block keeps its previous state. When CK is high, the function of the n1-block is the same as BDL. In a pipelined system using all-N-logic TSP BDL circuits, the n1-n2-n1-n2 arrangement is required. When the n1-blocks are in the precharge period, the n2-blocks are in the logic evaluation period. Therefore, the bootstrapped output of the n1-block may help drive the following n2-block. In the n2-block, when CK is high, MPD is off and the input N-logic is separated from V_{dd}. The V_{dp} node is predischarged to ground since MND is on. The output of n2-block V_{out2} keeps its previous state since both MCP2 and MN are off. When CK is low, MPD turns on and MND is off— the logic evaluation period. If all inputs to

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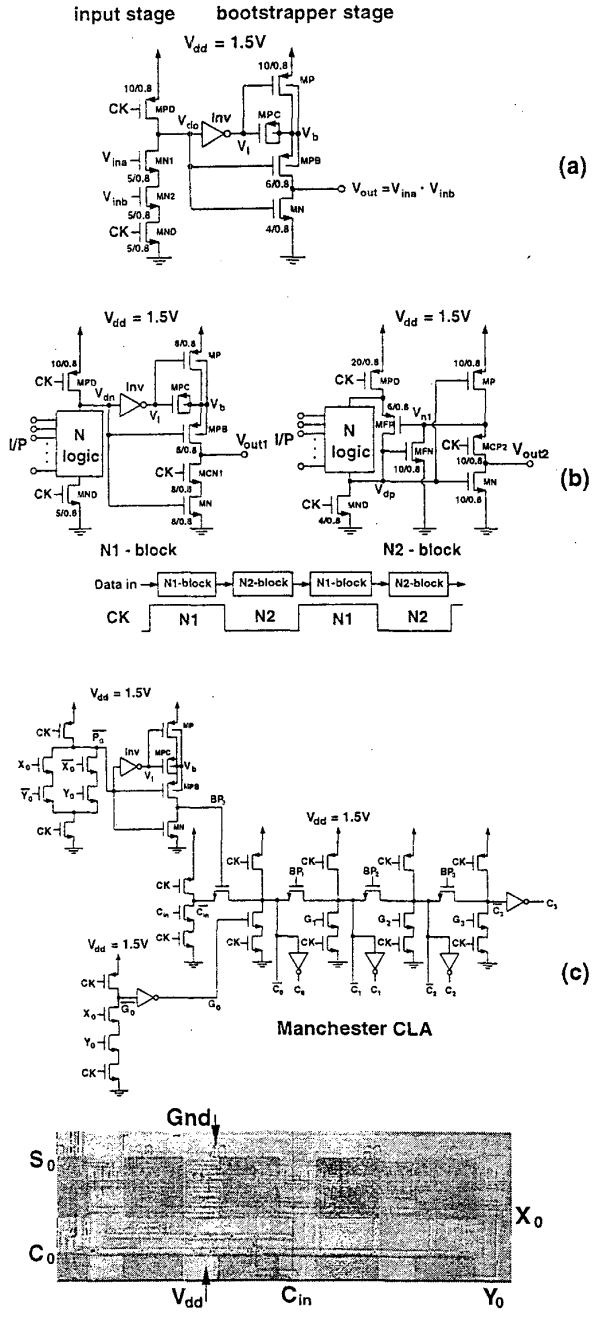

Fig. 1: The 1.5V CMOS bootstrapped dynamic logic circuit techniques (BDLCT) (a) the 1.5V BDL circuit and (b) the 1.5V all-N-logic true-single-phase (TSP) BDL circuit (c) the 1.5V adder circuit using the BDLCT (BDL circuit).

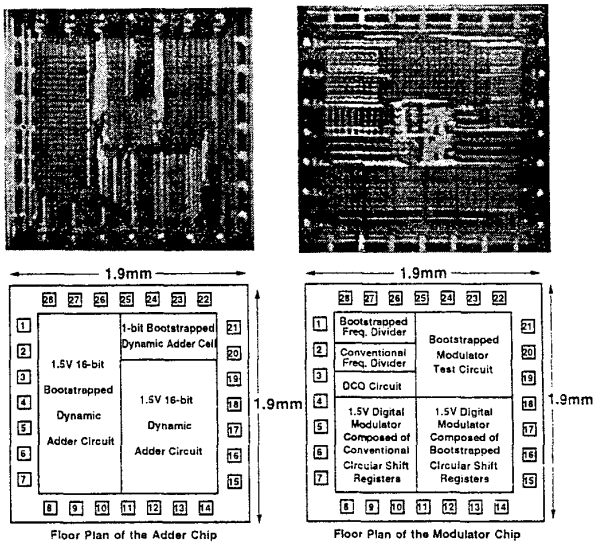

Fig. 2: Die photos of the adder and modulator chips using BDLCT and without.

the n2-block are high, V_{dp} is pulled high to $V_{dd} - V_{tn}(V_{dp})$, where $V_{tn}(V_{dp})$ is the threshold voltage of the NMOS device when its source voltage is V_{dp} due to the body effect of the NMOS device. Therefore, MN turns on and the output voltage V_{out2} is pulled low. The switching speed of V_{out2} and the stability of the V_{dp} level can be improved by raising the V_{dp} level by MFN and MFP. When MN turns on, MFN also turns on, which pulls the node voltage V_{n1} to ground. Thus, MFP turns on and V_{dp} is pulled high to V_{dd}.

Experimental Results

In order to show the effectiveness of BDLCT, a 1.5V adder circuit and a 1.5V digital quadrature modulator have been integrated using a standard 0.5μm CMOS technology.

(a) 1.5V Adder

Fig. 1(c) shows a 1.5V CMOS adder circuit using the Manchester carry look-ahead circuit with the BDL circuit. Die photos of the test chips are shown in Fig. 2. Fig. 3 shows the measured transient waveforms in the 16-bit 1.5V CMOS adder circuit with the Manchester carry look-ahead circuit (a) with BDLCT at 1.5V, (b) without BDLCT at 1.5V, (c) with BDLCT at 5V, (d) without BDLCT at 5V. With BDLCT, during the transient the pass transistor in the carry look-ahead circuit can turn on earlier. At 1.5V, with BDLCT the 12-bit delay in the 16-bit adder circuit is 27.6ns and without BDLCT, it is

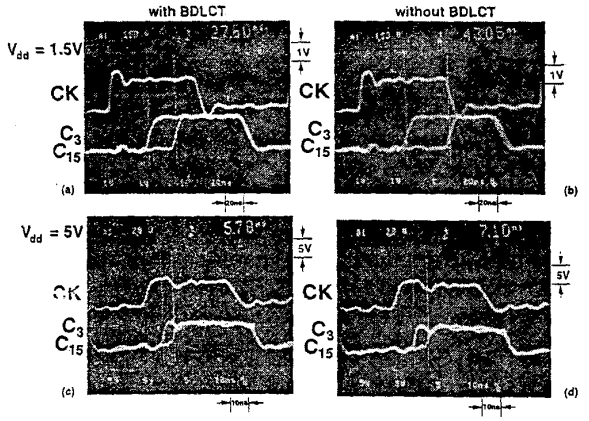

Fig. 3: Measured transient waveforms of the 16-bit CMOS adders with and without BDLCT (BDL) at 1.5V and 5V.

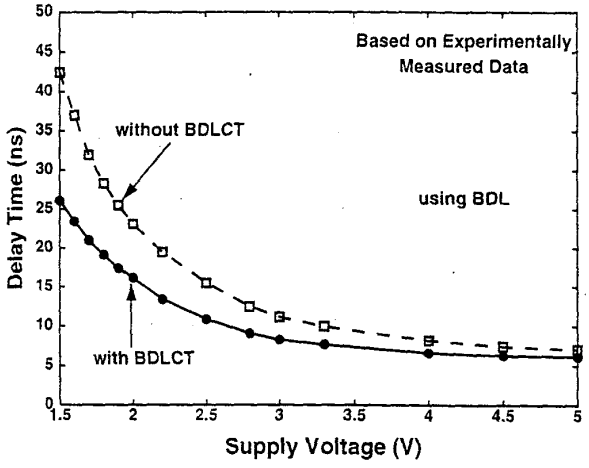

Fig. 4: Measured 12-bit delay time vs supply voltage in the 16-bit CMOS adder with and without BDLCT.

43.05ns. At 5V, with BDLCT it is 5.78ns and without BDLCT it is 7.1ns. Fig. 4 shows the measured 12-bit delay time vs the supply voltage of the 16-bit adder carry look-ahead circuit with and without BDLCT. At 5V, with BDLCT the propagation delay improves about 10%. At 1.5V, with BDLCT it improves 56%. Therefore, BDLCT is especially effective at low-voltage.

(b) 1.5V Quadrature Modulator

Fig. 5 shows the block diagram of a digital quadrature modulator [3]. It has an 8-stage circular shift register and 4 multiplexers to provide a four-bit digital output for representing a 5-level analog output. The 8-stage circular shift register is used to generate a set of eight adjacent outputs with various phases. The multiplexers are

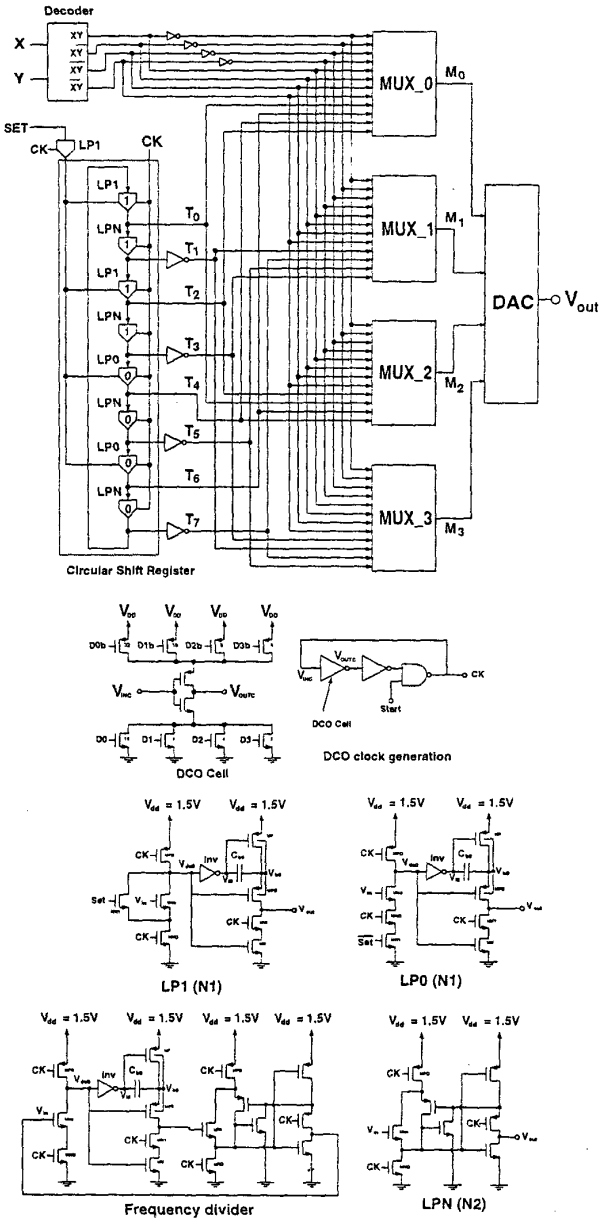

Fig. 5: Block diagram of the 1.5V CMOS quadrature modulator using BDLCT (all-N-logic TSP BDL).

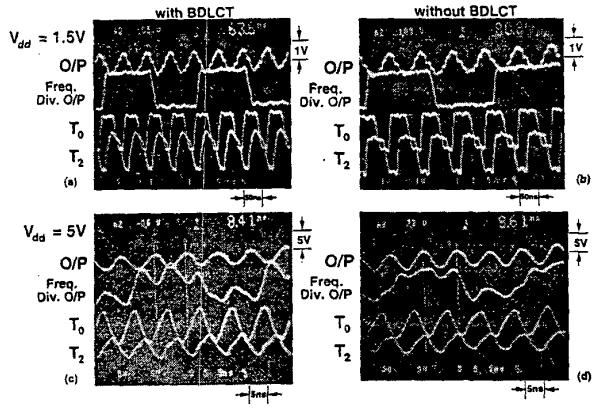

Fig. 6: Measured transient waveform of the CMOS quadrature modulator with and without BDLCT at 1.5V and 5V.

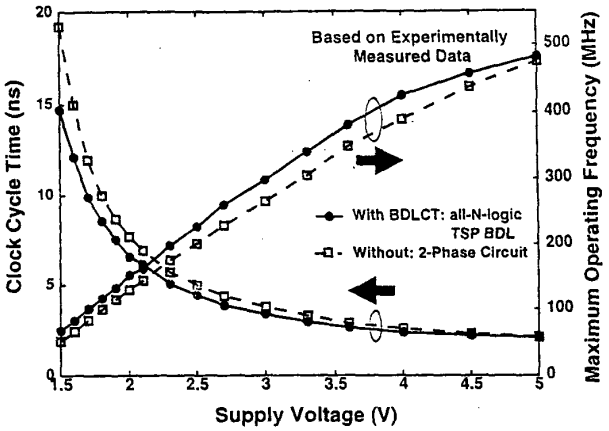

Fig. 7: Measured clock cycle time and maximum operating frequency vs supply voltage of the digital quadrature modulator with and without BDLCT.

used to select four appropriate outputs from the eight shift register outputs depending on the input baseband signals X and Y. In the circular shift registers, 'preset-to-1' (LP1), 'preset-to-0' (LP0), and 'no-preset' (LPN) latches based on all-N-logic TSP BDL circuits have been designed. In order to maximize the operation frequency, a digital controlled oscillator (DCO) is used to generate an on-chip clock. Fig. 6 shows the measured transient waveforms of the digital quadrature modulator using the all-N-logic TSP BDL circuits. (a) with BDLCT at 1.5V, (b) without BDLCT at 1.5V, (c) with BDLCT at 5V, (d) without BDLCT at 5V. At 1.5V, with BDLCT the modulator works at a minimum clock cyle time of 15.9ns and without BDLCT it works at 20.2ns. At 5V, with BDLCT it works at a minimum clock cycle time of 2.1ns and without BDLCT it works at 2.15ns. With BDLCT, it works at a faster speed. Fig. 7 shows the clock cycle time and the maximum operating frequency vs the supply voltage of the digital quadrature modulator with and without BDLCT. At 5V, the digital quadrature modulator works at a maximum operating frequency of close to 500MHz. With BDLCT, at 5V, the maximum operating frequency is slightly higher. As the supply voltage decreases, the maximum operating frequency decreases. At 1.5V, with BDLCT its maximum operating frequency is 68MHz, which is 27% faster than that without BDLCT.

Discussion

The BDLCT reported in this paper is especially useful for low-voltage application. From experimental measurement, it can work at a supply voltage of 1.3V using the conventional I/O pad driver circuits. Based on the SPICE simulation, it can work even at a supply voltage of 1V. Considering the CMOS BDL circuit with a serial fan-in of 2 and a fan-out of 4, the 1V CMOS BDL circuit has a speed enhancement of 1.8 times.

Acknowledgments

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References

[1] J. H. Lou and J. B. Kuo, "A 1.5V Full-Swing Bootstrapped CMOS Large Capacitive-Load Driver Circuit Suitable for Low-Voltage CMOS VLSI", *IEEE J. Solid-State Circuits*, Vol. 32, No. 1, pp. 119-121, Jan. 1997.

[2] J. H. Lou and J. B. Kuo, "1.5V CMOS and BiCMOS Bootstrapped Dynamic Logic (BDL) Circuits using a CMOS Bootstrapper Circuit", *Tech. Digest of Symp. VLSI TSA, Taipei*, June 1997.

[3] P. F. Lin, J. H. Lou, and J. B. Kuo, "A CMOS Quadrature Modulator for Wireless Communication IC," *IEEE Trans. Circuits and Systems-I*, Vol. 44, No. 6, pp. 559-561, June 1997.