Interactive Verification of Switched-Current Sigma-Delta Modulators

J.M. de la Rosa (1), A. Kaiser (2) and B. Pérez-Verdú (1)

(1) IMSE-CNM
Edificio CNM-CICA
41012 Sevilla, Spain
Tel. +34-5-4239923 Fax. +34-5-4231832
E-mail: jrosa@imse.cnm.es

(2) IEMN-ISEN, UMR CNRS 9929
41, Boulevard Vauban,
F - 59046 Lille cedex, France
Tel. +33 3 20 30 40 50 Fax. +33 3 20 30 40 51
E-mail: Andreas.Kaiser@isen.fr

Abstract

A simulation tool named SDSI, specifically suited for the simulation of switched-current (SI) sigma-delta data converters, has been developed in an interactive design environment. The tool exploits the sampled-data nature of the circuits and provides several levels of hierarchy for the models. High level behavioural models are suited for initial system-level simulations and specification of building blocks. Lower level models, which take into account non-linear effects and eventually full SPICE level transistor models, are suited for bottom-up verification of circuits after the design of the building-blocks. There are no restrictions on the interoperability of both types of models. Very fast simulation times are achieved thanks to the sampled-data simulation approach, making the tool appropriate for the extensive analysis of sigma-delta modulators. The tool has been used to check the performance of a SI bandpass sigma-delta modulator fabricated in a 0.8μm CMOS technology. Experimental results validate this approach to the verification of SI sigma-delta modulators[1].

1. Introduction

The analysis of sampled-data circuits such as sigma-delta modulators needs to be done in time-domain. Transistor-level simulations with SPICE-like simulators are not adequate due to excessively long simulation times. Discrete-time approaches have been proposed, both for switched-capacitor (SC) and SI circuits [1][2]. While simulators with a reasonable user-interface are available for SC circuits [1], nothing does yet exist for SI circuits. This paper describes a flexible approach for the implementation of such a SI simulator. It is based on an existing simulation environment, MATLAB/ SIMULINK. As will be shown, this environment can easily be adapted to our SI circuit-modelling approach. The benefits from MATLAB/SIMULINK are a reduced effort for the graphical user interface (GUI) implementation, high flexibility for the extension of the model library and extensive signal processing capabilities for the analysis of simulation results. The tool is also widely used, both in academia and industry.

2. Principle of discrete-time simulation

In switched-current circuits we can identify on every clock-phase distinct sub-circuits composed of one cell acquiring a new current and one or more cells restoring their memorised current. The transistor-level schematic diagram of one such subcircuit is shown in Fig. 1. The aim of the simulation is to determine the voltage stored on capacitor C_{g3} at the end of the clock phase ϕ_2. Obviously, this voltage is a function of the initial values of the voltages across the capacitors C_{g1}, C_{g2} and C_{g3} an depends on the duration of the clock phase ϕ_2. The precise form of the transient appearing on the gate of M_{m3} during ϕ_2 is however not important for the global operation of the circuit. Only the final value is sampled and needs to be determined precisely.

A minimal linear equivalent circuit for this subcircuit is shown in Fig. 2. Restoring cells are modelled by a current source in parallel with an output conductance, while the acquiring cell is simply modelled by the memory transistors transconductance in parallel with its output conductance. Finite switch conductances are also included. This example assumes complete settling and therefore no dynamic effects are modeled. In practice, the effect of incomplete settling is precalculated and incorporated as errors in the static model. The effectively acquired signal

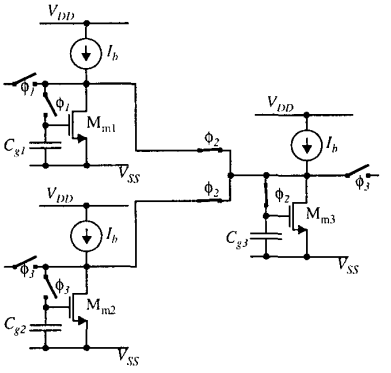

Fig. 1. Typical Subcircuit to be Modelled.

[1]This work has been partially supported by the Spanish CICYT Project TIC 97-0580.

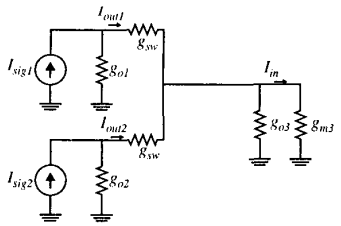

Fig. 2. Low-Frequency Small-Signal Equivalent Circuit for Fig. 1.

current is the current I_{in} flowing through the conductance of value g_{m3}.

This topology can easily be transposed into a block-level schematic diagram in the SIMULINK environment as Fig. 3 shows. Each block is evaluated on its respective clock phase based on the equivalent schematic of Fig. 2. The necessary parameters for each input are the values of the output current and the output conductance of the driving cell. The block interconnections in the current mode domain have been defined as vector quantities, making it possible to propagate these parameters from the restoring cells to the acquiring cell.

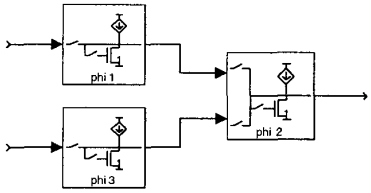

Fig. 3. SIMULINK Diagram for the Circuit of Fig. 1.

In addition to current memories, the basic library shown in Fig. 4, includes voltage-to-current converters, current-to-voltage converters, a comparator (1-bit A/D), 1-bit and 1.5-bit D-to-A converters and a current mirror. All models are written in C and integrated as dynamically linked libraries in the MATLAB/SIMULINK environment.

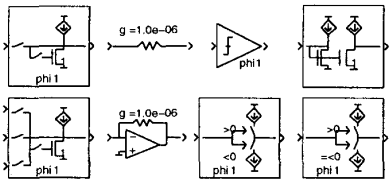

Fig. 4. Basic Switched-Current Library.

3. Low-level model implementation

A more detailed description of SI circuits can be given using the low-level library. A large number of memory cells and higher hierarchical level blocks have been included in this library. We will focus on the description of a fully differential Regulated-Folded Cascode (RFC) memory cell. This model can be extended to other blocks. The schematic of this cell is shown in Fig. 5(a). The differential mode input impedance is given by $g_{id} = g_m A$, where g_m is the differential mode memory transistor transconductance and A is the gain of the local feedback made by transistors $M_{cp,n}$ and $M_{rp,n}$. Fig. 5(b) shows a block-level schematic diagram in the SIMULINK environment showing the connection of two RFC cells in series. On clock phase ϕ_1, cell1 is on the restoring phase and cell2 is on the acquiring phase. The equivalent circuit used to compute the current acquired by cell2 is shown in Fig. 5(c). The differential mode memory transistor drain current, $I_D = I_{D_p} - I_{D_n}$ and the gate-source voltage, $V_g = V_{gsp} - V_{gsn}$ are state variables which need to be computed to calculate the final memorized current at the end of ϕ_1. The first step of the analysis is to determine the steady state of I_{D_2}, given by

$$I_{D_2}(nT_s) = \frac{1}{1 + g_o/g_{id}}\left(\frac{g_{sw}}{g_{sw} + g_{out}}(-I_{D_1}^{final}((n-1/2)T_s))\right) \quad (1)$$

Where $g_o = \frac{g_{out}g_{sw}}{(g_{out} + g_{sw})} + g_{out}$ and

$g_{out} = g_{ds_{bias}} + (g_{ds_p} + g_{ds_n})/2$.

The above expression is right only if the memory cell reachs the steady state before the end of the sampling time, nT_s. This is not the case of most of SI circuit applications where high sampling frequencies are required. For this reason we include an incomplete settling time model. A first order approach is considered. The equivalent circuit is shown in Fig. 5(c) and V_g is obtained by solving

$$C_g \frac{d}{dt} V_g(t) + f(V_g(t)) = I_{D_2}(nT_s) \quad (2)$$

for the initial condition $V_g = V_g(n-1)$. The function $f(V_g)$ can be chosen by the user. In the linear case, $f(V_g) = g_m I_D$. In the non-linear case two different approaches for $f(V_g)$ are considered. One consists of a non-linear differential transconductance $f(V_g) = g_m(I_D)V_g$ as [3], and the other one consists of using the first order model of the MOSFET in saturation [4].

The final actual gate voltage, $V_g^{final}(nT_s)$, is subject to perturbation due to charge-injection and noise. Charge injected by the switch transistor on the memory transistor gate introduces an additional error (ΔV_q) at the end of the sampling phase modelled as shown in [2]. Finally, a RMS noise sample, ΔV_n of the overall power is computed and added to V_g yielding

$$V_g^{final}(nT_s) = V_g(nT_s) + \Delta V_q + \Delta V_n \quad (3)$$

The differential drain current memorized at the end of the

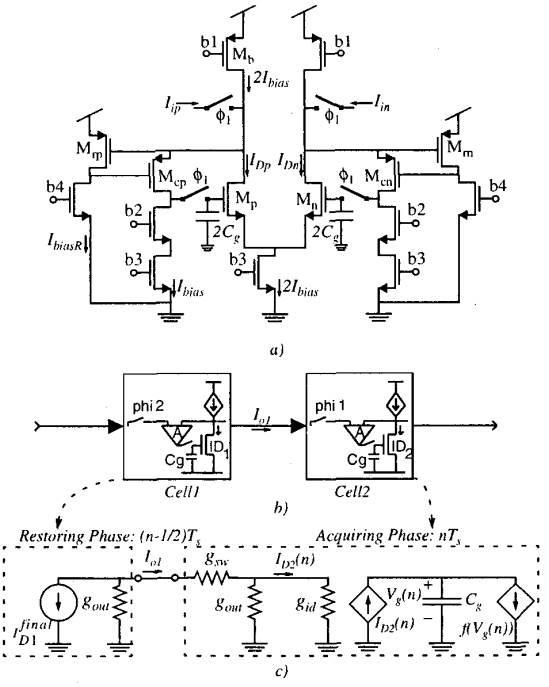

Fig. 5. Lowlevel Model of a RFC Memory Cell. a) Schematic of the Cell. b) Block Diagram of Two Memory Cells in Series in SIMULINK. c) Equivalent Circuit Used in the Model.

sampling phase, $I_{D_2}^{final}(nT_s)$ is computed as

$$I_{D_2}^{final}(nT_s) = f(V_g^{final}(nT_s)) \tag{4}$$

Our model limits $\left|I_{D_2}^{final}(nT_s)\right| < 2I_{bias}$ in order to prevent the calculation of unphysical circuit responses.

The model of this cell in the restoring phase will be a current source of value $I_{D_2}^{final}(nT_s)$ in parallel with g_{out}.

4. Extension to non-linear input conductance

The model used for the RFC memory cell in the above section assumed linear variations around the quiescent point. This assumption is only valid for small changes of the input current with respect to the bias current. For large changes, one of the transistors forming the input feedback loop may leave the saturation region, causing a strong change in the differential input voltage, V_{id} and increasing the input impedance of the memory cell.

This signal dependent input impedance has been introduced into the model for the RFC memory cell through a non-linear resistor as Fig. 6 shows. Using this model, an interactive procedure is needed to solve the stationary

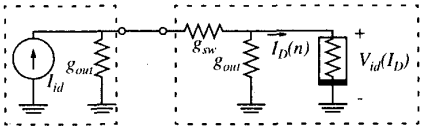

Fig. 6. Model for the Signal Dependence Input Impedance.

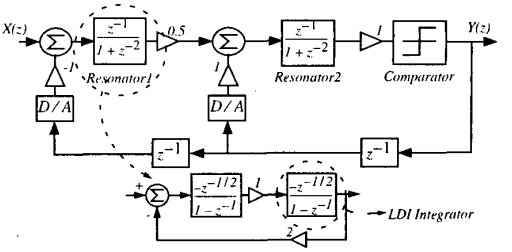

Fig. 7. Block Diagram of the Modulator.

value of I_D. The starting point is the ideal input current, $I_D = I_{id}$. This current is used to evaluate V_{id}. Knowing V_{id}, currents flowing through output conductances are computed and the new I_D is calculated. The procedure is then continued until convergence is obtained. Once this current is determined, the final value at the end of the acquiring phase, $I_D^{final}(nT_s)$ is computed in the same way as the linear case.

5. Application to a SI 4th Order Bandpass ΣΔ Modulator

The tool presented in the above sections has been used to analyse the performance of a SI 4th order bandpass ΣΔ modulator [5]. The block diagram of this modulator is shown in Fig. 7. LDI integrators are based on the memory cell shown in Fig. 5(a). Because of the input feedback loop, this memory cell exhibits a third-order dynamics. It can be shown that the current source called I_{biasR} (see Fig. 5(a)) must be taken as large as possible in order to obtain an overdamped settling response. However, large values of I_{biasR} may force some transistors to leave the saturation region, thus causing a non-linear dependence of V_{id} on the input signal. This has been validated by a DC HSPICE simulation. Fig. 8 plots V_{id} vs. I_{id} for different values of I_{biasR}. The differential input range is limited to $2I_{bias}$ being I_{bias}=212μA. It can be seen that the linear range decreases with I_{biasR}. This behaviour of the input voltage has been included into the model as a polynomial function given by

$$V_{id} = r_1 I_D + r_3 I_D^3 \tag{5}$$

Where r_1 and r_3 were extracted from DC nominal

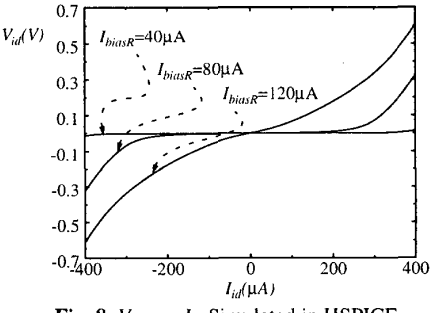

Fig. 8. V_{id} vs. I_{id} Simulated in HSPICE.

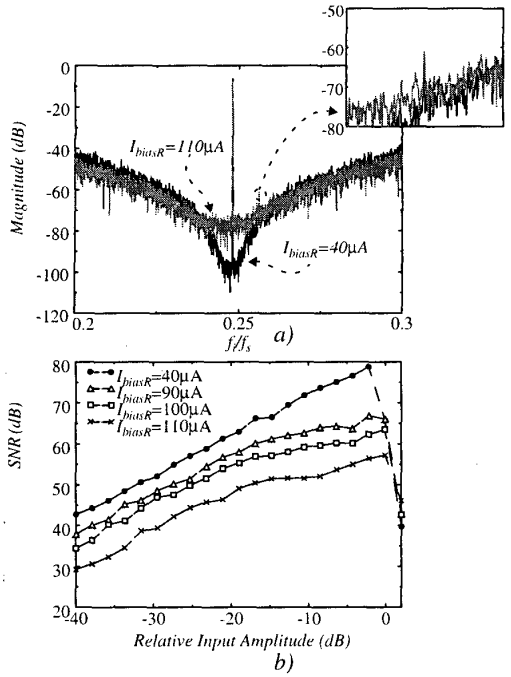

Fig. 9. Simulated Degradation with Non-Linear Input Impedance. a) Output Spectra for -6dB Input Amplitude@124kHz Signal Frequency. b) SNR vs. Relative Amplitude for an Input Single Tone of 124kHz and a Bandwidth of 1.5kHz.

HSPICE simulations for different values of I_{biasR}. The modulator was simulated including this error. Thermal noise was also included in the simulation by adding the input equivalent noise to the first memory cell gate voltage. The sampling frequency was 500kHz, being the settling error neglected. The input signal was a single tone of 124kHz frequency and an amplitude of -6dB relative to D/A reference current, I_{ref} = 50μA.

Fig. 9(a) shows two output spectra for different values of I_{biasR}. The quantization noise in the signal band increases due to the linear error, $r_1 g_{out}$ and the non-linear error, $r_3 g_{out} I_D^2$. The linear error term produces a shift of the notch frequency [6]. On the other hand, the non-linear error term produces intermodulation such that the third harmonic of the input signal appears at $f_s/4 + 3(f_s/4 - f_{signal})$. Hence, the presence of such outband tone is a clear manifestation of non-linearity and should hence becomes more strong as I_{biasR} increases. Fig. 9(b) plots the SNR vs. relative input signal amplitude for different I_{biasR} values. It shows that SNR degradation increases as I_{biasR} increases, and that degradation is larger for large input amplitudes - a consequence of the fact that non-linear error depends on the input signal amplitude. For large values of I_{biasR} the linear error dominates the non-linear error, and the degradation is the same in all the input range.

This phenomenon has been experimentally validated

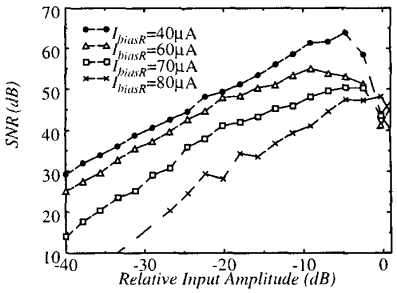

Fig. 10. Measured SNR vs. Relative Amplitude for an Input Single Tone of 122kHz and a Bandwidth of 1.5kHz.

with a prototype fabricated in a 0.8μm CMOS technology [5]. The chip was tested at 500kHz clock frequency, such that the settling error can be neglected. Fig. 10 plots the measured SNR vs. relative input amplitude for different I_{biasR} values showing similar degradation to that obtained by simulation. HSPICE simulations using MONTE-CARLO analysis confirm that the ranges of linearity for the input impedance are reduced for all I_{biasR} values. An improvement of the tool should evaluate the worst-case of this non-linear impedance taking into account mismatches in the differential cell.

6. Conclusions

This paper described the discrete-time modelling of SI circuits in an interactive simulation environment. Both high-level models for initial circuit verification and low-level models for precise characterization are included in the simulation libraries. The tools have been used to analyse the performance of a SI Bandpass ΣΔ modulator. Experimental measurements validate this approach to the verification of SI ΣΔ Modulators.

References

[1] F.Medeiro, B. Pérez Verdú, A. Rodríguez Vázquez,and J.L. Huertas, "A Vertically-Integrated Tool for Automated Design of ΣΔ Modulators". *IEEE Journal of Solid-State Circuits*, Vol. 30, pp. 762-772, July 1995.

[2] P. N'Goran, A. Kaiser, "A building block approach to the design and simulation of complex current-memory circuits", *Analog Integrated Circuits and Signal Processing*, pp.189-199, June 1995.

[3] P.J. Crawley and G.W. Roberts, "Predicting Harmonic Distortion in Switched-Current Memory Circuits", *IEEE trans. Circuits and Systems II*, pp. 73-86, February 1994.

[4] D.B. Nairn, "Analytic Response of MOS Current Copiers", *IEEE Transactions on Circuits and Systems II*,Vol. 40, pp. 133-135, February 1993.

[5] J.M. de la Rosa, B. Pérez-Verdú, F. Medeiro and A. Rodríguez-Vázquez, "A 2.5MHz 55dB Switched-Current BandPass ΣΔ Modulator for AM Signal Conversion", *Proc. of ESSCIRC'97*, pp. 156-159, 1997.

[6] J.M. de la Rosa, B. Pérez-Verdú, F. Medeiro and A. Rodríguez-Vázquez, "Quantization Noise Shaping Degradation in Switched-Current BandPass Sigma-Delta Modulators", *Proc. of DCIS'97*, pp.247-252, 1997.