

# RAPID - Retargetability for Reusability of Application-Driven Quadrature D/A Interface Block Design

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## Abstract

This paper describes ESPRIT 29648, concerning the development of an advanced methodology for the design of a mixed-signal application-driven quadrature D/A interface sub-system, aiming at its reusability by a retargeting procedure with minimal changes to their structural sub-blocks. The methodology will be demonstrated, first, by developing a nominal design platform for the implementation in 0.35  $\mu\text{m}$  double-poly CMOS technology of a Quadrature D/A Interface Block Design for the GSM standard, and, then, by an automatic retargeting in an evolutionary technology through the realization of a silicon prototype in 0.25  $\mu\text{m}$  CMOS.

## 1. Introduction

World-wide semiconductor market trends indicate a rapid increase of chips containing both analog and digital functionality, obtained at the expense of chips which contain purely analog functionality and also of chips which contain purely digital functionality [1-3]. It is generally accepted that such increased functionality is playing a bigger roll in the way integrated circuits are designed, and thereby making designers more concerned with integrated system solutions combining analog and digital functions and signals. In order to provide such increased functionality and combined use of analog and digital signals, it is necessary to develop the electronic circuitry that provides the appropriate analog-digital interface. Thus, in a not too distant future, the integration of complete systems on a chip will be achieved by assembling a variety of high functionality blocks, from powerful CPU and DSP cores to complex analog-digital blocks, as depicted in fig. 1.

In order to satisfy the need to reduce product development cycles and improve timely availability to the market in a world subject to a fast pace of technology evolution towards system level integration it is inevitably required that a significant increase of productivity is achieved in the design of complex mixed-signal interface functions. This can be provided by retargetable analog-digital blocks that allow easy

re-usability for different technology environments and application requirements. This paper describes the methodology for designing such retargetable application-driven analog-digital blocks, discusses its main ingredients and requirements of the supporting computer-based tools, and illustrates its application in practical industry designs.

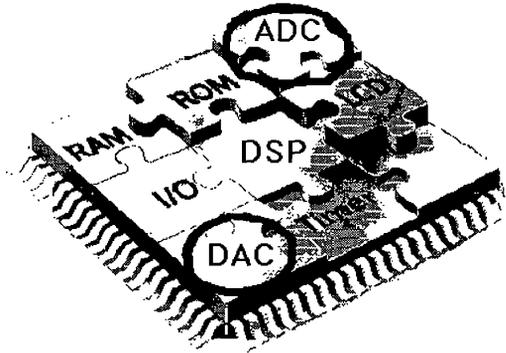


Fig. 1: System-level integration in mixed-signal VLSI chips will be achieved using high-functionality analog-digital blocks together with high-density digital cores.

## 2. Analog-Digital Interface requirements

Analog-digital blocks found in complex mixed-signal VLSI are needed to interface the digital processing engines at their heart to the physical sources of analog signals [4-6]. This can be the case of input and output in audio applications, sensors and actuators in micro systems, reading/writing channels for storage applications - disk or tape, and even complete transceiver interfaces for radio transmission. In this project a quadrature D/A interface was adopted, in order to illustrate the retargetable methodology.

In figure 2, a mixed-signal interface block, providing a two fully-differential channels in quadrature phase ( $90^\circ$  phase shift) between the input digital ports and the output analog ports [7], is illustrated. Each channel is formed by a digital processing unit for signal shaping

and interpolation, a digital-to-analog conversion function employing current-based circuit techniques and then a continuous-time filter, which also provides the embedded current to voltage conversion. An additional calibration unit is employed to adjust the unavoidable offsets and mismatches between the both channels. In order to control the functionality and calibration of the complete block, a control unit is also included. Again in this example we can notice the true multi-functional nature of a block design comprising digital signal processing, digital-to-analog conversion, analog continuous-time filtering and even functions of error correction and calibration.

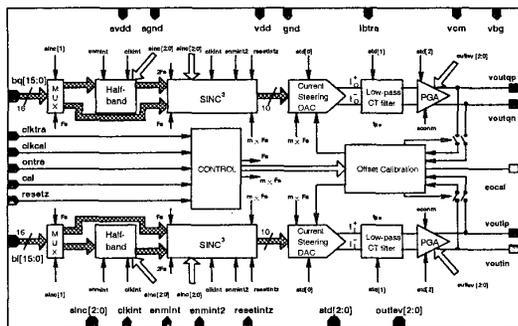


Fig. 2: Block diagram of a mixed-signal block providing full interfacing functionality between a quadrature digital port and a quadrature analog port.

The above example outlines that mixed-signal interface blocks are very demanding in terms of the knowledge that is needed for their development. Firstly, it is important to have knowledge about the system application and relevant signals, without which it will not be possible to define the block functionality and even its electrical requirements. Once the system is known, it is also important to have a knowledge about the circuits for signal processing and conversion that can be used inside those blocks. These can include continuous-time and sampled-data filters - both analog and digital, signal conditioning circuits, again both analog and digital, and also analog-to-digital and digital-to-analog conversion functions. Thirdly, it is also important to have the knowledge that allows the development of the circuit components for integrated circuit realization, such as operational amplifiers, comparators, voltage references and current references. Finally, it is important to know how to provide the physical implementation of all those components in a fully verified database that is submitted for fabrication.

### 3 Retargetable Block Design

#### Retargetable block model

The fundamental concept for the design of retargetable blocks is illustrated in figure 3. After carrying-out a

traditional top-down design, corresponding to the left hand side of the illustration, the results will be in the form of separate schematics and layout cells for the circuit components and functional building blocks. In addition to this basic circuit information, there may also be experimental results of prototype chip characterization to validate the design solutions and possibly establishing their practical limits of effectiveness. We may now consider that all such information at schematic, layout and silicon levels can be embedded into a single block model. Around each block model we can define a range of specifications which allow the fast retargetability of the model. Therefore, whenever a new set of specifications is defined within such range, the block model provides an important central platform from where the new block design can be quickly accomplished. In a CAD environment for retargetable block design, traditional libraries are now replaced by “knowledge” libraries containing objects that always need some retuning design in order to meet new specifications.

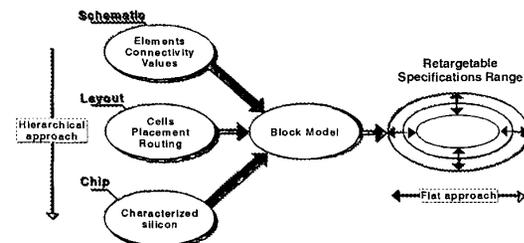


Fig. 3: The concept of block model embeds information from electric schematics, physical layouts and even experimental characterization of a design.

#### Design flow for retargetability

The design flow to carryout the retargeting of a block is illustrated in figure 4. First, it considers the validation of a new set of specifications against the range of specifications for which the block has been previously designed. The design is carried-out only if the specifications are validated, meaning that the new set of specifications falls within the range of the retargetability of the block. In this case, a set of priorities are initially defined in order to define the sequence of specifications that should be accomplished first by the constituting functional building blocks according to their inherent adaptability and suitability for integrated circuit realization. Once such sequence is defined, the design process consists of tuning the existing designs to the new specifications. Then, after tuning the functional building blocks, there is a process of tuning the circuit component cells within each functional block and which consists also of changing only the parts of the circuit components that need to be changed. Suppose, for example, the retargeting of a block which is needed to increase the driving capability

of an operational amplifier. It is clear that it would not be necessary to re-design the whole operational amplifier again, but simply to carryout a much smaller intervention in the output stage, may be by adjusting its biasing level or re-sizing the dimensions of its constituting transistors. After the tuning of all the functional building blocks and circuit components has been completed, a validation step takes place to verify the correctness of the new performance characteristics and then proceed to the final processing and verifications.

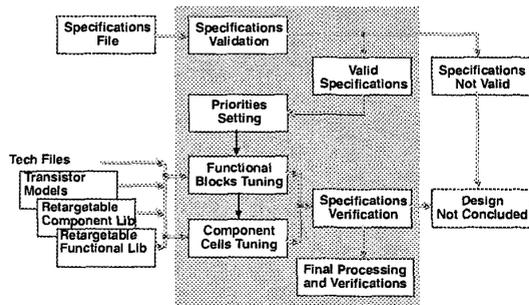


Fig. 4: Retargetable block design flow.

### Key features of designing for retargetability

The required features for design quality and productivity in the above environment are multiple. First, it is necessary to ensure that the trading-off of specifications of the multiple functional blocks inside the block converges and that in such a process the system partitioning is optimized for implementation. Second, it is necessary to ensure that the block model is easily adapted to a technology evolution by using circuit component design methodologies which reduce the technology dependency. Third, it is required to ensure that the retargeted design achieves an effective use of silicon area because, in volume production, the area of the chip is paramount for determining the final production cost. This can be assured by maximizing the layout regularity, optimizing the component aspect ratios or even by establishing careful floor planning for the block. Finally, the routing density and routing area of the block should also be minimized as this represents an overhead area which is not directly needed for the functionality that needs to be delivered and, therefore, the higher the overall routing area, the higher the production cost of the circuit. This can be assured by a detailed analysis of the route-path characteristics and the use of simplifying routing techniques.

### Design productivity

The productivity gains that can be achieved by using a methodology based on retargetable block designs is

illustrated in Table 1, both for different technologies and for different specs.

Table 1: Illustration of the productivity gains achieved through retargetable block design methodologies.

Block Design	Analysis	Tech File	Schematics	Design Time
Specs A, 1.2 $\mu\text{m}$	New	New	New	8 months
Specs B, 1.2 $\mu\text{m}$	---	---	Modified	3 weeks
Specs A, 0.7 $\mu\text{m}$	---	New	Modified	4 weeks
Specs C, 0.5 $\mu\text{m}$	---	New	Modified	2 weeks

## 4 Design Automation towards Retargetability

The methodology described above represents the design flow followed by experimented designers in an industrial environment. Besides the definition of such methodology the goal of RAPID (EP-29648) is to developed a design automation mechanism, embedded on available commercial tools, to perform the retargeting of mixed-signal ICs between different technologies in an industrial design environment. The a design automation mechanism is being build above Cadence DF II, making use of design facilities such as P-Cells structures, SKILL language and also some external tools, e.g., optimization mechanism. Next, the information flow, illustrated on figure 5, on such a design automation mechanism is described, outlining, the knowledge/data acquisition, the retargeting mechanism and the output data.

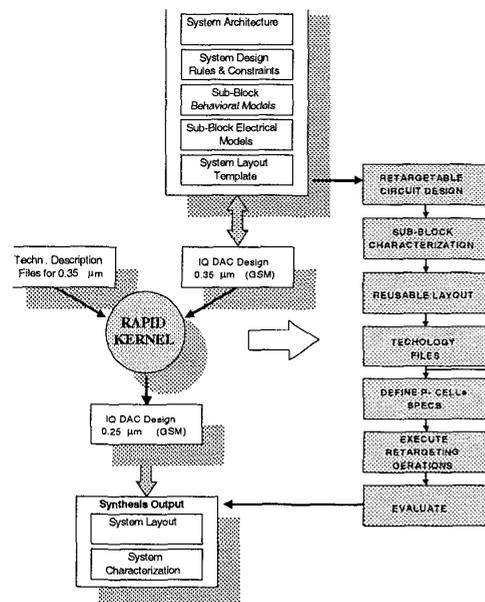


Fig. 5: Design Automation Mechanism (Information Flow)

### Knowledge Acquisition

The first step on such a design process corresponds to the knowledge acquisition to support the retargeting mechanism, this consist of the original IC design description made for a specific technology, e.g., AMS 0.35 $\mu$ m. This description should be made fully hierarchically, including high-level models of the complete system, made in SPECTRE HDL, Low-level models, made in SPECTRE, system design rules and constraints, hardcoded, and the complete layout described in terms of P-Cells structures. From this initial design and technology descriptions new IC should be automatically derived.

### Input Specs

For such a process focusing on the retargeting for different technologies, having very same high-level performance specs, e.g., GSM standard, the required input are mainly the new technology files, e.g., AMS 0.25 $\mu$ m.

### Retargeting Mechanism

Based on the original Layout and on the new technological files a circuit extraction is performed, so that all sub-blocks performance can be evaluated at electrical level and the full system can be evaluated by behavioral simulation using, e.g., SPECTRE, HSPICE and SPECTRE-HDL. Next, based on the performance evaluation results, on the desired system performance and on the sub-block design constraints, the P-Cells specs and corrections required, on the new technology, for each sub-block are defined, within acceptable limits. Then, based on the system layout template execute sub-block retargeting operations by either changing component sizes using SKILL, as illustrated in fig. 6, or polarization sources. Finally, readjust all system layout according to sub-blocks geometry changes.

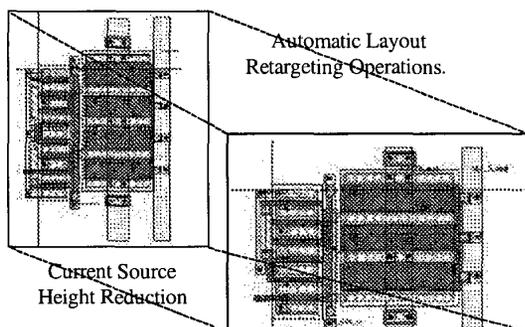


Fig. 6: Current Source Retargeting Operation.

### Output Data

The output data on such a process includes the mixed-signal IC layout on the new technology, as well as, the system characterization based on multi-level simulation as specified by the retargeting mechanism above.

## 5 Example from Industry Practice

### Quadrature D/A RF interface

The mixed-signal block discussed earlier in this paper, illustrated in fig. 2, and which is required to provide the interface between two digital signals in quadrature, one in-phase and the other 90° out-of-phase, and the analog signals that interface an RF transmitter for wireless applications, was selected as an example of industry practice.

The above block has been retargeted for different applications, all for wireless communications, and which have different requirements for the digital input data, baseband frequency band, sampling frequency and even out-of-band image rejection. Two examples of the resulting layouts of such block with retargeted characteristics are illustrated in Figure 7. First, in Figure 7 (a), we can see the I&Q D/A interface for the Japanese PHS system, with 25 kHz baseband, and which required an 8-fold interpolation of the input digital signal, an 8-bits D/A converter and a 2nd order active-RC filter with nominal 400 kHz cut-off frequency. In Figure 7 (b) we can see the layout of the same I&Q D/A interface architecture retargeted for a GSM application, with 100 kHz baseband, and which employs a 10-fold digital interpolation, a 10-bits D/A converter and a 2nd order active-RC filter with nominal 800 kHz cut-off frequency. A careful inspection of the layouts of both blocks shows the differences in each one of the constituting block areas. For example, the output active RC filters which correspond to the large areas on the right-hand side of the layout; we can also see different areas for the steering current D/A conversion in the middle of the blocks and the different areas for the digital processing unit just before the D/A conversion functions. In the first case, we clearly see that signal processing function. In the second case, this is not included in core as the customer has decided to implement that function together with other digital signal processing functions. This example illustrates the use of application-driven retargetable analog-digital blocks to achieve increased design productivity.

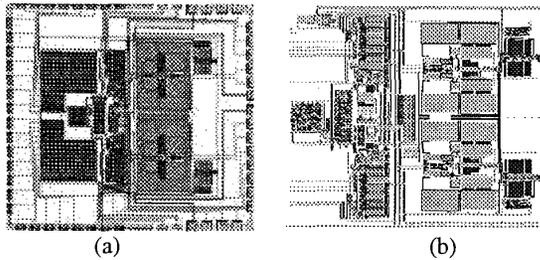


Fig. 7: Retargetable block layouts.

## 6 Conclusions

The material presented and discussed in this paper makes it clear that mixed-signal integrated circuits will play an increasingly important role in semiconductor markets and that the rate of technology and application developments will increase the pressure to cope with far greater productivity requirements for designing. Firstly, because of their intrinsic multi-disciplinary nature and secondly because of the lack of adequate tools that cross all the hierarchical levels of design, from architectural design to layout generation. The concept of retargetable, application-driven analog-digital blocks will provide the solution to those requirements in terms of design productivity and cost effectiveness. In order to achieve this, new methodologies and supporting tools encapsulating hierarchical multi-level design information must be developed alongside comprehensive behavioral models embedding both functional and electrical performance information. It is clear that the development of such methodology is still in its infancy and therefore significant efforts have to be deployed world-wide so that the tools that are needed to provide the required design support become widely available.

## Acknowledgements

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