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Nielsen, Jannik Hammel; Lehmann, Torsten

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AN IMPLANTABLE CMOS AMPLIFIER FOR NERVE SIGNALS

Jannik Hammel Nielsen[1], Torsten Lehmann[2]

[1]Ørsted-DTU, Technical University of Denmark, DK-2800 Kgs. Lyngby, jhn@oersted.dtu.dk
[2]Cochlear Ltd., 14 Mars Road, Lane Cove 2066 NSW Australia, tlehmann@cochlear.com.au

ABSTRACT: In this paper, a low noise high gain CMOS amplifier for minute nerve signals is presented. By using a mixture of weak- and strong inversion transistors, optimal noise suppression in the amplifier is achieved. A continuous-time offset-compensation technique is utilized in order to minimize impact on the amplifier input nodes. The method for signal recovery from noisy nerve signals is presented. A prototype amplifier is realized in a standard digital 0.5 μm CMOS single poly, n-well process. The prototype amplifier features a gain of 80 dB over a 3.6 kHz bandwidth, a CMRR of more than 87 dB and a PSRR greater than 84 dB. The equivalent input referred noise in the bandwidth of interest is $5\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. The amplifier power consumption is 275 μW.

1 INTRODUCTION

Thousands of individuals sustain damages to the central nervous system, e.g. spinal chord injury, stroke, etc. which potentially results in paralyzed limbs. However, such damages usually leave the nerves and muscles in the limbs unaffected. In recent years, biomedical research has focused on retrieving nervous information from the natural sensors of the body and using this to activate paralyzed muscles by Functional Electrical Stimulation (FES) [1, 2]. Succesful trials have been conducted using external devices, correcting dropfoot in early schlyrosis patients [1], and restoring basic hand functions [2], by using natural sensor feedback.

Our involvement comes from developing implantable ASICs for both sensing neural information and for stimulating muscles through FES. An implantable stimulator has been developed and is reported in [3]. Developing implantable devices, reduces the risk for infection as skin continuity is ensured. Also, the need for external sensors which need calibration, may be bulky and are subject to mechanical stress limiting device life-span [1], is eliminated by using the natural sensors of the body.

This paper reports the implementation of the proposed MOSFET amplifier in [4], for amplification of minute nerve signals.

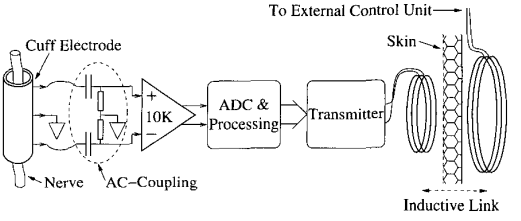

Fig. 1: Proposed nerve signal recovery implant.

2 PROPOSED SENSING IMPLANT

The overall sensing system for implantation to be developed is shown in fig. 1.

The electrical contact with the nerve is obtained using a so-called *cuff electrode* [1, 2]. The cuff electrode has a length of 10-20 mm and is placed around the nerve trunk. It has a contact resistance of about 5 kΩ and provides a differential nerve signal of about $\pm 10\,\mu$V. Control signals, data transmission and power supply are conveyed through the inductive link, dictating a very small supply current, on the order of a few hundred μA.

The signal from the cuff is AC-coupled to remove inherent DC offsets. Due to the very small signal amplitude, it is necessary to preamplify the signal prior to any processing. The preamplifier increases the input amplitude from $\pm 10\,\mu$V to $\pm 100\,$mV. As we are not interested in the absolute value of the signal, gain variation of 10%-15% can be tolerated. The nerve signals reside primarily in the bandwidth $400 < f_\mathrm{n} < 4000$ Hz [2], giving the necessary amplifier bandwidth.

After amplification the signal is anti-aliased and A/D converted. Some local processing to recover the nerve signal is then performed and the resulting signal is transmitted to the external control system through the inductive link.

3 SIGNAL RECOVERY

The technique used for signal recovery [1, 2], samples the nerve signal at $f_\mathrm{s} = 10$ kHz. After A/D conversion, the signal is rectified, integrated and downsampled to $f_\mathrm{r} = 20$ Hz, giving the signal envelope.

The nerve signal can be described as a zero mean

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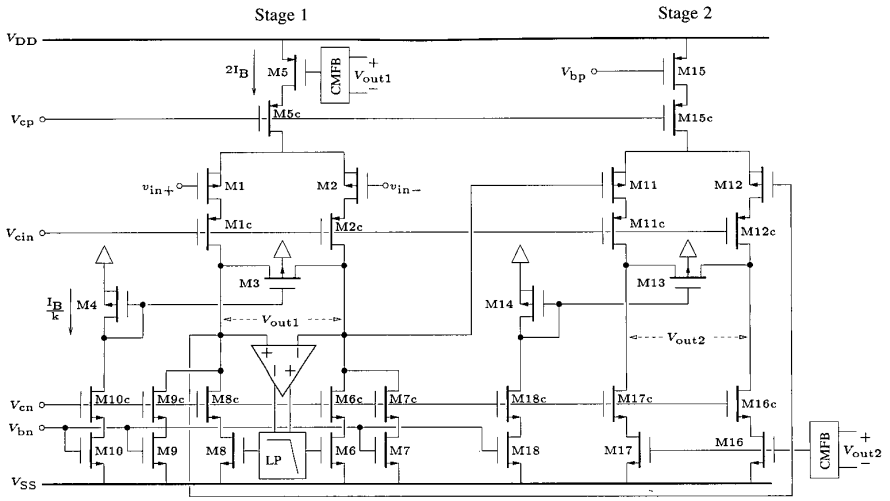

Fig. 2: Amplifier schematic.

stochastic variable V_n, with variance and mean:

$$\sigma_n^2 = \mathrm{E}\left\{V_n^2\right\} \text{ and } \mu_n = \mathrm{E}\left\{V_n\right\} = 0$$

The rectified signal V_r and its mean are given by:

$$V_r = \sqrt{V_n^2} \text{ and } \mu_r = \mathrm{E}\left\{\sqrt{V_n^2}\right\}$$

We can thus find the variance of the rectified signal:

$$\sigma_r^2 = \mathrm{E}\left\{\left(V_r - \mathrm{E}\left\{V_r\right\}\right)^2\right\} = \sigma_n^2 - \mu_r^2 \qquad (1)$$

Assuming a gaussian distribution of V_n, the mean of V_r can be found to be: $\mu_r = \sqrt{2/\pi}\,\sigma_n$. Inserting μ_r in eq. (1) yields the rectified signal variance: $\sigma_r^2 = \sigma_n^2\,(1 - 2/\pi)$. The variance of the downsampled signal is reduced by the ratio of sampling frequencies $k = f_s/f_r$. Thus the SNR of the downsampled signal is:

$$\mathrm{SNR} = 10\log\left(k\mu_r^2/\sigma_r^2\right) \simeq 29\,\mathrm{dB},\ f_s = 10\,\mathrm{kHz}$$

Though this SNR may seem low, it is sufficient to determine the state of a human nerve.

4 AMPLIFIER

A diagram of the designed amplifier is shown in fig. 2. Transistors denoted by a 'c' are used as cascodes. The amplifier consists of two amplification stages with similar topology, each has a gain of 100.

4.1 First stage

Due to the small amplitude of the input signal, it is of prime importance that the noise of the input transistors is kept to a minimum. The amplifier induced noise should remain below the thermal noise inherent to the cuff electrode. The input referred noise in a strong inversion MOSFET is given by [5]:

$$\frac{V_i^2}{\Delta f} = 4kT\left(\frac{2}{3}\right)\frac{1}{g_m} + \frac{K_f}{WLC_{ox}f} \qquad (2)$$

The first term of eq. (2) is the thermal noise in the MOSFET and the second term is the flicker (1/f) noise, where K_f is a process-dependent constant. In general, 1/f noise is found to be lower in P-MOS than in N-MOS transistors [6], thus P-MOS transistors are used in the input differential pair. Eq. (2) shows that the thermal noise is minimized by maximizing the transconductance g_m. Using the EKV-model, the g_m of the MOSFET in weak- and strong inversion can be shown to be [7]:

Weak inversion: $g_{m,\,weak} = I_D/nV_T$
Strong inversion: $g_{m,\,strong} = 2nI_D/V_{eff}$

Where $n \simeq 1.25$ is the slope factor and the thermal voltage $V_T \simeq 26.7\,\mathrm{mV}$ at 37°C. The ratio of the transconductances is: $g_{m,\,weak}/g_{m,\,strong} \simeq 5.6$ for a typical effective voltage of 300 mV. Thus, by biasing the input transistors in weak inversion, we can obtain maximum thermal noise suppression for a given I_D. So in order to obtain a low input referred noise, most of the amplifier current is drawn by M1 and M2.

The DC gain of stage 1 is given by:

$$A_{V1} = -\frac{g_{m1}}{2g_{ds3}} = \frac{(W/L)_1}{(W/L)_3}\cdot\frac{1}{2n} \qquad (3)$$

Provided M1, M2 and M3 in fig. 2 are biased in weak inversion. Thus the gain can set by device dimensions. The prerequisite of eq. (3) is that

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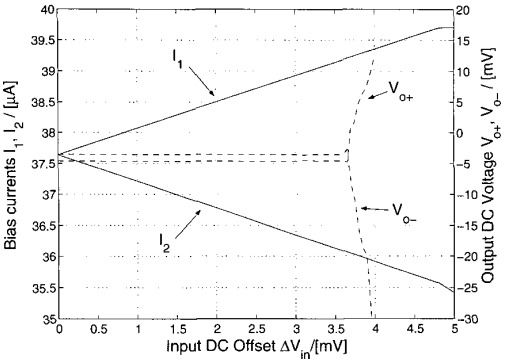

Fig. 3: Offset cancellation by current steering.

the gate-source voltages of M1, M2 and M3 are equal. This is ensured by letting a scaled current I_B/k, flow through the diode-connected M4 and using V_{G4} to bias M3. M4 is accordingly scaled $(W/L)_4 = 1/k\,(W/L)_1$, and will also be working in weak inversion. The source/drain voltage of M3 is set equal to zero by a common mode feedback circuit. All current source transistors (M6-M10) operate in strong inversion to minimize their noise contribution [5].

Gain variation due to device dimension mismatch can be minimized by layout techniques. The gain is however also dependent on the slope factor n. It can be shown that n is ultimately dependent on the substrate doping concentration N_{sub}. For variations in N_{sub} of ± 1 order of magnitude, the variation in n was found to be less than 10%, which is acceptable.

4.2 Offset cancellation

As the inherent threshold offset ΔV_{t0}, present in the input pair M1, M2 indeed may be orders of magnitude larger than the input signal, it will force the input stage out of weak inversion. Hence some scheme for offset cancellation is needed. To avoid the clock-feedthrough problems of switched methods, a continuous time scheme is utilized.

In fig. 2, the output of stage 1 is LP filtered and used to control source transistors M6 and M8 to match the current offset in M1 and M2. As we are not interested in DC, this scheme is applicable provided the time constant around the control loop is large enough. In fig. 3, the simulated bias currents I_1, I_2 and the measured output voltages of stage 1 are shown vs input DC-offset. Fig. 3 shows that offsets $< 3.5\,\mathrm{mV}$ will be compensated. Some residual offset will remain at the output due to device mismatch in the control loop and is $\simeq 1.1\,\mathrm{mV}$ in fig. 3.

Using this scheme will cause some bias current mismatch in M1 and M2. The operating point

Supply Voltage	3 V
Power Consumption	$275\,\mu\mathrm{W}$
SNR	36 dB
THD(@ f=1 kHz)	2.2 %
Typ. Input Offset (Stage 1)	$< 40\,\mu\mathrm{V}$
CMRR	$> 87\,\mathrm{dB},\ f < 100\,\mathrm{kHz}$
PSRR	$> 84\,\mathrm{dB},\ f < 100\,\mathrm{kHz}$
Gain	$10000 \pm 10\%$
Equiv. input referred noise	$5\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$

Table 1: Measured Amplifier Performance.

transconductance of M1 and M2 is given by [7]:

$$g_m = 2nK_p\left(\frac{W}{L}\right)\frac{1}{nV_T}\exp\left(\frac{V_G - nV_S - V_{t0}}{nV_T}\right)$$

The current offset can be modelled by letting a small pertubation ΔV_{GS}, offset the operating point:

$$g_{mi} = g_m \exp\left(\pm\Delta V_{GS}/nV_T\right),\ i = 1,\ 2 \qquad (4)$$

As $|\Delta V_{GS}| \ll nV_T$, we can use a 1st order approximation for eq. (4). Thus the total transconductance of the differential pair can be expressed:

$$g_{m,tot} = \frac{g_{m1}g_{m2}}{g_{m1}+g_{m2}} = \frac{g_m}{2}\left[1-(\Delta V_{GS}/nV_T)^2\right] \simeq \frac{g_m}{2}$$

Hence to a first order approximation, the gain of the stage will not be affected.

4.3 Second stage

The second amplification stage basically has the same topology as the first stage, only all transistors are now in strong inversion. Due to the magnitude of the signals in the second stage, weak inversion operation is not applicable here. Using the EKV model in strong inversion, we find the gain to be:

$$A_{V2} = -\frac{g_{m11}}{2g_{ds13}} = \frac{(W/L)_{11}}{(W/L)_{13}}\cdot\frac{1}{2n}$$

As the transistors are biased in strong inversion, the inherent offset can be tolerated as this will not bring the transistors out of saturation. However, AC-coupling the two stages was done in the experimental setup to minimize the contribution to offset from the first stage.

Thus by choosing the gain to 100 for both stages, a total gain of 80 dB is achieved.

5 EXPERIMENTAL RESULTS

A test chip with the proposed amplifier has been fabricated in a standard digital $0.5\,\mu\mathrm{m}$, single poly, N-well CMOS process. Table 1 summarizes the measured performance of the amplifier. Fig. 4

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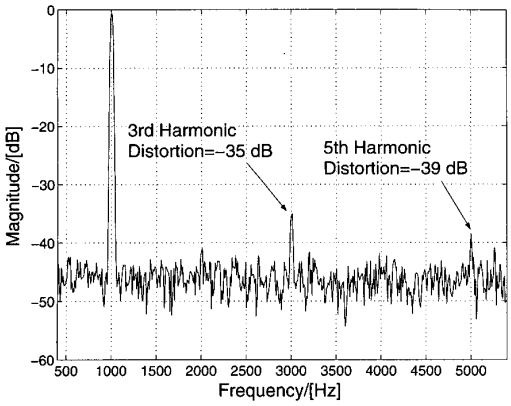

Fig. 4: Measured spectrum at the amplifier output.

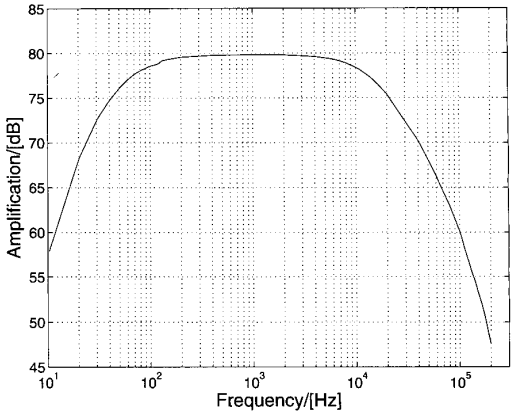

Fig. 5: Amplifier magnitude frequency response.

shows the output power spectrum for an input sine at 1 kHz and amplitude $v_{\text{in}} \simeq 22\,\mu\text{V}_{\text{rms}}$. The total distortion power is -33 dB below the fundamental, equivalent to a THD of 2.2 %, which is acceptable for for our application. The circuit draws 91.5 μA from a 3 V supply, thus consuming 275 μW. The measured output magnitude frequency response is shown in fig. 5. For frequencies $f < 100$ kHz, the amplifier has a CMMR > 87 dB and a PSSR > 84 dB. The equivalent input referred noise over the signal bandwidth is $5\,\text{nV}/\sqrt{\text{Hz}}$, equivalent to a maximum SNR of $\simeq$ 36 dB.

Some gain variation was observed in the test chips. These variations are mainly due to offsets in the common mode voltage of stage 1, which in turn modulates the gain as V_{GS} of M3 is altered.

The simple scheme of using a single fixed bias transistor as load, does not provide high linearity as seen from fig. 4. However, as the signal recovery method only provides an SNR of approx. 29 dB, the THD is within acceptable bounds.

6 CONCLUSIONS

In this paper an amplifier for minute nerve signals was presented. The utilization of weak inversion input transistors, with maximized $g_{\text{m}}/I_{\text{D}}$ to suppress inherent device noise, has been shown to be feasible for the very tight power consumption limits inherent to implantable devices.

For offset cancellation, a continuous-time scheme by tuning bias currents was used. This was done in order to avoid the dynamic offsets introduced by switching schemes, which potentially could be far larger than the minute input signal itself. A condition of this method is that only AC-information needs to be amplified as DC is filtered out.

Finally, the characteristics of a test chip with a prototype amplifier was presented. The prototype exhibits performance within the boundaries put forth. Some harmonic distortion is present, and the SNR is limited. However, for the used signal recovery method, these are within acceptable range.

7 ACKNOWLEDGMENT

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