A Flexible Resonation-Based Cascade ΣΔ Modulator with Simplified Cancellation Logic

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Abstract **– This paper presents a new two-stage cascade ΣΔ modulator architecture that uses inter-stage resonation to increase its effective resolution as compared to conventional cascades and avoids the need for digital filtering in the error cancellation logic. The combination of these two strategies, together with the use of unity signal transfer function in all stages, make the presented modulator highly tolerant to noise leakages, very robust to non-linearities and mismatches of the loop-filter circuitry, and especially suited for low-voltage implementations at low oversampling ratios. In addition, the use of loop filters based on Forward-Euler integrators, instead of Backward-Euler integrators, simplifies the switched-capacitor implementation of the resonation and makes the presented architecture very suited for reconfigurable multi-standard applications. As an illustration, a Beyond-3G case study is shown to demonstrate the benefits of the presented approach.†1**

I. INTRODUCTION

Beyond-3G wireless telecom systems require efficient CMOS multi-standard transceivers capable to operate over different co-existing standards, signal conditions and battery status, while minimizing their power consumption [1]. One of the most challenging parts in these systems is the Analog-to-Digital Converter (ADC), because of the varying sampling rates and resolutions required to handle the wide range of signals corresponding to each individual operation mode [2].

The majority of reported multi-standard ADCs uses the ΣΔ Modulation (ΣΔM) technique [3]-[9], being the most commonly applied reconfiguration strategy just changing the OverSampling Ratio (*OSR*) according to the operation standard. However, the increasing demand for high data rates in new standards restricts oversampling to low values, what forces to increase the noise-shaping filter order and/or the number of bits of the internal quantizers.

A usual design choice is to employ cascade (MASH) topologies in order to circumvent the stability problems of high-order loops. However cascade topologies are more sensitive to quantization noise leakages caused by mismatches between the analog and digital signal processing in the cascade. These problems can be alleviated by using the so-called *sturdy* MASH (SMASH) architecture, which eliminates the need of digital filtering in the error cancellation logic [10]. Moreover, the use of cascade ΣΔM topologies can be combined with loop-filter resonation in order to optimally distribute the zeroes of the Noise Transfer Function (NTF), so that the in-band noise can be reduced without increasing the filter order. Recently, a new kind of resonation strategy, called *global resonation*, has been applied to cascade ΣΔMs [11]. Traditionally, the implementation of the in-loop resonators requires Backward-Euler (BE), which makes its Switched-Capacitor (SC) implementation more difficult and less robust. In addition, it requires extra Digital-to-Analog Converters (DACs) in the resonation inter-stage paths.

This paper contributes to this topic and presents a novel ΣΔM architecture intended for low-voltage broadband applications, which extends the underlying principle of SMASH ΣΔMs to the implementation of global resonation in an efficient mode. It uses only Forward-Euler (FE) integrators, with neither digital cancellation logic filter nor extra DACs required. In addition, unity Signal Transfer Function (STF) [12] is used in all stages of the modulator, thus relaxing the requirements of amplifier gain nonlinearity and output swing. Moreover, the modulator incorporates reconfiguration strategies at both architectural- and circuital-level, thus making it very suited for multi-standard telecom systems. As an application, time-domain behavioral simulations including main circuit limitations are shown for different standard requirements included in Beyond-3G wireless telecom systems.

II. PROPOSED MODULATOR ARCHITECTURE

Fig. 1 shows the proposed modulator architecture. It consists of a 2-2 cascade ΣΔM including unity STF and multi-bit quantization in both stages. Global resonation is implemented through the two inter-stage paths (highlighted in Fig. 1) that feed back a delayed version of the last-stage quantization error at the input of the first-stage quantizer. One advantage of this scheme is that, contrary to the one reported in [11], only FE integrators are used. This simplifies the SC implementation and reduces sensitivity to circuit non-idealities.

Besides, the proposed modulator removes the matching requirements between analog and digital filtering. This is achieved by a modified version of the SMASH concept, implemented in Fig. 1 as a digital subtraction of the quantizer outputs inside the first-stage loop [13]. This strategy eliminates the need of additional

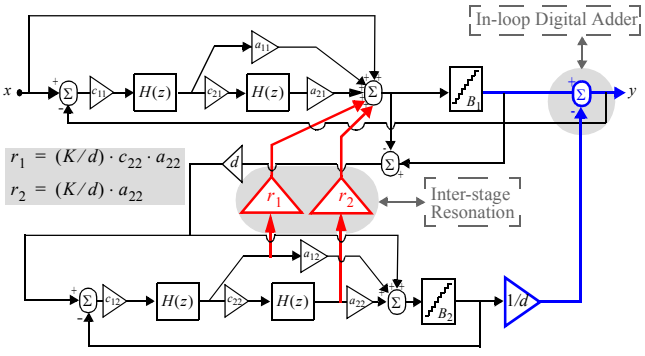

Figure 1. Proposed ΣΔM architecture.

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feedback paths as originally proposed in [10], so that the number of linear DACs required is not increased as compared to a conventional MASH ΣΔM. However, a DAC with a full scale larger than that of the quantizers in the cascade (with resolutions B_1 and B_2) is required in order to account for the summation of the digital output of the stages. Nevertheless, the location of the digital adder helps to increase considerably the robustness to capacitor mismatches [13].

Another advantage of the proposed topology as compared to conventional SMASH consists of the beneficial use of an inter-stage scaling factor d that helps to reduce the power of the second-stage quantization error at the output [13]. This factor together with the rest of coefficients, listed in Table I, have been properly selected in order to minimize the amplifiers output swings.

In case that resonation is enabled and considering a linear model for the embedded quantizers, it can be shown that the NTF of the proposed architecture is given by:

$$NTF(z) = \frac{-(1-z^{-1})^2 \cdot [1-(2-K)\cdot z^{-1}+z^{-2}]}{d} \quad (1)$$

where two of the NTF zeroes are a function of K, whose value can be optimally chosen to maximize the Signal-to-(Noise+Distortion) Ratio (*SNDR*). Note that an increase of d (to reduce the quantization noise) yields a reduction of the feedback coefficient K/d. In practice, this results in a smaller capacitor ratio, which complicates its electrical implementation while reducing capacitor matching. However, the value of K/d can be easily implemented if the oversampling ratio is low enough because —as shown in [11]— a reduction of *OSR* means an increase of K. Therefore, the resonation provided by the proposed modulator is specially suited for wideband applications with low *OSR*.

III. SWITCHED-CAPACITOR IMPLEMENTATION

Fig. 2 shows the conceptual SC schematic of the modulator in Fig. 1, in which the required analog additions are implemented by passive SC networks in order to save power. The desired analog coefficients are implemented as capacitor ratios as shown in Table II. Note that a number of capacitors in Fig. 2 have negative values; in the actual fully differential implementation, this negative value would be implemented by swapping the corresponding capacitors in the positive and negative signal branches.

TABLE I. MODULATOR COEFFICIENTS

$a_{11}=8$	$a_{21}=4$	$a_{12}=8$	$a_{22}=4$	$d=2$
$c_{11}=1/4$	$c_{21}=1$	$c_{12}=1/4$	$c_{22}=1$	

TABLE II. SC IMPLEMENTATION OF THE ΣΔM COEFFICIENTS

In-loop Capacitors
$a_{11}= C_{a11}/C_{in1}$; $a_{12}= C_{a12}/C_{in2}$; $a_{21}= C_{a21}/C_{in1}$; $a_{22}= C_{a22}/C_{in2}$
$c_{11}= C_{s11}/C_{i11}$; $c_{12}= C_{s12}/C_{i12}$; $c_{21}= C_{s21}/C_{i21}$; $c_{22}= C_{s22}/C_{i22}$
Inter-stage Capacitors
$C_{r1}= c_{22}\cdot a_{22}\cdot (K/d)\cdot C_{in1}$; $C_{r2}= a_{22}\cdot (K/d)\cdot C_{in1}$
$C_{s12d} = d\cdot C_{s12}$; $C_{in2d} = d\cdot C_{in2}$;
$C_{r1d} = c_{22}\cdot a_{22}\cdot K\cdot C_{in2}$; $C_{r2d} = a_{22}\cdot K\cdot C_{in2}$
$C_{r1s12d} = c_{22}\cdot a_{22}\cdot K\cdot C_{s12}$; $C_{r2s12d} = a_{22}\cdot K\cdot C_{s12}$
Adder Capacitors
$C_{a12}= a_{12}\cdot C_{in2}$; $C_{a22} = a_{22}\cdot C_{in2}$
$C_{s12d}= d\cdot C_{s12}$;$C_{a11s12d} = d\cdot a_{11}\cdot C_{s12}$; $C_{a21s12d} = d\cdot a_{21}\cdot C_{s12}$
$C_{in2d}= 2\cdot C_{in2}$; $C_{a11in2d} = d\cdot a_{11}\cdot C_{in2}$; $C_{a21in1d}= a_{21}\cdot C_{in2d} = d\cdot a_{21}\cdot C_{in2}$

The use of passive SC analog additions involves a reduction of the full scale at the quantizer input and, consequently, a compression of the references and the quantizers voltage levels to be used [14]. For instance, considering charge redistribution in the capacitors of the first-stage analog adder, the resulting scaling factor is

$$\frac{C_{\text{in1}}}{13C_{\text{in1}} + 8K/d\cdot C_{\text{in1}} + C_{\text{quant}}} \quad (2)$$

where C_{quant} stands for the input capacitance of the quantizer.

In order to get a robust modulator implementation it is desirable to have the same factor regardless of the use of resonation. However, note from (2) that the denominator term $8K/d\cdot C_{\text{in1}}$ equals zero in case resonation is not employed, and thus the scaling factor varies from the one obtained with resonation. Let us assume that $C_{\text{in1}} = 0{,}4\text{pF}$, $d = 2$, $K = 0.1$, a 1.5-bit quantizer and 40-fF input capacitance for the quantizer comparators; then the corresponding scaling factor would be 0.0649, being 0.0667 when resonation is not employed ($K = 0$). This former value can be implemented via a resistor ladder with a 2 to 30 ratio. The second-stage quantizer scaling factor can not be obtained with a mathematical formulae since this stage only processes the quantization error of the previous one. Therefore a simulation-based approach is used to determine this value as depicted in Fig. 3 for two different modes of the case study in next section. An acceptable value is 0.025 which can be realized with a resistors ratio of 4 to 160. Unfortunately, small scaling factors —as those employed in this example (0.067 and 0.025)— impose strict requirements on the comparators input offset. For instance, the first- and second-stage comparators offset requirements are 40 and 7.5mV respectively in this case. This issue can be relieved by design and/or using auto-zero techniques.

The modulator uses 3- and 5-level quantization in the first and second stages respectively, and an inter-stage scaling factor of 2 that leads to a 13-level DAC embedded in the front-end feedback. In practice, Dynamic Element Matching (DEM) is needed in this feedback path to reduce the effect of mismatches of the DAC elements.

The modulator includes different reconfiguration strategies. On the one hand, the order can be configured to be either 2 or 4, by using the control signal SL in Fig. 2. On the other hand, several SC networks (highlighted in Fig. 2) are enabled or disabled depending on whether the global resonation is used or not. All these reconfiguration strategies (adaptive global resonation and NTF order) can be used independently, thus giving more flexibility to the ΣΔM to adjust its functionality to the required performance. In a practical application, those components that are not used can be turned off by using a power-down control in order to save power consumption.

IV. CASE STUDY: APPLICATION TO BEYOND-3G SYSTEMS

In order to show the benefits of the proposed ΣΔM architecture, a case study is presented considering the standards and their specifications listed in Table III. This table also shows the values of the modulator design parameters that are reconfigured for the different

TABLE III. STANDARDS SPECIFICATIONS AND ΣΔM PARAMETERS.

Standard	**GSM**	**BT**	**UMTS**	**DVB-H**	**WiMax**	**WLANa**	**WLANg**
***SNDR* (dB)**	80	75	65	55	60	65	50
***BW* (MHz)**	0.2	0.5	1.96	3.8	10	10	20
L	2				4		
OSR	200	80	40	20	8	16	8
***fs* (MHz)**	40	80	160		160	320	

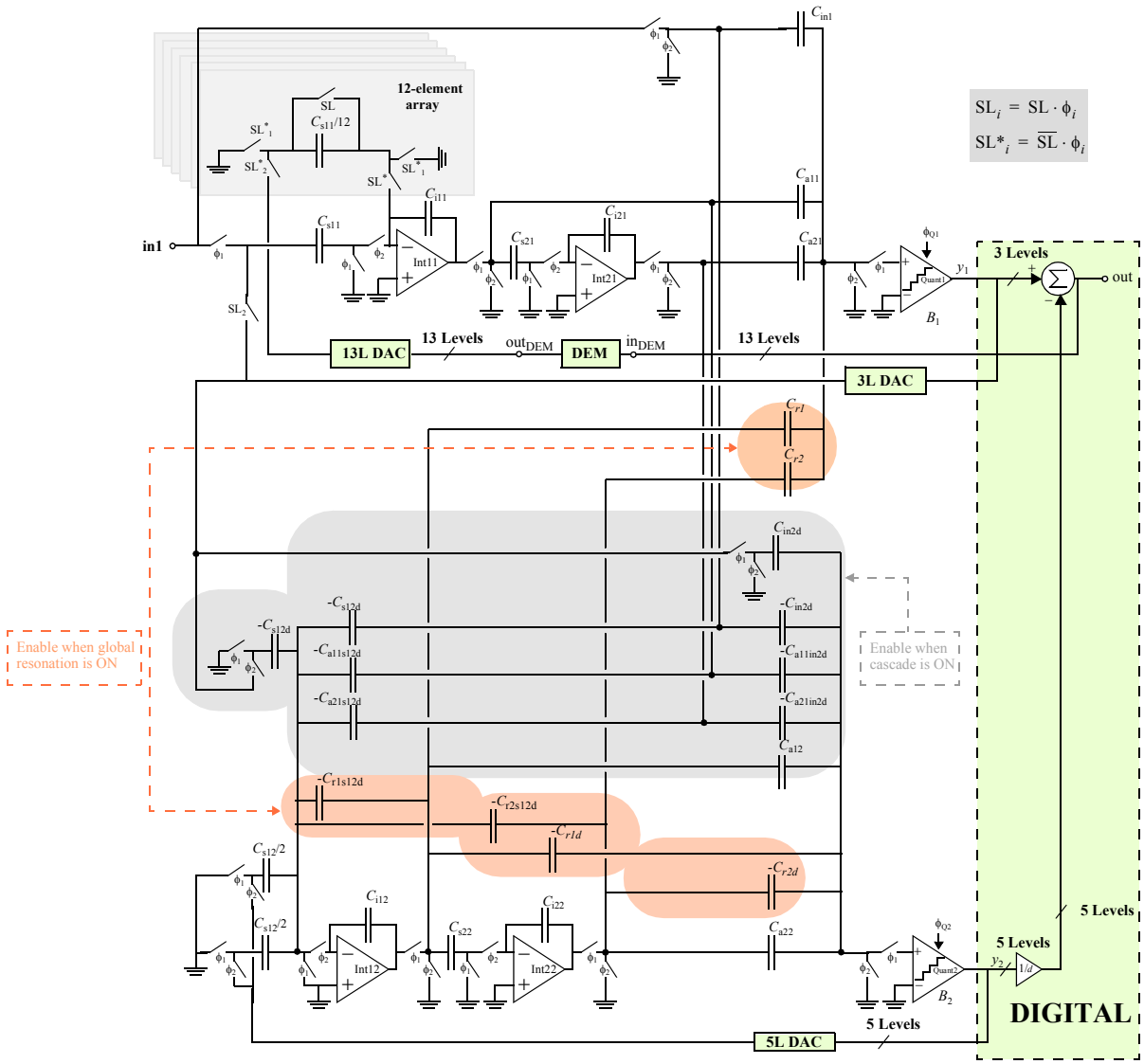

Figure 2. SC schematic of the proposed reconfigurable ΣΔM (single-ended version).

operation modes, namely: NTF order (L) and *OSR*. Different oversampling ratios —and their corresponding sampling frequencies (f_s)— are employed in order to cope with the required resolution for each signal bandwidth. Besides, global resonation is used only in WLANg mode with a feedback coefficient of $K/d = 0.05$, resulting in a shift of two zeroes of the NTF from 0 to $0.95 \pm j0.32$. This zeroes distribution reduces in approximately 9.5dB the quantization noise within a 20-MHz bandwidth.

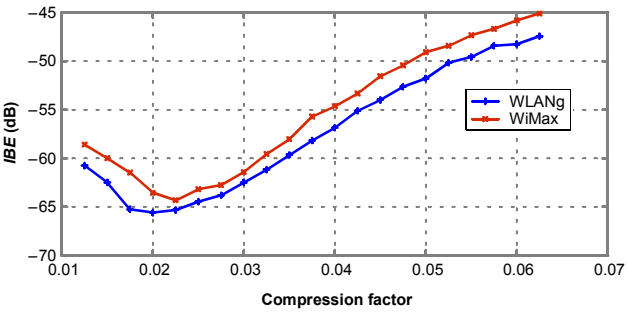

Figure 3. Evolution of the In-Band Error (*IBE*) versus the 2nd-stage quantizer compression factor (-6dBFS input signal).

Several behavioral simulations have been performed using SIMSIDES, a SIMULINK-based time-domain simulator for ΣΔ modulators [15]. The main circuit non-ideal effects were taken into account considering the quantizer scaling factors given in the example of Section III. The first-stage feedback DAC is assumed linear. Nevertheless, as stated above, DEM will be required in practice.

Since there is no noise leakages due to mismatching between analog and digital processing in the cascade in Fig. 1, the DC gain amplifiers requirements are clearly relaxed —compared to those of a traditional cascade— as illustrated in Fig. 4 for WiMax mode. In fact, only a 35-dB amplifiers DC gain is selected for all modes. This is specially beneficial with the technological scaling where the transistor gain, and subsequently that of the amplifier, is getting lower and lower. Moreover, Fig. 4 shows that except for the 3rd opamp the amplifiers DC gain can be lowered much more. Note that contrary to conventional cascades —in which the requirements are more

challenging in the front-end amplifiers— the 3rd opamp is the most demanding one. This is a result of the elimination of the digital processing, that relaxes the requirements of the front-end amplifiers. In addition, the 3rd amplifier drives the largest capacitance load what imposes the greatest requirements in opamp dynamics.

Fig. 5 shows the resulting spectra for the cascade in Fig. 1 for the operation modes of WiMax, WLANa and WLANg. Note that a duplication of *fs* implies a reduction of the *IBE* power for WLANa when compared to WiMax for a 10-MHz bandwidth. On the other hand, the effect of the optimal distribution of two NTF zeroes —thanks to the use of inter-stage resonation— in WLANg mode diminishes the *IBE* power when compared to WLANa in its bandwidth of 20 MHz. Resonation is only noticed when resolution is dominated by quantization and not thermal noise. Indeed, the resonation resolution enhancement is not so clear for frequencies below 10MHz in which thermal noise has a noticeable influence on the overall *IBE* power.

Fig. 6 depicts the *SNDR* curves for all operation modes. It can be observed that the modulator fulfils the requirements of Table III. Note that for the cascade configured modes, even when resonation is applied (WLANg), overload levels are comparable —and better in a number of modes— to those of 2nd-order loop configurations

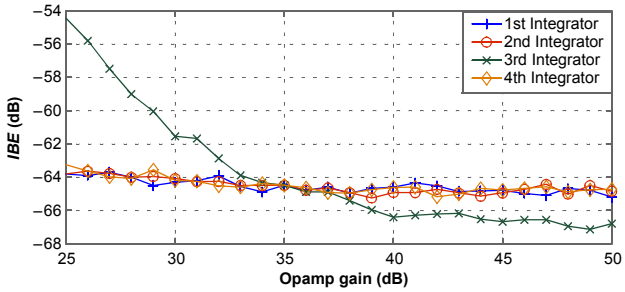

Figure 4. *IBE* vs. amplifier DC gain for WiMax (-6dBFS input level).

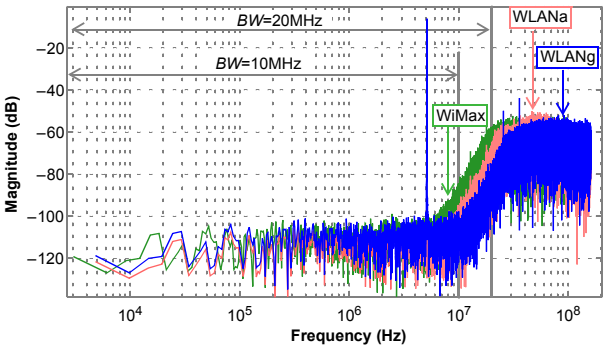

Figure 5. Spectra for WiMax and WLAN modes (-3dBFS input level).

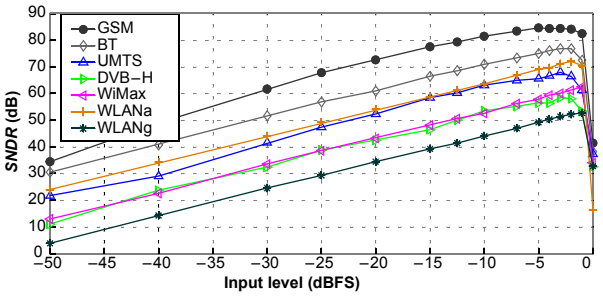

Figure 6. *SNDR* vs. input signal level.

with feedforward paths. Additionally, as Fig. 6 shows, the ΣΔM overloads very close to the reference voltage (1.2V) for all modes, suggesting thus a large robustness to amplifier non-linearities. This translates into very low amplifier output swings, being always lower than 0.2 and 0.3V for the cascade and 2nd-order single-loop configurations, respectively.

CONCLUSIONS

A new resonation-based cascade ΣΔM architecture is presented. This modulator is capable to reconfigure the order of the quantization noise filtering and to resonate through switchable feedback inter-stage paths. These figures are combined with unity STFs in both cascade stages, thus achieving high linearity with reduced output swing requirements. Moreover, no digital cancellation logic filtering is required, removing thus noise leakages given by analog and digital processing mismatches. All these characteristics make the presented architecture very suited to the implementation of low-voltage multi-standard ADCs with very relaxed opamp requirements. In order to demonstrate the capabilities of the proposed modulator, a case study covering a number of standards, including GSM, Bluetooth, UMTS, DVB-H, WiMax and WLAN is shown.

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