Improved Rf Cmos Active Inductor With High Self Resonant Frequency

Cristian Andriesei, Liviu Goras, Farid Temcamani, Bruno Delacressonnière

IMPROVED RF CMOS ACTIVE INDUCTOR WITH HIGH SELF RESONANT FREQUENCY

C. Andriesei, L. Goraş
ETTI/"Gh. Asachi" Technical University
Iaşi, Romania
candriesei@etc.tuiasi.ro

F. Temcamani, B. Delacressonniere
ENSEA/Université de Chergy-Pontoise
Cergy, France
temcamani@ensea.fr

Abstract—Many architectures of transistor only simulated inductors (TOSI) have been proposed until now in literature. Exhibiting tuning possibilities, low chip area and offering integration facility, they constitute promising architectures to replace passive inductors in RF circuits. An improved CMOS active inductor topology is proposed in this paper. With a novel loss compensation scheme, frequency increase up to 1.1 GHz (30%–66%) of the inductor self resonant frequency is achieved in the frequency band 1.5–3.3 GHz with large quality factors and very low current consumption. Besides, a more accurate passive model is proposed for CMOS TOSI active inductors and tested for this particular topology. Consisting of four parallel branches, it is still second order even though it contains three conservative elements. The model is sufficient general and proves superior performances over the classical RLC model mainly for higher frequencies. The simulations were carried out in a 0.18 um CMOS process.

Keywords-active filter; circuit modeling; CMOS; gyrators; negative capacitor

I. INTRODUCTION

Various CMOS TOSI architectures have been proposed during the last two decades, covering a wide range of applications: RF bandpass filters [1–3], (RF/bandpass) amplifiers [4–5], current or voltage oscillators [6–7] and even frequency dividers [8].

TOSI architectures basically consist of a capacitively loaded gyrator made of several transistors, typically two, loaded by the parasitic capacitor of one transistor. The main advantages of these capacitorless entirely active simulated inductors over on–chip passive inductors are low silicon area and frequency and quality factor tuning possibility while current consumption, noise and nonlinearity are the main drawbacks. Inductor losses can be reduced by using varactors [3], one negative resistance or even two [9].

The only equivalent model reported so far in literature for TOSI is the lossy LC parallel resonant circuit. Even though such model contains approximations, only gate to source capacitors being taken into account by the authors, it is good enough in applications where the inductive behavior only is exploited (LNAs). However, for voltage controlled oscillators (VCO) or bandpass filters where the self resonant frequency is of utmost importance, this classical RLC model does not approximate the resonant frequency accurately, giving significant errors for higher frequencies in the GHz domain.

This article is organized as follows. First, a more accurate TOSI passive model is proposed and discussed for a particular CMOS TOSI architecture in Section II. Frequency enhancement technique with negative capacitances is applied to the same inductor and studied in Section III. Simulation results are reported in Section IV while conclusions are presented in the last Section.

II. PROPOSED RLC MODEL FOR TOSI

The simulated inductor [2] studied in our research is presented in Fig. 1a together with the RLC model (Fig. 1b), generally adopted in literature for TOSI architectures [3–8]. The gyration function is implemented by transistors M_1 (inverting stage) and M_2 (non–inverting transconductor) while a current source I_b is used for biasing purpose. In other words, only three transistors are necessary to emulate the inductor behavior, therefore making this active inductor suitable for low power and small chip area RF devices. Furthermore, the inductor input impedance Z_{in} is computed (1-2) and synthesized as obtained in Fig. 1c), the bulk effect being neglected.

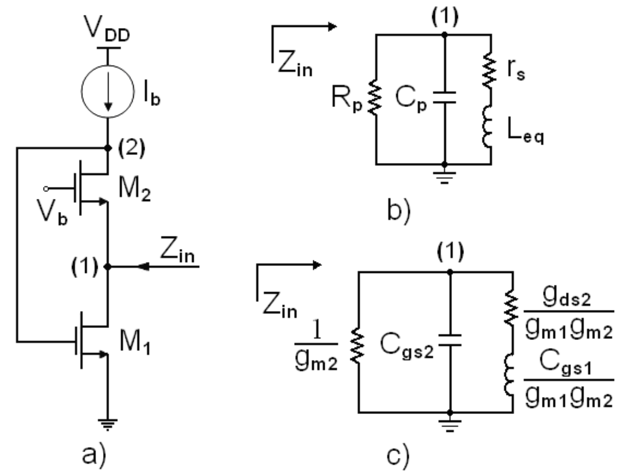

Figure 1. CMOS simulated inductor and equivalent passive model

$$Z_{in}(s) = \frac{b_1 s + b_0}{s^2 + 2\alpha s + \omega_0^2} \tag{1}$$

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$$
\begin{cases}
b_0 = \dfrac{g_{ds2}}{C_{gs1}C_{gs2}},\ b_1 = \dfrac{1}{C_{gs2}} \\
2\alpha = \dfrac{g_{ds1}C_{gs1} + g_{ds2}C_{gs2} + g_{m2}C_{gs1} + g_{ds2}C_{gs1}}{C_{gs1}C_{gs2}} \\
\omega_0^2 = \dfrac{g_{m1}g_{m2} + g_{m1}g_{ds2} + g_{ds1}g_{ds2}}{C_{gs1}C_{gs2}}
\end{cases}
\tag{2}
$$

As it can be noticed, the input impedance is a function of transistor trans–conductances (gm1, gm2), parasitic capacitors (Cgs1, Cgs2) and output resistances (rds=1/gds).

In order to obtain a more accurate equivalent passive model, several steps must be followed, as presented hereinafter. First, it's important to notice that the TOSI equivalent passive model is obtained through a non–canonical decomposition of the input admittance (or impedance). In addition, the key in finding a more realistic RLC model is to synthesize the input admittance function without any approximation.

Taking into account (1) and synthesizing the input admittance, after rearranging the terms in (1) so that the parasitic parallel resistor R_p and capacitor C_p are obtained, a first order expression in the form (as+b)/(cs+d) is obtained. This factor naturally appears during the fraction decomposition and the model accuracy is strictly dependent on its synthesis. A common way, reported in several previous papers which focused on the model, is to approximate this term with b/(cs+d). However, as our simulations showed, this approximation affects the model accuracy, offering a much more simplified and not realistic RLC passive model, mainly for RF design. The methodology we propose in our work consists in a further decomposition of the first order expression as presented below (3):

$$
\frac{as+b}{cs+d} = \frac{as}{cs+d} + \frac{b}{cs+d} = \frac{1}{\frac{cs+d}{as}} + \frac{1}{\frac{cs+d}{b}} = \frac{1}{\frac{c}{a} + \frac{1}{\frac{a}{d}s}} + \frac{1}{\frac{c}{b}s + \frac{d}{b}} \tag{3}
$$

Since all fraction terms (a, b, c, d) are nonzero for any active inductor and the model obtained this way is to be used at higher frequencies in GHz domain, this decomposition (3) is valid and reveals two series branches (RC and RL) connected in parallel.

For further improvement of the model accuracy, all transistor parameters must be considered when computing the TOSI input impedance, including g_{mb} and current source output resistance. This is the second step and currently the input admittance can be expressed as it follows (4), where G_{eq} is the sum of g_{m2}, g_{mb2} and g_{ds2}.

$$
Y(s) = sC_{gs2} + g_{ds1} + \frac{1}{\frac{sC_{gs1}}{g_{m1}G_{eq}} + \frac{g_{ds2}}{g_{m1}G_{eq}}} + \frac{1}{\frac{1}{G_{eq}} + \frac{1}{sC_{gs1}G_{eq}/g_{ds2}}} \tag{4}
$$

A good matching between theory and practice while studying the RF behavior of MOSFET transistors only is achieved by using a suitable small signal MOSFET transistor model. In addition, the key element which sets the frequency response is represented by the transistor parasitic capacitors. Thus, it is well known that two different MOSFET models are currently developed [10]:

a) a *capacitor model* which considers reciprocal capacitors network for transistor;

b) charge based model, making using of trans-capacitances and considering capacitors as non-reciprocal elements.

These models offer different results but as stated in several RF books, the second model gives better results for GHz frequencies, up to 30% of the cut-off frequency. Excepting [3] where transcapacitances were taken into account, all references studying active inductors have used the capacitor model only even if the inductors were designed at higher frequencies. Since our inductor model is developed for GHz frequencies where significant errors are expected, the case b) is taken into consideration during our research and this represents also the third step in finding a more accurate TOSI passive model. Consequently, in the previous formula (4), total node capacitances – C(1), C(2), including Cgg, Cdd, Css, are considered instead of node to node capacitances (Cgs, Cgd, Cgb). This means that the gate to source capacitances are replaced with nodal capacitances in (2) and (3) which have adequate values. Moreover, since most TOSI configurations have no floating parasitic capacitors, as the inductor studied in this work, the use of the second model is advisable.

The final model proposed for TOSI architectures with input impedance of second order as described by (1-3) is presented in Fig. 2.

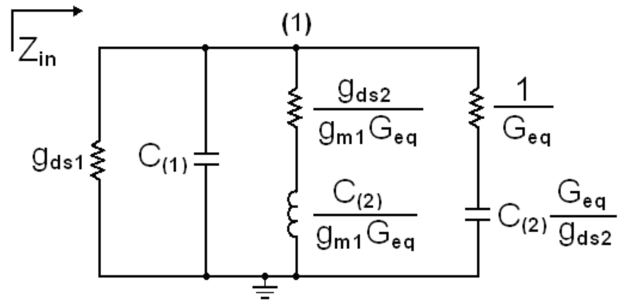

Figure 2. Proposed RLC model for CMOS active inductors

Compared to the classical RLC model, our proposed one contains a supplementary RC series branch (the fourth parallel one) which apparently raises the order of the circuit to three. However, since the synthesized circuit is not canonic i.e., there is a pole/zero cancellation explained by the dependencies between the inductive and capacitive branches parameters, the model order remains two. Since this model can be applied to any active inductor having the same input impedance/admittance and all TOSIs implemented with two transistors and having no floating parasitic capacitors are characterized by (1–2), the model is sufficient general. This proposed model is validated by simulations, as shown in Section 4. The utility of this proposed model resides in the theoretical accurate estimation of the simulated inductor parasitic elements and self resonant frequency. Finally, this "improved" model proves that a transistor only simulated inductor is much more than a simple RLC resonator, as considered until now.

III. IMPROVED ACTIVE INDUCTOR

Like any CMOS TOSI, the active inductor studied above has a very small quality factor. This is the reason why a compensation scheme must be used in order to decrease the intrinsic losses at the frequency of interest. The most common compensation method for VCOs and active inductors consists in using negative resistances, implemented with two cross–coupled transistors. In the most applications, the negative resistance is dc coupled therefore negatively changing the inductor biasing. In addition to a larger quality factor, obtained by connecting a negative resistance to an active inductor, always the self resonant frequency decreases while the quality factor increases. However, as reported in [12], it is possible to increase the self resonant frequency while using a negative resistance but only in conjunction with a supplementary positive gate resistance.

In this paper, a novel compensation scheme is proposed to active inductors, particularly for the basic cell shown in Fig. 1, considered in differential topology (Fig. 3).

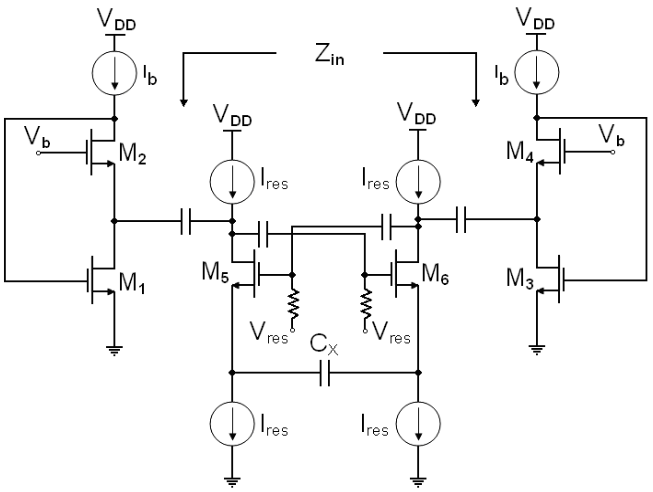

Figure 3. Active inductor with negative capacitance

Basically, it consists of a dc decoupled negative resistance, as previously used and described in [12] but improved in such way that it acts as a more general negative impedance converter. Thus, a small supplementary positive capacitor is connected between the sources of the cross coupled transistors, easy to implement practically by means of layout. Therefore, a negative capacitor must be seen by the active inductor at its inputs. The use of negative capacitors together with active inductors, as we propose in this communication, envisages the increase of inductor self resonant frequency with positive effects upon its frequency capability. No extra compensation scheme is required to increase the inductor quality factor since the negative capacitor already includes a negative resistance, as stated by (5), where $Z_{neg}(s)$ represents the negative resistance input impedance.

$$Z_{neg}(s) = -2/g_m - 1/sC_x \qquad (5)$$

Consequently, the active inductor will see at the input a negative resistance of value $R_{neg} = -2/g_m$ in series with a negative capacitance whose value is given by the supplementary shunt capacitor (C_X). Therefore, a double compensation is effectively implemented with a single scheme, an increase of the both self resonant frequency and inductor quality factor being expected. The positive results are shown in the following Section.

IV. SIMULATION RESULTS

For testing our proposed passive model (Fig. 2), the active inductor shown in Fig. 1a was biased at four different frequencies in the GHz domain. All transistor parameters were extracted and used to compute the both equivalent RLC models (classical and the proposed one). Finally, the frequency response of these three circuits was compared. The simulations showed a good matching between the results offered by our proposed model and the behavior of the real inductor, implemented with transistor and modeled. These results are further presented in Fig. 4.

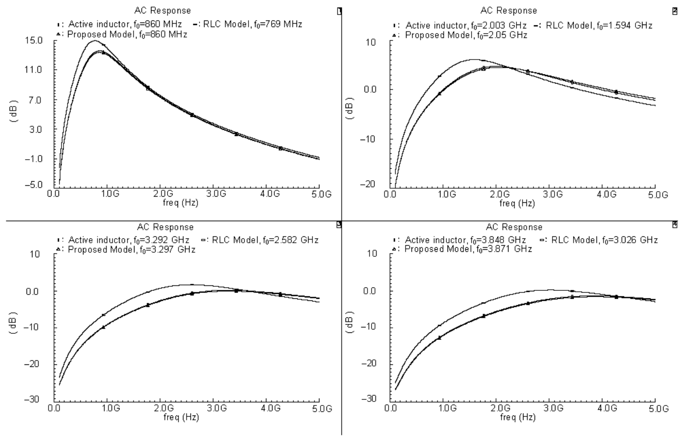

Figure 4. Frequency behavior comparison for the CMOS active inductor, RLC classical model proposed RLC model

Regarding the improved inductor architecture, it was biased at three resonant frequencies (1.5 GHz, 2.34 GHz and 3.3 GHz). Although a decrease of the self resonant frequency is expected due to the cross coupled transistors parasitic, the negative capacitor compensates these parasitics and consequently higher frequencies are obtained. Thus, our simulations showed a frequency increase of 1.1 GHz for the resonant frequency of 2.34 GHz, while about 1 GHz is obtained for the first and third cases. Large quality factors are obtained for each frequency and particularly with very small current consumption (< 350 µA). The current consumption is at least halved compared to the case of using negative resistances only.

An interesting aspect is that, besides frequency increase, this compensation method has relaxed constraints since one capacitor is enough for all three simulations (10 fF) while the current through the negative resistance is almost constant (~ 134 µA). In other words, the method is insensitive to the quality factor tuning at different frequencies. By its performances, this compensation scheme is superior to that proposed in [12]. In any case, higher current consumption is expected if high linearity, low noise and impedance matching are required for the final filter shown in Fig. 3.

The Simulation Results are illustrated in Figures 5–7. All simulations were carried out in a 0.18 um CMOS process.

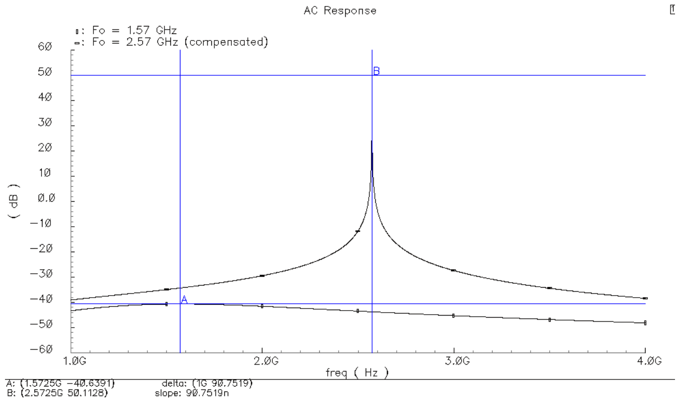

Figure 5. Frequency increase of 1GHz at F_o=1.57 GHz with compensation

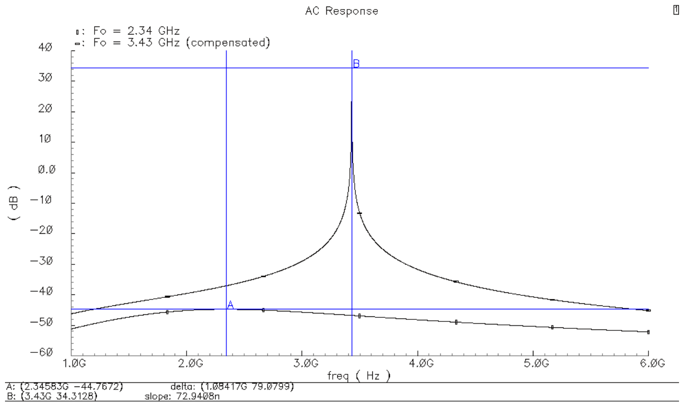

Figure 6. Frequency increase of 1.1 GHz at F_o=2.34 GHz with compensation

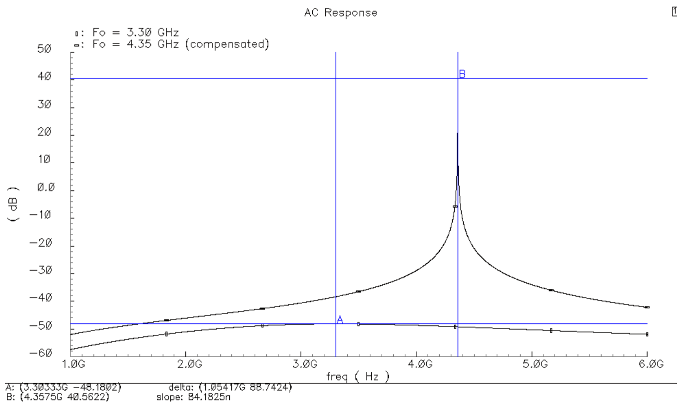

Figure 7. Frequency increase of 1 GHz at F_o=3.30 GHz with compensation

CONCLUSIONS

A more accurate equivalent RLC passive model has been proposed for CMOS transistor only simulated inductors. The new model has four branches but is still second order. Simulations have showed good accuracy for this proposed method, almost perfect matching between the frequencies results of the proposed model and the active inductor being noticed. In addition, a novel compensation scheme was applied to the same active inductor consisting of a more general negative impedance converter. A supplementary frequency increase of 1.1 GHz was obtained in the frequency range 1.5 GHz … 3.3 GHz, with a maximum current consumption of 350 µA. High quality factors are obtained with this compensation scheme but careful design must be applied to avoid the circuit instability.

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