

Wide Range 8ps Incremental Resolution Time Interval Generator based on FPGA technology

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Abstract—Accurate generation of picosecond-resolution wide-range time intervals has become a necessity for the characterization of time-to-digital converters involved in time resolved imaging. This paper presents the design and measurement of a time interval generator based on FPGA technology. Although it can be employed in different automatic test setups, it has been designed to characterize an array of time-to-digital converters. It can work as periodic pulse/ frequency generator but also as a digital-to-time converter. The accuracy of periodic pulse generator is around 20ps RMS jitter over a time range of 600ps to 33μs. The incremental time resolution is 8ps and the repetition rate is up to 2MHz. The accuracy of the digital-to-time converter is less than 0.8LSB DNL and 2LSB INL, whilst the time resolution is 27ps. Full characterization of the module is reported including a comparison with state-of-the-art instruments in this field.

I. INTRODUCTION

In the last few years, Time-of-Flight (ToF) 3D imagers based on Single-Photon Avalanche-Diodes (SPADs) are featuring promising figures of power consumption and pixel pitch towards high resolution integration [1]. Basically, the elementary cell in this kind of systems incorporates a SPAD detector and a Time-to-Digital Converter (TDC) [2]. This TDC is meant to evaluate the time elapsed between two consecutive electric pulses. The first one is given by the SPAD detector when a photon detection event occurs, while the second pulse comes from the synchronization signal that triggers the laser.

From the testability point of view, specific issues have to be addressed:

- (i) The test bench has to provide the means for full characterization of the TDCs array by estimating the *time resolution, uniformity* and *nonlinearities*. A commonly used method to measure the nonlinearities is the statistical code density test. This can be done either by using a test generator that delivers Poissonian distributed trains of pulses, or by employing a SPAD detector exposed to an uncorrelated light source. In both cases, the number of measurements should be large enough to cover the whole range with the maximum number of channels (i.e. time interval bins). An effective alternative proposed in this work is to use a linear Time-Interval-Generator (TIG), thus minimizing the number of measurements per time bin.
- (ii) For the sake of simplicity and flexibility, most of the ToF imagers have the control signals provided off-chip.
- (iii) Moreover, 3D image sensors rely on Time-Correlated Single-Photon Counting measurement techniques [3]. Therefore a large amount of data needs to be compiled off-

chip. One possibility is to send the data to a personal computer using an USB link.

In order to have a compact setup for test and characterization of a 3D imager, it is more convenient to embed in the same FPGA board the TIG, the control logic of the unit under test and the USB interface. This work is presenting only the design and characterization of the TIG module based on phase shifting method.

In order to properly characterize TDCs, the TIG has to deliver picosecond-accuracy time intervals which are delimited by the leading edge of successive START/ STOP pulses. The simplest approach to generate a preset time interval is to count a preset number of clock periods. To achieve a time interval granularity of 8ps, the counter needs to be driven by a clock reference of 125GHz. This is hardly possible even using the top high speed CMOS technologies. One possibility to avoid this limitation is to combine high dynamic range with high precision by splitting the conversion scheme in two stages. The first stage generates a coarse approximation of the time interval whilst the second one handles the fine tuning [4]. They are implemented by a large depth ripple counter and a Delay-Locked Loop (DLL), respectively. Our proposal is based on this approach.

The design is implemented on a Virtex-5 FPGA, incorporated on a ML505 development kit [5]. This FPGA has the advantage to incorporate Digital Clock Managers (DCMs) of 256 steps phase shift and low-jitter Phase Locked-Loops (PLLs) [6]. The TIG has been optimized to use the minimum resources. It can be configured as Periodic Pulse Generator (PPG) or Digital-to-Time Converter (DTC). The accuracy of the TIG running in the first mode is given by the FWHM or RMS jitter over a large number of measurements. In the second operating mode, the maximum value of the jitter impacts the minimum time resolution of the TIG. In other words, the jitter of the TIG as periodic signal generator traces the lower bound of the single shot precision (or LSB) of the DTC.

The proper functionality of the design has been proved by measurements. The PPG has an incremental time resolution of 8ps which is close to the state-of-the-art instruments [8]. The jitter of the pulse width is less than 20ps RMS, better than [7]. The 600ps lower limit of the time range is far below the 10ns reported [7], [8]. The DTC has an LSB of 27ps, better than previous implementation [7]. Moreover we achieved a better accuracy per phase offset word, featuring less than 0.8LSB DNL and 2LSB INL by averaging only 16 measurements.

These specifications allowed us to use the proposed TIG to test an array of 64x64 TDCs with a dynamic range up to 460ns.

II. TIME INTERVAL GENERATOR BUILDING BLOCKS

The TIG (Fig. 1) is composed of the clock generator (CG – Fig. 3), the pulse generator (PG–Fig. 4), and the additional control logic. The first module provides CLK1 and CLK2 from an external reference clock. These two clocks have to be stable before the synthesis of the time interval starts. The second block generates the START, STOP and WIDTH signals.

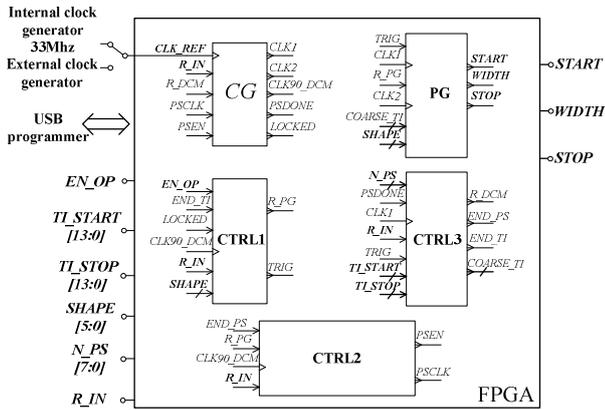


Fig. 1. Block diagram of the TIG

The control logic is aimed to provide: (i) the reset and trigger signals for CG and PG, (ii) the required signals for phase shifting, (iii) the signals to control the fine and coarse approximation. All the component modules have been low level designed to use the minimum resources and keep the signal path as short as possible.

Before any time interval generation starts, the PG module is reset and the DLL is set with the appropriate phase. After the DLL is locked, the internal trigger enables the time interval generation. Further, on the positive edge of CLK1 a START pulse is sent. When the preset number of T_{CLK1} is reached, the STOP pulse is delivered on the first positive edge of CLK2 as shown in Fig. 2. The coarse value of the synthesized time interval is made by merely counting the full periods of CLK1. Its fine value is obtained by delaying CLK2 against CLK1 with the proper time bin.

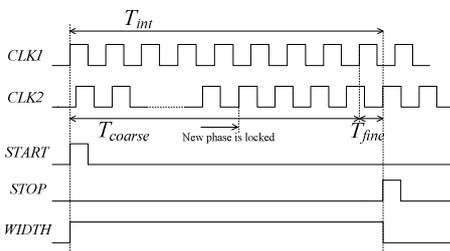


Fig. 2. Chronogram of the TIG

As already mentioned in the previous section, the only way to achieve picosecond time resolution is by applying time interpolation [4]. In this paper time interpolation is based on phase shifting, using the DCM of the FPGA as a DLL.

$$T_{int} = T_{coarse} + T_{fine} = N \times T_{CLK1} + M \times T_{bin} \quad (1)$$

where N, M are the integer number of coarse periods and time bins of the delay line. The maximum number of N, M that can be synthesized depends on the long term stability of the reference clock and the maximum number of steps in the delay line respectively.

A. The timing block

The incremental resolution needs to be traded with the linearity of the DTC. In other words, smaller incremental resolution leads to stronger nonlinear behavior of the DTC. In order to reach the smaller incremental resolution claimed above, one has to use the maximum frequency allowed by the DCM in Virtex-5 FPGA. This can be done by using a PLL2DCM instance which is a low jitter IP core [9].

If the single-shot linearity is more important, then there is no need to push the incremental time resolution beyond the maxim jitter. Therefore CLK1 can be lowered and only an IP core of DCM set as a DLL is enough. Both possibilities are considered below.

1) Clock generator based on PLL2DCM

In order to get a minimum incremental resolution of 8ps, the timing block need to provide two clocks of 488MHz. This scenario is obtained by using a PLL2DCM IP core block. The schematic is depicted in Fig. 3. The PLL is fed by a reference clock. The synthesized output CLK1 is used to trigger the START pulse. The same clock is also driven the DCM. The shifted version of this clock, CLK2 is used to trigger the STOP pulse. The DLL is shifting the phase in 256 steps. In this arrangement, the coarse and fine periods from (1) are the PLL period and DLL tap respectively.

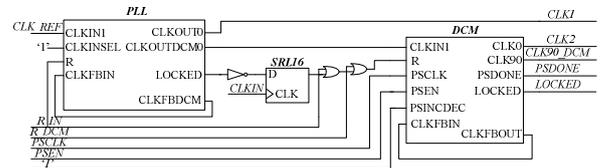


Fig. 3. Clock generator (CG) based on PLL2DCM IP core

2) Clock generator based on DCM

The clock generator block in this case has only a DCM configured as DLL. It is clocked by an external reference of 145MHz. This means a time bin, T_{bin} of 27ps. On the positive edge of CLK1 it is triggered the START pulse. CLK1 is delayed by the DCM into CLK2 whose positive edge triggers the STOP pulse.

$$T_{int} = N \times T_{CLK1} + M \times T_{bin} + T_{offset} + PS \quad (2)$$

T_{offset} is the delay introduced on the signal paths of CLK1 and CLK2. It is compensated by the fixed phase shift (PS) which is set in the DLL.

B. The pulse generator block

The module is clocked by CLK1 and CLK2 provided by CG. The N bit counter, CNTN handles the coarse approximation. It is enabled by an internal trigger, TRIG which set up the START pulse on the positive edge of CLK1. This

Fig. 6b has been obtained with the CG based on the DCM. The characterization of the PPG is extended up to 33 μ s because this is the maximum range that PICOHARP 300 can measure. The value of the jitter is expressed both in RMS and FWHM values.

B. Digital to time converter (DTC)

In this setup TIG operates as a linear DTC. To have a monotonic single-shot converter, the incremental step has to be larger than the maximum jitter which is less than 100ps. The CG is based on DCM and the external reference clock is about 145MHz. Therefore the incremental step is set to 27ps. In this case less than 3LSB DNL and 2.5LSB INL are obtained per coarse time interval period. The DTC monotonicity is affected by the jitter. At this point the only way to increase the accuracy is by averaging different measurements. If each step is repeated by M times then the accuracy improves \sqrt{M} times. The improvement is shown in Fig. 7. The results are obtained by averaging 16 measurements. Subplots a) and b) depict the DNL and INL over 460ns range. The accuracy is less than 0.8LSB DNL and 2LSB INL.

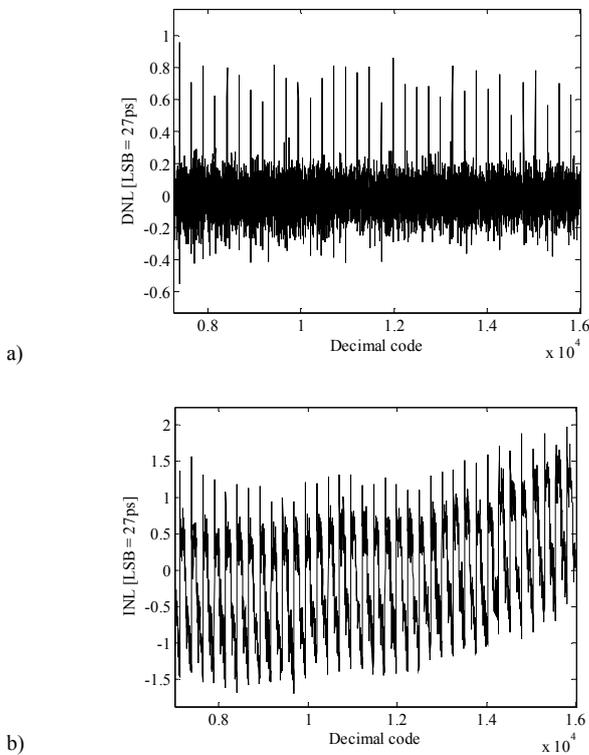


Fig. 7. DNL (a) and INL (b) vs. decimal code

IV. CONCLUSION

Compact automatic control and test setup for 3D imagers is highly desirable for portable applications. Both, the test, control and data modules can be implemented on the same FPGA development board. The design and characterization of a TIG implemented on Virtex-5 FPGA is reported. It is based on phase-shift method and is able to work as PPG or DTC. In the first operating mode the jitter is less than 20ps RMS in the

range of 600ps to 33 μ s. The incremental resolution is 8ps. For the second operating mode the LSB is 27ps. The accuracy over 16 measurements is less than 0.8LSB DNL and 2LSB INL. We achieved better results in terms of jitter, lower time range limit and accuracy than the implementation based on SPARTAN-3 FPGA [7]. The proposed TIG has been used to test a 64 \times 64 3D imager with in-pixel TDCs. The USB link still has to be integrated on the FPGA in order to have a stand-alone test board for this kind of image sensors.

TABLE I. SPECIFICATIONS COMPARISON

Feat.\Ref.	[8]	[6]	This work
Integration	T5300U	Spartan-3	Virtex-5
Range	10ns – 10s	4ns – 50ms	600ps – 33μs
Inc. resolution	5ps	35ps	8ps
Jitter	<28ps RMS	<65	<20ps RMS
LSB of DTC	-	32ps	27ps
DNL/ INL	-	-/ 3LSB	0.8/ 2LSB
Trigger generator	10mHz – 1Mhz	-	30.3kHz – 2Mhz

ACKNOWLEDGMENT

This work has been funded by Office of Naval Research (USA) grant No. N000141410355, the Spanish Government through projects TEC2012-38921- C02 MINECO (European Region Development Fund, ERDF/FEDER), IPT-2011-1625-430000 MINECO, IPC- 20111009 CDTI (ERDF/FEDER) and Junta de Andalucía, Consejería de Economía, Innovación, Ciencia y Empleo (CEICE) TIC 2012-2338

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