

A Ferroelectric Tunnel Junction-based Integrate-and-Fire Neuron

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Abstract—Event-based neuromorphic systems provide a low-power solution by using artificial neurons and synapses to process data asynchronously in the form of spikes. Ferroelectric Tunnel Junctions (FTJs) are ultra low-power memory devices and are well-suited to be integrated in these systems. Here, we present a hybrid FTJ-CMOS Integrate-and-Fire neuron which constitutes a fundamental building block for new-generation neuromorphic networks for edge computing. We demonstrate electrically tunable neural dynamics achievable by tuning the switching of the FTJ device.

Index Terms—Integrate-and-Fire Neuron, FTJ, HZO, neuromorphic computing, edge computing.

I. INTRODUCTION

Event-based neuromorphic systems where data is processed asynchronously as spikes are an attractive solution for low power edge computing. The basic computing blocks in such systems are artificial neurons and synaptic circuits. While there has been significant effort to develop CMOS neurons and synapse circuits [1], the recent developments in emerging devices provides an opportunity for integration with CMOS technology to design neuron and synaptic circuits that can be power and area efficient compared to their CMOS only counterparts [2]. Among the various emerging devices, ferroelectric tunnel junctions (FTJ) feature ultra-low switching energy [3]. Hafnium Zirconium Oxide ($\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$; HZO) based FTJ devices can be integrated on the CMOS back-end-of-line enabling hybrid FTJ-CMOS circuits [4]. Despite growing interest in synaptic applications of HZO FTJs [5], neuron circuits have not been much explored. The HZO FTJ device features thresholding behavior in resistance change which is useful for neuron circuits. In this context, we present a hybrid FTJ-CMOS Integrate-and-Fire neuron circuit. The

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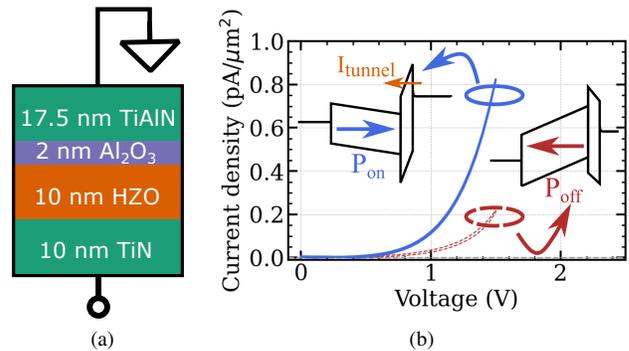


Fig. 1: (a) Schematic of the FTJ stack. (b) DC-IV measurements of the FTJ in ON and OFF state, measured up to 1.5 V. Schematics of the corresponding band structures are shown in the inset.

circuit utilizes an HZO-based bilayer FTJ device that realizes the pulse integration. The circuit can become a building block for low-power neuromorphic systems.

II. GRADUAL SWITCHING PROPERTIES OF FTJ DEVICES

Fig. 1a shows the HZO based bilayer FTJ device considered in this work. Details of the FTJ device fabrication can be found in [6]. The operation principle of the devices is shown through band diagrams in the insets of Fig. 1b. When the ferroelectric polarization (blue/red arrows) points towards the Al₂O₃ layer, an electric field is induced which results in the ON state defined by a high tunneling current. When the polarization points away, the band bending results in a larger tunneling barrier width and an OFF state with a low tunneling current. The polarization is switched ON (set) by applying 5 V, and switched OFF (reset) by applying -5 V. The polarization can be partially switched by using lower voltage amplitudes or shorter pulse times. The currents of these intermediate states are directly proportional to the amount of switched polarization [7]. In order to study gradual switching under identical set or reset pulses (representing spikes) for the neuron integration function, the switching under multiple square pulses with fixed amplitude and width was characterized. Variable numbers of voltage pulses were applied to the device and the switched

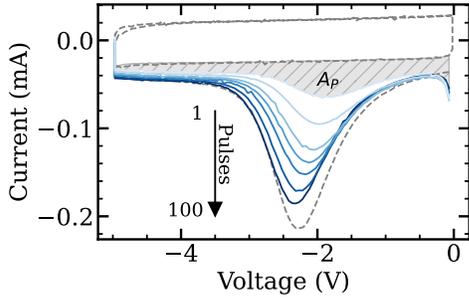


Fig. 2: Measured FTJ reset currents after an exponentially increasing amount of pulses with amplitude 4 V and length 10 μ s. The shaded area A_p is integrated to obtain the polarization in Fig. 3. The dashed line represents the complete switching process with a single -5 V, 500 μ s triangular voltage pulse.

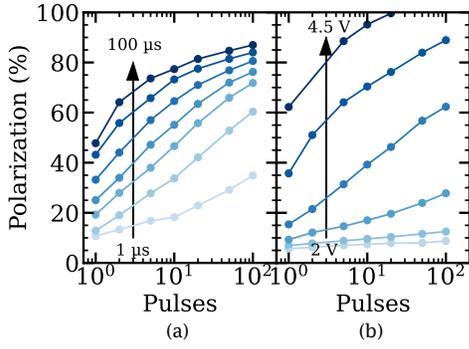


Fig. 3: Measured switched polarization as a function of the number of applied pulses, for (a) exponentially increasing pulse widths at 3.5 V and (b) different voltages in steps of 0.5 V at a pulse width of 10 μ s. The polarization is normalized to a full switching measurement.

polarization was measured by switching the device back with a single, triangular -5 V, 500 μ s pulse [7]. Fig. 2 shows the back-switching current after gradual switching with pulses of 4 V amplitude and 10 μ s width. Based on the non-switching current measured on a second back-switching pulse, the switching current and accordingly the switched polarization can be measured, which is illustrated by the shaded area in Fig. 2. Complete switching was measured under a triangular voltage pulse with amplitude 5 V and width 500 μ s. An evaluation of the switched polarization for different pulse widths and an amplitude of 3.5 V (Fig. 3a), as well as for different voltages with a pulse width of 10 μ s (Fig. 3b) supports the viability of the gradual switching approach employed in the neuron circuit.

III. FTJ COMPACT MODEL

For the circuit simulations, a compact model based on a HZO ferroelectric capacitor was used. Here we provide a summary of the salient aspects of the model. For a more detailed description, please see [8]. We do not model a two-layer structure, rather we take the Al_2O_3 layer into account by adapting the value of the effective coercive field E_C to

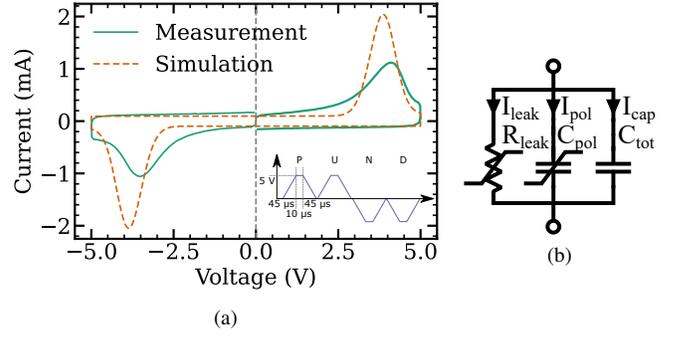


Fig. 4: (a) Switching I-V characteristic obtained with 100 μ s wide trapezoidal excitation (shown inset) and the equivalent simulated I-V obtained using the compact model. (b) Equivalent circuit.

represent the capacitive divider we have in our FTJ. The HZO layer consists of a mix of ferroelectric, antiferroelectric, and paraelectric phases due to the fabrication process. Therefore, the total capacitance of the FTJ is modeled as the parallel of a ferroelectric capacitor and a dielectric one (Fig. 4b).

The FTJ model is based on the Preisach model of ferroelectric hysteresis and has been calibrated to fit the characteristics of the device discussed in Section II. The Preisach model describes the evolution of the polarization P as a function of applied electric field E [9]. We calculate the asymptotic polarization for a certain voltage following Miller et al. [10] as:

$$P(E, k, P_{off}) = k \cdot P_{sat} \cdot \tanh\left(\frac{E_{eff} \pm EC}{2\delta}\right) + P_{off} \quad (1)$$

where k and P_{off} are a scaling factor and the offset polarization, respectively, used to account for unsaturated loops [11], P_{sat} is the saturation polarization, E_{eff} the field applied to the ferroelectric layer, and δ is:

$$\delta = EC \left(\ln \frac{1 + P_r/P_{sat}}{1 - P_r/P_{sat}} \right)^{-1} \quad (2)$$

where P_r is the remanent polarization. The switching kinetics is added to the model by using the static polarization P as in (1) and adding a time dependence to find the dynamic polarization P_{dyn} :

$$P_{dyn} = \frac{P \Delta t + P_{old} \cdot \tau_{pE}}{\tau_{pE} + \Delta t} \quad (3)$$

Δt is the actual time-step of the simulation, P_{old} is the polarization calculated in the previous time-step, and τ_{pE} is

$$\tau_{pE} = \tau_p 10^{\alpha_E \left(\frac{EC}{10} + abs(E_{eff}) \right)} \quad (4)$$

where τ_p and α_E are fitting parameters.

TABLE I: Values of the parameters used to calibrate the compact model.

Parameter	Value	Parameter	Value
E_C	3.3 MV/cm	τ_p	10 μ s
k	0.5	α_E	0.25
P_{sat}	20.0000 μ C/cm ²	A_{tot}	3.14 · 10 ⁻⁴ cm ²
P_r	19.9997 μ C/cm ²	R_{A0}	110 μ A
V_{P0}	0.36 V	ΔV_P	0.06 V

Each change in the polarization results in a polarization current, I_{pol} , modeled through the ferroelectric capacitor (Fig. 4b):

$$I_{pol} = \frac{dP_{dyn}}{dt} \cdot A_{tot} \quad (5)$$

The actual state of the FTJ is given by a current, I_{leak} , flowing through a non-linear resistor placed in parallel to the capacitors. The current through this resistor depends on the polarization state of the ferroelectric layer (Fig. 4b):

$$I_{leak} = R_{A0} A_{tot} \left(e^{\frac{V}{V_{PE}}} - 1 \right) \quad (6)$$

where R_{A0} is a fitting constant dependent on the ferroelectric material stack, A_{tot} is the area of the FTJ, V is the applied voltage, and V_{PE} is a polarization-dependent variable:

$$V_{PE} = V_{P0} - \Delta V_P \cdot \frac{P_{dyn}}{P_{sat}} \quad (7)$$

with V_{P0} and ΔV_P fitting constants.

Fig. 4a compares a typical measured and simulated I-V characteristic of our FTJ devices measured with 100 μ s-wide trapezoidal positive-up-negative-down pulses. The simulation was obtained using the values from Table I. The model agrees well with the capacitive behavior and the coercive voltage V_c of the device (V_c is higher than in Fig. 2 due to the measurement frequency). The evolution of the polarization, given as the integral of the I-V curves, is roughly the same, but the simulated switching current is higher and narrower than the measured one (about 2.1 mA peak current obtained in the simulation versus 1.1 mA measured in the device). Notably, the simulation yields a Gaussian current peak which is not observed experimentally. This is due to the model assumption of a statistically independent switching of domains.

IV. FTJ-BASED INTEGRATE-AND-FIRE NEURON

The very low leakage current in FTJ devices (see Fig. 1b) allows very energy efficient operations, but poses a challenge in reading the memory state. The proposed circuit, shown in Fig. 5, adopts a variation of the 2 transistor-1 capacitor (2T1C) readout scheme (T_1 to T_4 in Fig. 5) which uses a read transistor T_4 to amplify the signal from the FTJ [12]. The circuit was designed in a standard 180 nm CMOS technology. Transistor T_3 is added to prevent any disturbance to reach the gate of T_4 during the writing phase. Two inverters with tunable switching threshold (T_4 to T_7) are used in order to obtain sharp pulses starting from a slow changing input signal [13]. The PMOS gate voltages (V_{p1} and V_{p2}) are used to tune

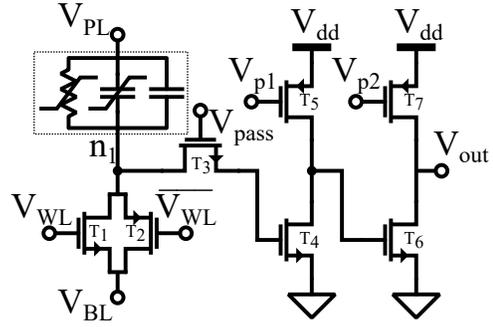


Fig. 5: Integrate-and-Fire neuron schematic. Transistors T_1 to T_4 implement a variation of the 2T1C cell [12]. Transistors T_4 to T_7 implement two inverters with electrically tunable switching threshold.

the switching threshold of the inverters. During the writing operation (green and purple shades in Fig. 6a), transistors T_1 , T_2 are turned ON through V_{WL} , while the pass transistor T_3 is OFF. Voltage pulses, negative to reset and positive to set, are applied at the plate line (PL) while the bit line (BL) is kept at a constant voltage. The reading operation (orange shade in Fig. 6a) is divided in two different phases, pre-charge and integration. During the pre-charge phase (2 μ s, evidenced by the overlapping of the orange shade with the green / purple one in Fig. 6a), transistors T_1 , T_2 , and T_3 are turned ON, thus charging node n_1 to V_{BL} . V_{BL} is chosen near the switching voltage of the first inverter, in the high-gain region. Then the integrating phase begins. T_1 , T_2 are turned OFF so that BL is disconnected, leaving n_1 floating, and a read voltage (V_{read}) is applied to PL . Under these conditions, the FTJ discharges, i.e., the voltage at n_1 (V_{n1}) increases, because of the FTJ leakage current. Indeed, the device can be modeled as an RC circuit where the capacitance is constant and the resistance is proportional to the polarization (see Sect. III). The final V_{n1} after a read phase of 100 μ s depends on the resistance of the FTJ. If it is higher than the switching voltage of the first inverter, V_{out} rises and the neuron fires, as shown in Fig. 6a. Fig. 6b shows V_{n1} during each read phase shown in Fig. 6a. The slope of n_1 depends on the state of the FTJ and the difference between the final voltage at the end of the reading phase after the first and the last pulse is of almost 20 mV.

It is worth noting that the signals which provide the full functionality of the neuron (e.g., bias and pulse generators) have to be generated outside the neuron itself, although on the same chip. However, the additional circuit can be shared among several neurons when using an asynchronous, event-based approach. Each single neuron can process event occurring at a minimum time distance of 150 μ s. The limit on the bandwidth imposed by the necessary integration time of the single neuron is overcome in scaled systems with a large number of neurons [14].

The choice of V_{read} is critical, as there is only a small window where a readable leakage current is obtained (see Fig. 1b) without modifying the polarization. Therefore, a

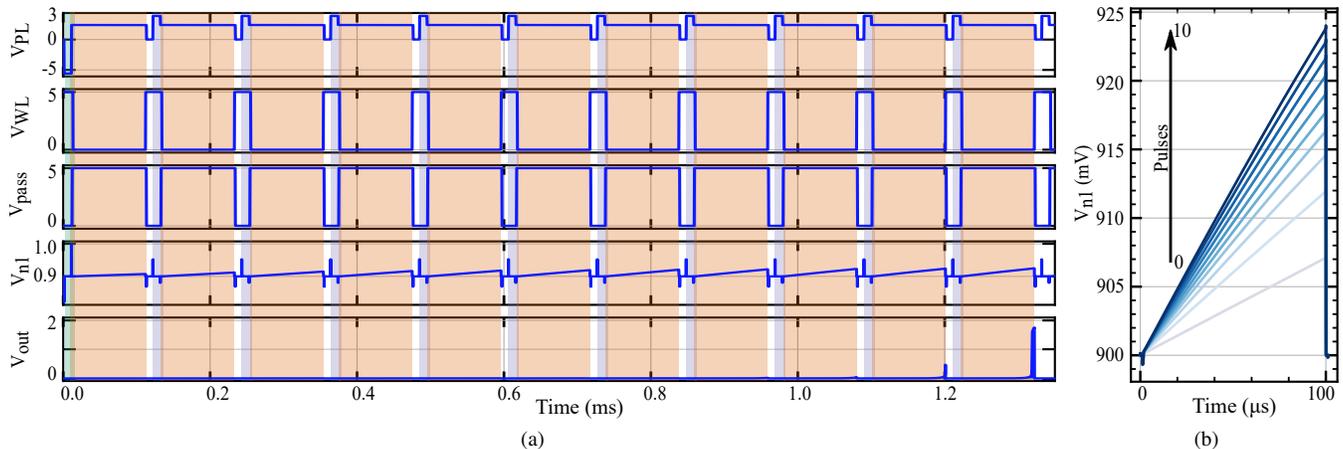


Fig. 6: (a) Simulation of the neuron behavior from the initial condition (reset) to the first spike. The green shade highlights the reset operation, the purple the set operation, and the orange the integrating phase. The pre-charge phase occurs where the different colors (green and orange, purple and orange) are overlapping. All the y axes are given in V. (b) Evolution of node n_1 during the reading phases shown in (a).

voltage of 1.5 V was chosen. Other important parameters for the performance of the neuron are the BL voltage V_{BL} and the integration, i.e., read, time. Decreasing the integration time and/or reducing V_{BL} slows down the neuron response, i.e., increases the number of pulses needed before the firing event.

The reset can be performed by applying a strong negative pulse (-5 V for 10 μ s) or by applying 5 V at the BL while keeping the PL at 0 V. The behavior of the neuron, i.e., the number of pulses needed to fire, can be modulated by changing the parameters of the set pulse. In accordance to the experimental data (Fig. 3), we can observe in Fig. 7 that a change in the set pulse amplitude or time width results in a different number of pulses needed before the firing event. It is observed that higher voltages / longer times lead to firing with a lower number of pulses. From the perspective of circuit design, it would be more convenient to exploit the time- rather than voltage-dependence of the FTJ. However, the FTJ shows a better modulation with voltage amplitude than time width. A change in voltage of 2.5 V results in a gradual reduction of pulses before fire, from 43 to 1 for 10 μ s pulses. When fixing the voltage at 3 V and modulating the pulse width, a sharp reduction is instead observed between 10^{-6} and 10^{-5} s, from 43 to 10 pulses before fire. This hardly changes for pulse widths over the next two orders of magnitude. One way to improve flexibility in the neural behavior and cope with process variability, both at circuit and at device level, whilst still keeping the design compact can be by changing the values of V_{p1} and V_{p2} to change the switching thresholds of the inverters. More specifically, a higher voltage at the gate of T_5 , T_7 lowers the switching threshold of the inverters.

V. CONCLUSIONS

In this work, a novel hybrid FTJ-CMOS neuron circuit design and simulations are presented. The integration function in the neuron can be achieved by accumulative polarization

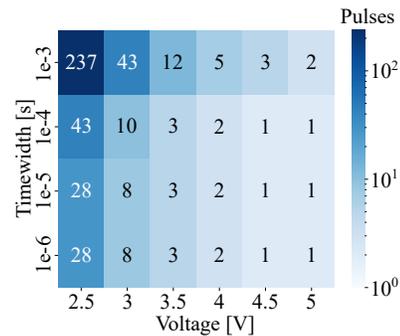


Fig. 7: Simulated number of pulses before a firing event as a function of the voltage amplitude and of the time width of the set pulse. The number of pulses is written inside the colored square.

switching behavior, which has been demonstrated experimentally in FTJ devices under application of identical pulses. The read current through the FTJ is amplified by the CMOS circuits and leads to the firing event. We simulated the pulse number needed for firing and its dependence on voltage pulse amplitude and width. The possibility of electrically tuning the neural dynamics by controlling the switching of the FTJ makes the proposed neuron suitable as a fundamental building block in new-generation neuromorphic computing systems.

REFERENCES

- [1] E. Covi *et al.* *Front. in Neurosci.*, p. 429, 2021.
- [2] E. Covi *et al.* in *IEEE Int. Conf. Flexible and Printable Sensors and Systems (FLEPS)*, 2022.
- [3] B. Max *et al.* *J. Electron Devices Soc.*, vol. 7, pp. 1175–1181, 2019.
- [4] V. Deshpande *et al.* *Solid-State Electronics*, vol. 186, p. 108054, 2021.
- [5] B. Max *et al.* *ACS Appl. Electron. Mater.*, vol. 2, no. 12, pp. 4023–4033, 2020.
- [6] S. Lancaster *et al.* in *IEEE ESSDERC*, 2022 (Accepted).
- [7] S. Lancaster *et al.* *Appl.d Phys. Lett.*, vol. 120, no. 2, p. 022901, 2022.

- [8] S. Slesazeck, "D2.4 Provide initial FTJ SPICE model for adoption in Task 5.3." <http://www.beferosynaptic.eu/deliverables>, 2021.
- [9] F. Preisach *Zeitschrift für physik*, vol. 94, no. 5, pp. 277–302, 1935.
- [10] S. Miller *et al. J. Appl. Phys.*, vol. 68, no. 12, pp. 6463–6471, 1990.
- [11] B. Jiang *et al. in IEEE Symp. VLSI Tech.*, pp. 141–142, 1997.
- [12] S. Slesazeck *et al. in IEEE Int. Memory Workshop (IMW)*, 2019.
- [13] V. Kornijcuk *et al. Frontiers in Neuroscience*, vol. 10, p. 212, 2016.
- [14] S. Moradi *et al. IEEE Trans. Biomed. Circuits Syst.*, vol. 12, pp. 106–122, 2017.