Delta-Sigma Modulator Design Using a Memristive FIR DAC

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***Abstract*— This paper proposes the design of a first-order single-bit continuous-time Delta-Sigma modulator using a memristive finite impulse response (FIR) digital-to-analog converter (DAC) in the feedback. To achieve better power and circuit area efficiency, the coefficients of the 8-tap FIR filter are implemented using memristors with programmable resistance in the range of 17.20kΩ to 55.63kΩ. The modulator was designed and simulated using a 180nm standard CMOS technology in addition to a memristor model, which was constructed based on the measured characteristics of the real device behavior. The modulator targets 10kHz signal bandwidth and samples at 10MHz. Simulation results show that the FIR DAC can improve the modulator signal-to-noise and distortion ratio (SNDR) from 44.36dB to 62.29dB with the existence of 5ns RMS jitter at the sampling clock. The FIR DAC still contributes to a better modulator SNDR performance even considering a worst-case 20% resistance variation of the memristors.**

Keywords*— *memristor, continuous-time Delta-Sigma modulator, FIR DAC.

I. Introduction

Continuous-time Delta-Sigma modulator (CTΔΣM) is a type of analog-to-digital converter (ADC) that can achieve high resolution through oversampling and quantization noise shaping with the continuous-time loop filters. Compared with the discrete-time counterpart, its inherent anti-aliasing property eases the requirement for preceding stage anti-aliasing filters, making it highly attractive for the analog front-end designs in sensor and communication systems [1][2]. A single-bit CTΔΣM is simplest to implement, but the feedback signal is at full scale, which places a high linearity requirement on the loop filter. It is also sensitive to clock jitter and quantizer metastability and requires a higher sampling frequency to reach the desired signal-to-quantization-noise ratio (SQNR), which can, on the contrary, increases the in-band noise floor due to signal-dependent quantization delays resulting from the reduction in the available regeneration time for the latches [1]. These limitations are tackled in a multi-bit CTΔΣM, but a multi-bit quantizer consumes more power, and it is difficult for the feedback DAC to maintain linear at high clock rates, which limits the speed of operation [2].

To combine the merits of both the single- and multi-bit CTΔΣM, an FIR DAC can be used in the feedback path with a single-bit quantizer, as shown in Fig 1(a). The FIR DAC has an embedded FIR filter which attenuates the shaped quantization noise and effectively reduces the step size of the feedback waveform, thus relaxing the loop filter's linearity requirement and reducing the modulator's jitter sensitivity. The architecture of an N-tap FIR DAC is shown in Fig. 1(b), which can be implemented in a semi-digital fashion using digital delay elements (a chain of flip-flops) and analog coefficients (e.g., using resistors [1]). Unlike multi-bit DAC, the FIR DAC does not require precise matching of the analog

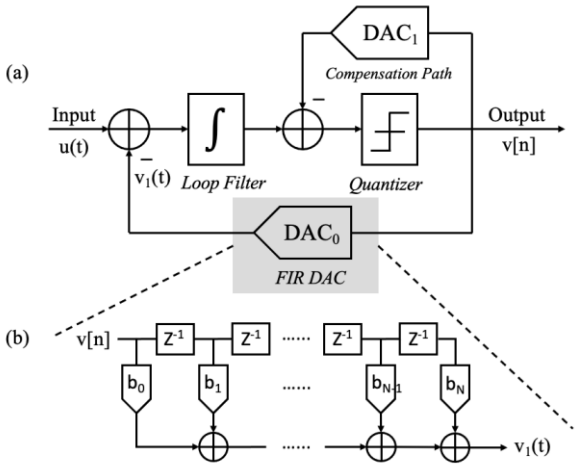


Fig. 1. (a) First-order CTΔΣM with an FIR filter in the feedback path. (b) N-tap FIR DAC in this work.

elements to achieve high linearity. The excessive loop delay (ELD) induced by the FIR operation can be compensated by adding a direct path from the quantizer output to its input, as shown in Fig. 1(a).

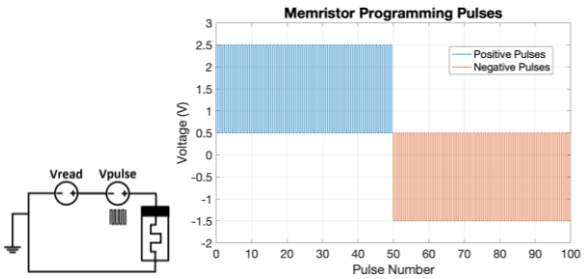
In this work, we propose a CTΔΣM design with a memristive FIR DAC where the analog FIR coefficients are implemented using memristors. Memristors are high-density devices whose resistance can be programmed by applying voltage pulses; the resistance states are sustained when the programming voltage is removed or is lower than the threshold for resistive switching [4]. Besides, the memristors can be integrated with CMOS back-end-of-line process in 3D and thus do not occupy additional silicon area when they are placed on top of the CMOS circuitry [5]. Therefore, a memristive FIR DAC will have better reconfigurability, area, and power efficiency compared with the implementations using passive resistors [6]. The concept of memristive FIR was proposed in [3], and this work is the first demonstration of using memristive FIR for CTΔΣM design.

This paper is structured as follows: Section II introduces the memristive FIR DAC design; Section III describes the architecture of the first-order single-bit CTΔΣM, including a memristive FIR DAC in the feedback. Simulation results of SNDR and ENOB on the CTΔΣM, including and excluding the FIR DAC, are assessed in Section IV.

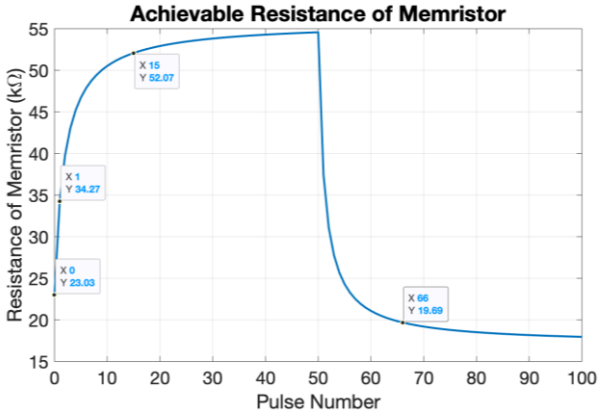
II. Memristive FIR DAC

A. Memristor Modelling

In this design, we use the device model in [6], which was constructed based on the measured characteristics from the real fabricated Pt/Al_2O_3/TiO_2/Pt stack memristors. The device can be programmed using voltage pulse trains to reach the



(a)



(b)

Fig. 2. (a) Memristor programming pulses; (b) the memristor resistance in response to the programming pulses in (a), which proves the resistance values for the memristive FIR DAC used in Fig. 3 are achievable.

resistance required for the FIR coefficients. By using reconfigurable memristors, filters with different transfer functions can be achieved by reprogramming the memristors representing FIR coefficients.

The simulation testbench to program and read the memristor is shown in Fig. 2(a), where the device was programmed with a train of 2V-amplitude and 100µs-wide pulses in accordance with the guidelines given in [6]. The verified resistance switching range of the memristor is 17.20kΩ to 55.63kΩ, as shown in Fig. 2(b). The resistance was read out using 0.5V voltage, which is below the switching threshold voltage, so that the resistance is not affected by the reading process. When using the memristors in the modulator, their resistance will first be programmed to the values that are required for the corresponding FIR coefficients. Then during the modulator operation, the voltage across the memristors must be maintained below the 0.5V switching threshold so that the FIR coefficients stay constant.

B. FIR DAC Design using MATLAB

FIR filter is a digital filter containing several delay cells, weights for the delayed signals to be multiplied, and a summing circuit, as shown in Fig. 3. The coefficients b_i of the filter are achieved through the equation

$$b_i = \frac{R_f}{M_i} \tag{1}$$

R_f is the resistance of the summing amplifier's feedback resistor, and M_i is the resistance of the i^{th} memristor, which corresponds to the i^{th} -tap FIR coefficients.

The FIR filter was designed using the digital filter function in MATLAB, where the filter's coefficients were synthesized based on the filter type, tap number, cut-off frequency, and passband/stopband ripple requirement. The filter designed has a Chebyshev window, which has a high roll-off rate and flat passband. The tap number was set to 8, sidelobe attenuation to 25dB, and normalized cut-off frequency to 0.01, which was optimized for the best filter performance with the existing resistance range of the memristors. R_f was set to 3.5kΩ, and the required memristor resistances were calculated using the coefficients synthesized from the MATLAB function.

C. FIR DAC Implementation

Delay cells, memristors corresponding to the filter coefficients, and the summing amplifier are required to construct the FIR DAC. Delay cells are implemented using D flip-flops, with their output voltage ranging from 0 to VDD (1V). The summing amplifier has a common-mode voltage of VDD/2 (0.5V). Therefore, the voltage swing across the memristors is limited to within 0.5V, which is lower than the threshold for resistive switching. This ensures that the resistance of memristors does not vary during modulator operation.

The schematic of the 8-tap memristive FIR DAC is shown in Fig. 3. Fig. 2(b) verified that the memristors could be programmed to achieve the required resistances. M1 and M8 can be programmed with 15 positive pulses, M2 and M7 with one positive pulse, and M4 and M5 with 50 positive and 16 negative pulses. The FIR filter was then implemented with circuits and simulated in Cadence, and the obtained frequency response of the FIR DAC is almost identical to the results from MATLAB, as shown in Fig. 4.

III. Delta-Sigma Modulator Design

A first-order single-bit CTΔΣM was designed, including the memristive FIR DAC in the feedback path, as shown in Fig. 5. The sampling frequency is 10MHz, and OSR is 500 for a target signal bandwidth of 10kHz. It contains four components, an active-RC loop filter, a single-bit quantizer, an auxiliary DAC_1 for ELD compensation, and a main DAC_0 in the feedback path. DAC_0 and DAC_1 are both memristive FIR DACs.

In practice, there is a delay in the quantizer to resolve the analog input; hence the FIR DACs in the feedback should be

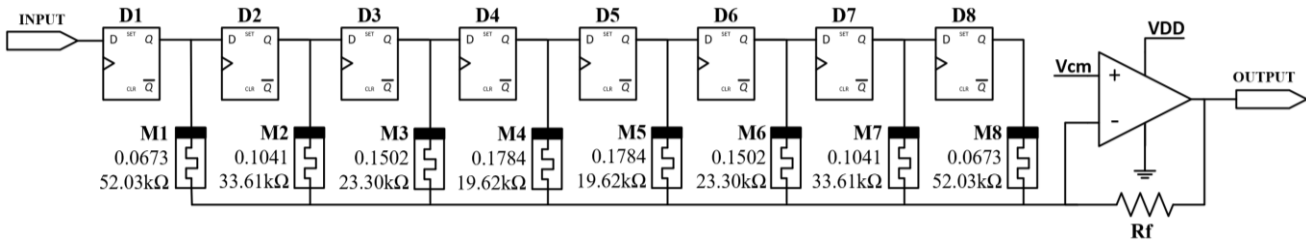


Fig. 3. 8-tap memristive FIR DAC.

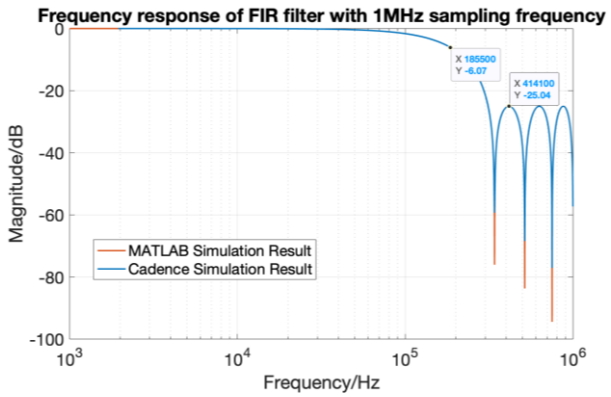


Fig. 4. Frequency response of the FIR filter

clocked with a delay compared with the quantizer [2]. In this design, the quantizer samples the loop filter output at the clock rising edge, and the quantization output is sampled by the FIR DAC at the falling edge; this allows a half-cycle regenerating time for the output of the modulator, effectively reducing its sensitivity to signal-dependent jitter [1]. This method introduces a half-cycle delay, which can be compensated using a direct path across the quantizer. The direct path includes a gain *k,* which equals to the half-cycle delay time, controlled by the resistance f_c, as shown in Fig. 5. This path is connected to the modulator through a unity-gain amplifier.

As shown in Fig. 6(a), a two-stage operational transconductance amplifier (OTA) with miller compensation was designed to implement an OTA-RC integrator with transfer function -1/sRC. The single-bit quantizer was implemented using a StrongArm latch [7] with the schematic shown in Fig. 6(b). The circuits are implemented using a standard 180nm CMOS technology.

IV. Simulation Results

A. Modulator performance against clock jitter

A main advantage of using FIR DAC in CTΔΣM is the immunity against clock jitter. To verify this, a sample clock jitter of 5ns RMS (5% clock period) was included in the simulation. The transient noise method was used to include the effects of device noise in the simulation. The modulator performances were simulated and compared by including and excluding the memristive FIR DAC in the modulator. The results were also compared with the case where the modulator was designed using ideal components. The simulated SNDR and ENOB are summarized in Table I. The simulated modulator performance is very close to the case with ideal components, which proves the functionality and performance of the circuits designed. Note that the slight difference between rows 3/4 and 1/2 in Table I is because the simulations with ideal components do not include device noise.

Table I shows that the in-band noise is reduced when the memristive FIR DAC is included in the modulator, improving SNDR from 45.99dB to 63.69dB. This shows that the modulator with the FIR DAC is less sensitive to clock jitter and quantizer metastability. Moreover, the residue signal being processed by the loop filter is also reduced, thus relaxing the linearity requirement on the loop filter. Detailed output spectra are shown in Fig. 7. The spectra show that the modulator without FIR DAC has a higher in-band noise floor due to the existence of clock jitter. Additionally, the FIR DAC

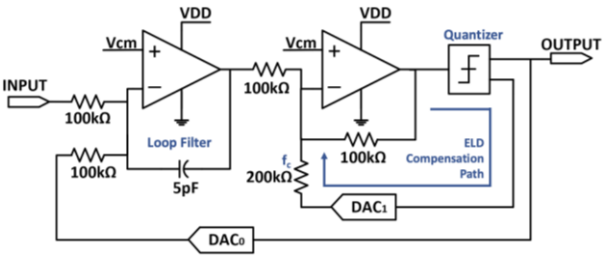


Fig. 5. First-order single-bit CTΔΣM with memristive FIR DAC

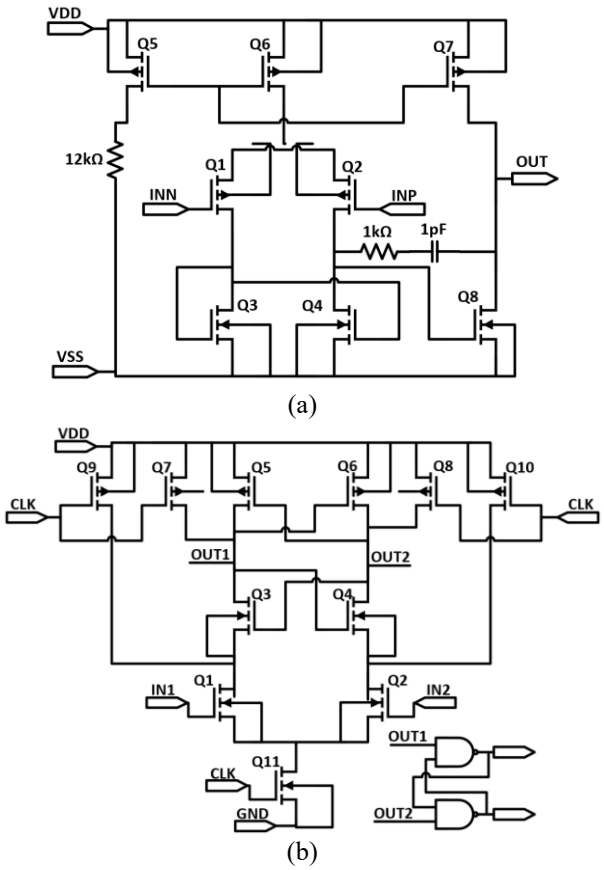


Fig. 6. Schematics of the OTA in the loop filters (a), and the quantizer (b).

also has slight attenuation effects on the idle tone spikes, which are common in low-order ΔΣ modulators [8].

B. Impacts of resistance variations in memristors

Since memristors have a limited resistance resolution, and the voltage signals across the memristors are dynamic, leading to resistance drift over time, the resistance of the memristors may vary around the calculated values. Simulations were conducted on the modulator where the resistance of the memristors in the FIR DAC were varied by ±20% to their nominal values. Comparing the 5th and 6th rows with 3rd and 4th rows of Table I, the variation in filter coefficients degrades output resolution indeed, which is due to variation of the FIR filter transfer function and the deviation of the circuit operating points, which needs to be addressed by further improvement on the circuit design in the future. Notably, the worst-case performance of the modulator, including the FIR DAC (49.56dB), is still better than that of the modulator without the FIR DAC (44.36dB). This verifies the advantage of using memristive FIR DAC in CTΔΣM designs.

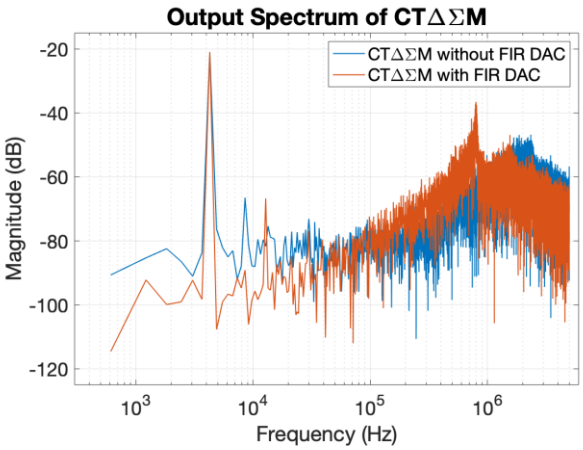


Fig. 7. Comparison between the output spectra of the first-order single-bit CTΔΣM with and without memristive FIR DAC. Spectra were obtained by applying a 16384-point fast Fourier transform (FFT) on the modulator outputs derived from a transient noise analysis. A sample clock jitter of 5ns RMS was included in the simulation.

V. Conclusions and Future Work

A first-order single-bit CTΔΣM with a memristive FIR DAC was designed and validated. An 8-tap FIR DAC was designed based on the available resistance range of a $Pt/Al_2O_3/TiO_2/Pt$ memristor. We then verified in simulations that the required resistance to implement the FIR coefficients could be achieved by programming the memristors with voltage pulses. We implemented the circuits for the loop filter, the quantizer, and the ELD compensation. The performance of the CTΔΣM shows that the memristive FIR DAC can significantly improve the modulator robustness against clock jitters, increasing the SNDR by ~18dB with the existence of 5ns RMS jitter in the sampling clock. Finally, the effects of memristor resistance variation in the memristive FIR DAC were investigated, which shows that the memristive FIR DAC can still improve the modulator performance with a worst-case 20% variation in the filter coefficients.

A primary limitation in this design is the resistance range of the memristors, which has restricted the freedom of the FIR filter design. Better FIR filters with higher stop-band attenuation can be designed if the memristor resistance range is wider. Notably, we are taking a conservative approach in this study and the the memristor resistance range is the worst case from the actual measurement data [4]. As an initial feasibility study, the objective of this work is to demonstrate how much performance improvement a memristive FIR DAC can bring to a CTΔΣM even with a limited memristor resistance range, and what circuits are required to support the memristor operation in this application. To achieve superior performance compared with the CTΔΣM state of the art, improvements to the memristor technology is needed. Although technology development is beyond the scope of this work, we would like to highlight the recent progress in memristor/RRAM technology which indicates 0~40μS conductance can be achieved with less than 1.75μS standard deviation using iterative write-verify programming methods [9]. In the future we can combine the technology advancement with the modulator-level and circuit-level improvements to achieve better modulator performance. Higher-order modulator topology can be adopted for higher resolution, and a larger number of FIR taps can be used. Dedicated circuits to program the memristors in the modulator will be designed, which involves additional control switches and pulse generators that are not yet included in the presented design. More power-efficient methods such as OTA-stacking [10] can be used to implement the loop filters and thus improve the modulator performance further. Upon the further improvements mentioned, a CTΔΣM with the memristive FIR DAC will be fabricated through standard CMOS foundry and the post-CMOS processing in house for memristor-CMOS integration so that eventually, a monolithic chip will be prototyped, characterized, and benchmarked against state of the art.

TABLE I. Simulation Results of CT ΔΣ M Including and Excluding Memristive FIR DAC

Simulations	Simulation Results	
	SNDR (dB)	***ENOB (bits)***
1.Ideal CTΔΣM excluding FIR DAC	45.99	7.346
2.Ideal CTΔΣM including FIR DAC	63.69	10.29
3.CTΔΣM excluding FIR DAC	44.36	7.075
4.CTΔΣM including FIR DAC	62.29	10.05
5.CTΔΣM with +20% variation in memristors' resistance in FIR DAC	53.79	8.641
6.CTΔΣM with -20% variation in memristors' resistance in FIR DAC	49.56	7.94

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