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Embedding hafnium oxide based FeFETs in the memory landscape

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***Abstract*— During the last decade ferroelectrics based on doped hafnium oxide emerged as promising candidates for realization of ultra-low-power non-volatile memories. Two spontaneous polarization states occurring in the material that can be altered by applying electrical fields rather than forcing a current through and the materials compatibility to CMOS processing are the main benefits setting the concept apart from other emerging memories. 1T1C ferroelectric random access memories (FeRAM) as well as 1T FeFET concepts are under investigation. In this article the application of hafnium based ferroelectric memories in different flavours and their ranking in the memory landscape are discussed.**

Keywords—ferroelectric hafnium oxide; FeFET; FeRAM;

I. INTRODUCTION

Charge-based semiconductor memory technologies such as SRAM, DRAM and FLASH face scaling challenges as geometries shrink towards 22nm and below. That is the driving force for an increased research activity focusing on alternative memory technologies during last few years. Charge trapping devices employing a 3D-integration ensure a continued cost per bit scaling of NAND FLASH. New high-k dielectric and electrode materials manufactured by adoption of ultra-fine dielectric deposition technology with a dielectric layer uniformity to a few Angstroms and quadruple patterning technology were able to push the DRAM roadmap beyond the 20nm frontier and might pave the way to even single-digit nodes. SRAM scales continuously at an approximate time-lag of two generations behind the smallest feature size to guarantee the crucial imperative of transistor matching. Besides that, the non-charge storage-based memories such as PCM, MRAM, ReRAM and FeRAM although in commercial production, suffer from high costs vis-à-vis current technologies and are still ranking in front of the step to overcome their limited adoption in niche applications thus far. Ferroelectricity in doped hafnia that was first reported in 2011 [1] opens the opportunity to overcome the integration and scaling limitations of conventional perovskite ferroelectrics due to low permittivity, high coercive field E_C and CMOS compatibility. Thus new boundary conditions in the race against the conventional charge based memories have to be considered and might catapult the ferroelectric memories towards leading position. Two flavours of ferroelectric memories are under consideration – the 1T1C FeRAM and the 1T FeFET concept. Ranking of both concepts in the memory hierarchy will be discussed in the following sections.

II. CHARACTERISTICS OF HAFNIUM OXIDE BASED FERROELECTRIC MEMORIES

A. 1T1C FeRAM implementation

In the 1T1C FeRAM the data is stored as polarization in a capacitor. During destructive readout upon application of a read voltage pulse at the plate line PL the polarization charge is transferred via a selector transistor to the bit line BL where similar to the DRAM concept a sense amplifier determines the stored logic state. The memory cell concept is depicted in Fig. 1. After readout the information has to be refreshed. Thus, for continuous operation of the device the trade-off between access time and cycling endurance has to be matched. For example, at a given endurance in the order of 10^{12} switching cycles at 10 year lifetime a 100us access time could be realized. Higher endurance might be attained by application of an anti-ferroelectric hafnium or zirconium oxide as was demonstrated in [2]. In order to gain sufficient signal to be sensed on the bit line the ferroelectric capacitor has to provide a polarization charge in the order of 15fC. Hence for a typical remanent

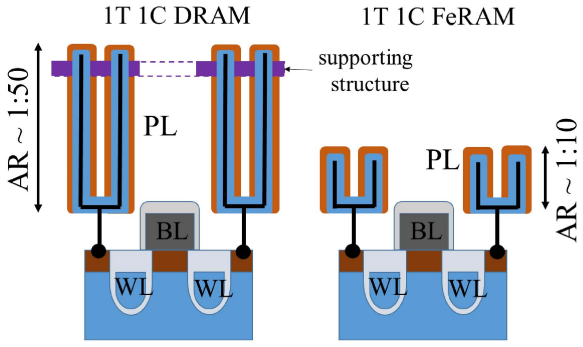

Fig. 1. Realization of 1T1C FeRAM compared to state of the art DRAM .

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polarization of 10-20 µC/cm² for doped HfO_2 a capacitor area of about 0.1µm² is required. Compared to high-density stand-alone DRAM, where the typical charge density of the capacitor is approximately 2 µC/cm² at a k-value of approximately 30 a reduction of the capacitor area by a factor 8 can be attained. For a given DRAM node the potential reduction in the cylinder capacitor area results in a decrease of the aspect ratio from about 50 down to approximately 12 during the capacitor trench etch. Moreover, the stabilizing support structures that were introduced since the sub-50nm DRAM nodes [3] can be omitted. Overall the alleviation of area requirements would lead to a reduction in manufacturing complexity and consequently in the cost per bit.

B. Planar 1T FeFET memory

The 1T FeFET memory concept relies on the change of threshold voltage due to polarization charge of the ferroelectric gate oxide material. Successful integration of the hafnium oxide based FeFET into planar state-of-the art high-k metal gate technology into 28nm and 22nm was demonstrated [4]. For typical coercive voltages of 1-2 MV/cm a switching voltage in the range of 4 V is mandatory where about half of the applied potential drops over the interfacial silicon oxide layer. Nevertheless, that programming voltage is at least a factor 4 less than typical programming voltages for FLASH devices, resulting in an increased array efficiency. Moreover, low programming voltages in conjunction with negligible programming currents and non-destructive readout makes the FeFET concept the most promising candidate for realization of ultra-low-power memories. The reported endurance of 10^4 for gate first process [4] up to 10^7 write cycles for gate last process [7] can easily compete with conventional planar NAND devices and makes the FeFET device very suitable as eNVM solution. However, in terms of cost per bit three detrimental aspects come into play that have to be solved to compete with planar stand-alone NAND. Firstly, from array disturb analysis the realization of AND or NOR array architecture seems to be beneficial [5, 6], implying a larger number of contacts and metallization lines in the array, thus increasing the cell size compared to NAND. Secondly, the poly-crystallinity of the ferroelectric material with grain sizes in the range of 10nm yields to a certain variability in the switching characteristic that can be omitted by increasing transistor size beyond 0.01 µm² [4]. Thus, based on the available ferroelectric films such cell size hinders scalability of the concept. Improvement could be attained by the application of textured or epitaxial grown ferroelectric films that are subject of current research [8]. Thirdly, multi-level storage was successfully demonstrated for FeFETs based on the polarization switching of individual ferroelectric domains in small devices [9]. However, in contrast to charge trapping memories, where the different levels are separated by up to 1V, in the FeFET case the maximum achievable memory window MW as calculated from a 1st order estimation by MW = Ec * tox ~ 2V would be divided down to just some 100mV by increasing the number of stored bits per cell. Hence, the realization of 2 or even 3 bits per cell seems not realistic and the resulting lower bit density would further degrade the competitiveness in terms of cost per bit compared to conventional planar NAND.

C. 3D integration for FeFET stand-alone memory

When considering to replace the charge trapping layer in state-of-the-art 3D NAND structures for realization of high density 3D FeFET memory two additional aspects have to be considered. Firstly, multi-level storage seems not realistic as was already discussed for the planar FeFET devices, even though the gate area for each cell is larger compared to the planar cell. That is, the bit density would be reduced by a factor of 2 to 3 compared to state-of-the-art 3D NAND devices. That drawback might be slightly counterbalanced by an increased array efficiency due to lower programming voltages for the FeFET that have to be generated on-chip.
Secondly, due to high coercive field of the hafnium oxide based ferroelectrics the cycling endurance of the FeFETs was shown to be limited to 10^4 to 10^7 cycles. The degradation effect is mainly attributed to the break-down of the silicon oxide interface between the ferroelectric and the transistor channel. From that data one can deduce that the silicon interface integrity is of utmost importance for high endurance. For the integration of the ferroelectric hafnium oxide in between the two polysilicon structures forming the NAND string channel and the gate planes as depicted in Fig. 3, the formation of a reliable silicon oxide interface seems to be the most challenging task. Correspondingly, degradation of the memory window already after 10^2 cycles was shown in [10].

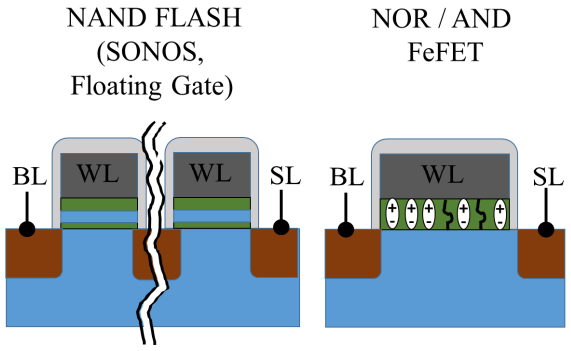

Fig. 2. Realization of 1T FeFET AND array compared to NAND FLASH.

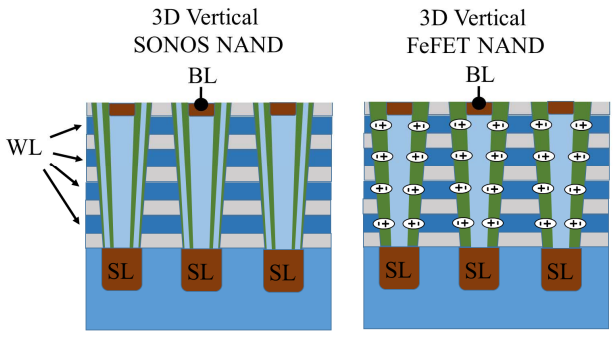

Fig. 3. Realization of 3D NAND FeFET compared to 3D NAND FLASH.

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Hence, for the realization of 3D FeFET memory further material development towards lower coercive voltages and improvement of the interfaces to silicon or the implementation of metallic gate planes are main tasks to be solved. Similar as stated previously for the planar NAND array architecture up to now the cell-to-cell disturb and program inhibit schemes for FeFET NAND operation have not been proven yet.

III. Ranking of Hafnium Oxide Based Ferroelectric Memories in the Memory Hierarchy

Table 1 summarizes typical values for several performance metrics of the three different implementations of hafnium oxide based ferroelectric memories and compares them to state-of-the-art NVM technologies. The 1T1C ferroelectric memory performs closest do DRAM specification. Due to higher charge density of the ferroelectric material compared to the conventional DRAM dielectric a reduction in capacitor size and hence a reduction in manufacturing complexity is attained. The improvement of cycling endurance and reliability of the ferroelectric capacitor would be the key enabler for the ferroelectric 1T1C concept being a real DRAM replacement.

In Fig. 4 the ranking of the different memory types is visualized in the memory pyramid. Following the proposal by Geoffrey W. Burr from 2010 [11] the storage class memory (SCM) with memory-like high performance but storage-like low cost and non-volatility fits in between conventional DRAM and FLASH. Two distinct levels can be distinguished. A storage type (S-SCM) closer to the bottom of the pyramid serves as a high-performance solid-state drive accessed by the system I/O controller. On the other hand, the memory type (M-SCM) features low read/write latency to remain synchronous with the memory system. In that arrangement the ferroelectric 1T1C concept clearly ranks on the memory type side among the storage class memories.

The 1T FeFET suffers from comparatively high area consumption per bit and is therefore not directly competitive

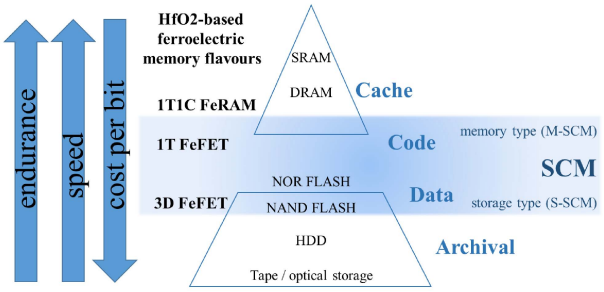

Fig. 4. Ranking of hafnium oxide based ferroelectric memories in the memory hierarchy

to stand alone planar NAND devices. However, for embedded memory application the area consumption of FLASH devices is larger since typically in that case no minimal geometries are realized. Furthermore, since the FLASH devices together with the high voltage devices that are mandatory to control the word lines in the array have to be treated as add-on devices to be implemented into standard CMOS process, the manufacturing complexity strongly increases for embedded FLASH. Thus together with the benefit of faster read and write times and potentially higher cycling endurance the FeFET is very likely to outperform the FLASH on the eNVM market. In comparison to competing eNVM solutions based on STT-MRAM or ReRAM, where cell size is mainly determined by current driving performance of the access transistor, the comparatively low manufacturing complexity together with an only slightly larger cell size at much lower power consumption makes the concept favourable. However, for SRAM-like applications the race between FeFET and STT-MRAM as eNVM will be decided mainly based on the endurance characteristics. Due to lower cycling endurance of the FeFET compared to the ferroelectric capacitor it is ranked presently as S-SCM closer to the bottom of the pyramid.

The 3D FeFET solution suffers from a lower bit density compared to the 3D NAND case due to the lag of multi-level

TABLE I. Memory Performance Metrics Comparison

Parameter	FLASH planar	PBICS 34 layer	FeFET 3D 34 layer	SRAM	FeFET planar	DRAM	FERRO 1T1C	ReRAM	STT-MRAM
write time	100 µs	100 µs	10 ns	1 ns	10 ns	10 ns	10 ns	10 ns	10 ns
read time	10 µs	10 µs	10 µs	1 ns	10 ns	10 ns	10 ns	10 ns	10 ns
write voltage	20 V	20 V	4 V	1 V	4 V	2.5 V	2 V	1.5 V	1 V
power consumption	medium	medium	low	medium	low	high	low	high	high
cycling endurance	3E+03	3E+03	1E+02	1E+15	1E+10	1E+15	1E+12	1E+05	1E+12
cell area [F²]	4	1	1	140	20	6	6	16	10
bits per cell capability	3	3	1	1	1	1	1	1	1
area / bit [F²]	1	0.3	1	140	20	6	6	16	10
rel. manufacturing complexity	1.2	1.6	1.6	1.0	1.0	1.4	1.3	1.1	1.2

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cell capability. Further, the cycling endurance is much lower at the current state and potential disturb issues are not solved yet. Therefore even though the write access times are much smaller the 3D FeFET would rank on the outer side of S-SCM even closer to the bottom of the pyramid.

IV. Summary

From the current perspective two realizations of hafnium oxide based ferroelectric memories are likely to enter the market in foreseeable future. For stand-alone devices a memory type storage class device based on the 1T1C concept, featuring close to DRAM-like performance in terms of speed and density but at reduced endurance is the most likely case.
Due to low cost implementation the 1T FeFET concept integrated into high-k metal gate technology is a very attractive candidate in terms of low-power and cost-per-bit. Additionally, reasonable cycling endurance and fast access times makes the concept very likely to find first niche applications that pave the way into eNVM market.

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