Design and Implementation of a Dependable CPSoC for Automotive Applications

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***Abstract*— Safety-critical cyber-physical systems-on-chip, consisting of analog/mixed-signal front- and back-ends combined with massive digital many-processor cores, are being increasingly applied. The imminent collision detection chip for cars is an example of this and such a complex system requires zero downtime and a very high dependability. By on-line monitoring the health status of processor cores and IPs and taking counteractions, we have accomplished this goal via IJTAG-compatible embedded instruments and appropriate embedded software. An IJTAG-compatible I_{DDT} monitor has been designed, a slack-delay embedded instrument for detecting timing issues, as well as a monitor for detecting intermitted resistive faults in interconnections. By the on-chip replacement of degraded (non-healthy) cores, the lifetime can be increased by a factor of around four of our mixed-signal cyber-physical systems-on-chip.**

Keywords*— *CPSoC, Industrial cyber-physical systems, Robust Automotive Systems, Dependability, System Awareness, IJTAG embedded instruments, I_{DDT} & slack-delay and IRF monitors

I. INTRODUCTION

Cyber-Physical Systems-on-Chip (CPSoC), including analog/mixed-signal front- & back-ends and many-processor cores increasingly find their way in applications in automotive safety-critical systems. Unfortunately, the overall dependability of these complex systems is decreasing [1]. Dependability is defined as the ability to deliver a service that can be justifiable trusted [2]. It integrates known attributes like reliability, availability and maintainability, among others. Hence, especially in safety-critical applications under harsh environmental conditions, on-chip on-line monitoring and fast counteractions during lifetime becomes a prerequisite to maintain a high dependability. The new contribution of this paper is the actual integration of new IJTAG-compatible embedded instruments into an industrial safety-critical CPSoC for lifetime enhancement; to our knowledge, no literature evidence is available on this subject except for our work. The design of single embedded instruments in general is not new, but until now only related to PVT control [3]. Isolated work on the potential usage of the IEEE IJTAG standard for controlling embedded instruments through the lifetime of systems has recently appeared [4]. An interesting example of a safety-critical application is the Imminent Collision Detection (ICD) system in cars.

The paper is organized in the following way. In section II, first the architecture of the ICD-CPSoC as well as its application requiring high dependability and zero down-time are briefly discussed. Next, the required sensors for this system are introduced and their dependability shortly explained based on our accelerated tests. The healths of its four-processor cores are evaluated by a number of IJTAG-compliant embedded instruments (EI). IJTAG is a recently approved standard (IEEE 1687) for embedded instrument communication in chips. In the case of degrading health, cores can be electronically isolated and replaced on-chip. Three new IJTAG-compliant embedded instruments are discussed in detail in sections III, IV, and V, being the dynamic power-current I_{DDT} monitor, the slack-delay and intermittent resistive fault (IRF) monitors. Design principles, chip layout and post-layout simulations as well as measurements are presented. The relation between the embedded instruments and lifetime prediction as well as the

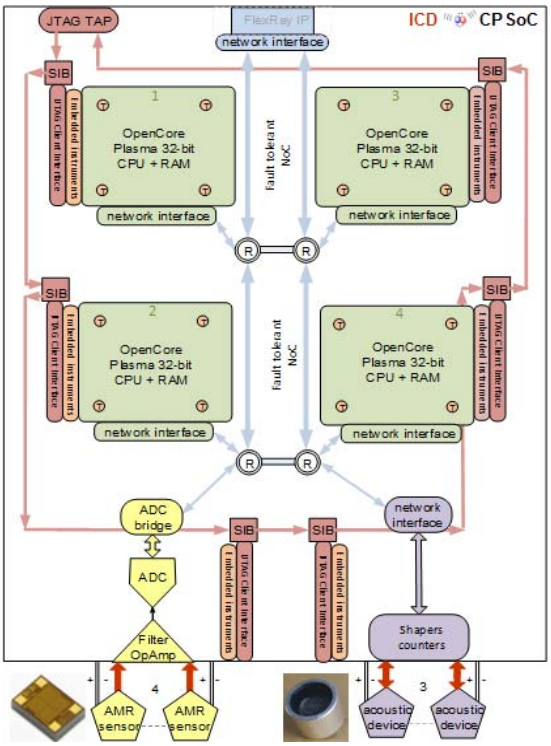

Fig. 1. The Imminent Collision Detector (ICD) CPSoC.

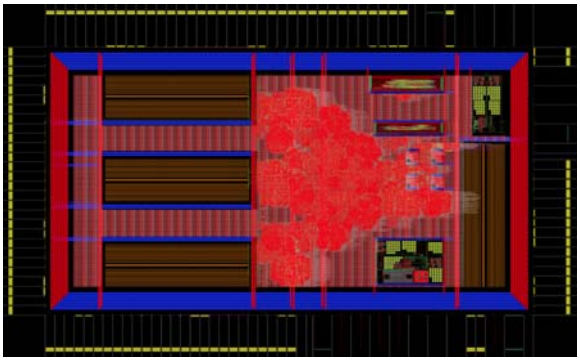

Fig. 2. The layout of the four-core CPSoC including RAMs, embedded instruments, IJTAG and fault-tolerant NoC network. Designed in 40nm TSMC CMOS technology. Silicon area: 1440µm x 840µm.

inherently dependability are briefly treated in section VI. The paper is completed in section VII with the conclusions.

II. The Imminent Collision Detection CPSoC

The basic set-up of the ICD CPSoC and its dependability is briefly explained first, and then the dependability of the analog front-ends is discussed.

A. The architecture of the ICD CPSoC

The goal of the ICD system in cars is to confirm that a collision is unavoidable and guarantees that preliminary actions take place, like seat belt tightening and pre-inflating the airbags, just before the actual collision takes place. In high-end cars from Mercedes-Benz, the PRE SAFE option based on expensive LIDAR (radar) monitors is available. In our case, a low-cost version employing anisotropic magneto resistive (AMR) sensors for detecting a disturbance of the magnetic field due to another car, in combination with ultrasonic distance measurements have been used for this purpose [5].

Based on the previous research we developed a CPSoC, using four Plasma processors, a fault-tolerant NoC, and front-ends capable of robust detection as shown in Fig. 1 [6]. The layout of the CPSoC in 40nm TSMC CMOS technology is depicted in Fig. 2. It is obvious that this system should be highly dependable with zero down time (availability). For embedded signal processing [6], like sensor fusion [7], two cores are required, leaving two cores for dependability (run-time mapping) back up. We accomplish the dependability requirements by monitoring the health of the four-processor cores by data fusion of a number of embedded instruments connected via an IJTAG network [8].

Three embedded instruments will be discussed in detail, the I_{DDT} monitor, the slack-delay and IRF monitors. Environmental embedded instruments for supply-voltage and temperature have been presented in [9]. In the case of the degrading health of a processor core or interconnections, an on-chip failure prediction is made and subsequent isolation and task reallocation to another processor core will take place *before* an actual failure occurs enabling zero mean time.

B. The dependability of AMR and ultrasonic sensors and their signal-conditioning electronics

The used sensors in the ICD are positioned into an array fashion as shown in Fig. 1. Four AMR sensors are being employed, and three ultrasonic devices, of which the one in the middle is configured as transmitter while the other five act as receivers (each unit has two devices). From our previous research [10], it has been proven that AMR devices age over time, in terms of their drift. However, a solution has been provided employing smart signal processing, to drastically reduce this issue. Recently, also our used ultrasonic devices have been undergoing accelerated stress tests [11], which revealed there was no significant degradation of their functional behavior. Finally, the mixed-signal and digital signal conditioning hardware following the sensors (OpAmp, filter, ADC, shapers and counters in Fig. 1) age in terms of offset and delay respectively, but previous research [9] has presented embedded instruments which can monitor (and compensate) that performance loss. Hence, we will focus in the remainder of this paper on the health monitoring of the four-processor cores.

We will now subsequently treat the three IJTAG-compatible embedded instruments in detail.

III. The I_{DDT} Embedded Instrument

The I_{DDT} or transient-power supply current has been found to have a strong relationship to NBTI degradation and hence aging of CPSoCs [12]. Fig. 3 shows the schematic of the raw and IJTAG-wrapped I_{DDT} embedded instrument. The raw instrument consists of circuit blocks such as current-to-voltage converter, sampling circuit, data converter, and monitor controller. The current-to-voltage converter is based on utilizing a current mirror to sense the transient current flowing through parasitic resistance of the power supply line [13]. The converted voltage signal from the current-to-voltage converter is sampled using a conventional sample and hold circuit. The sampled voltage is the input to an Analog-to-digital Converter (ADC) for digitization.

The control signals to the monitor and the digitized outputs are interfaced with the IJTAG network via the I_{DDT} EI Test-Data Register (TDR). The write-only TDR bits are the configuration bits of the monitor (3 left registers in Fig. 3). The configuration bits consist of bits to configure the monitor for calibration or measurement and to reset the monitor.

The read-only TDR consists of the 10-bit digital outputs of the monitor, data ready bit and overcurrent flag bit (right registers, Fig. 3). By interfacing with a 10-bit ADC, the design can achieve a resolution of 17µA which can sufficiently capture the transients of interest.

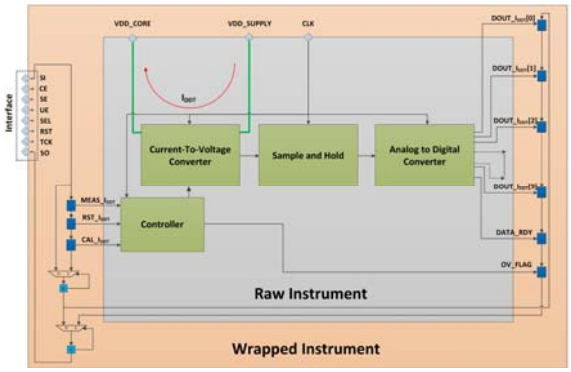

Fig.3. Raw and IJTAG-wrapped I_{DDT} embedded instrument

Due to the intermittent operation of the monitors, the aging of the monitor is significantly less compared to the CPSoC active cores that are in constant operation. Nevertheless, the design was also simulated using aging models [14] to guarantee that the monitor specifications are met over the lifetime. To mitigate the impact of process variations, a calibration mechanism has been introduced in the design. The calibration procedure could be carried out in the test phase as well as in the field throughout the lifetime to further ensure that the aging related drifts do not affect the monitor specifications.

A two-point calibration mechanism is required to mitigate the first-order process variations as well as drifts of the monitor. The additional hardware required for calibration is an accurate external current sink, which can sink two precise currents that are at the either end of the range of currents, which the I_{DDT} EI measures. The monitor has been designed to measure currents in the range of 0.5mA up to 9.5mA. If the monitor is in calibration mode, the current at the lower end of the measurement range is enabled for the measurement from the current sink. The digital output corresponding to this measurement is readout through the IJTAG network and stored in an embedded memory. Subsequently, the current at the higher end of the range is enabled from the current sink and the digital output is readout via the IJTAG network and also stored in memory. The calibration parameter is now calculated from these two measurements and also stored in memory.

In the measurement mode, in addition to the measured digital output, the calibration parameter and the digital output corresponding to the lower end of the range are readout from memory and used for the actual calibrated I_{DDT} computation. Fig. 4 depicts the layout of the I_{DDT} EI, which consists of the current-to-voltage converter, sample and hold circuit and the controller. The area of the monitor is 0.0171 mm^2, which also includes buffers for driving off-chip loads for test and characterization purposes.

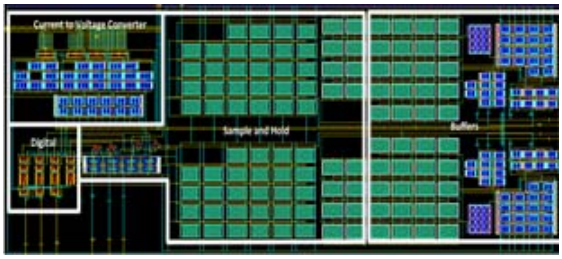

Fig. 4. Layout of the I_{DDT} monitor in 40nm TSMC CMOS technology.

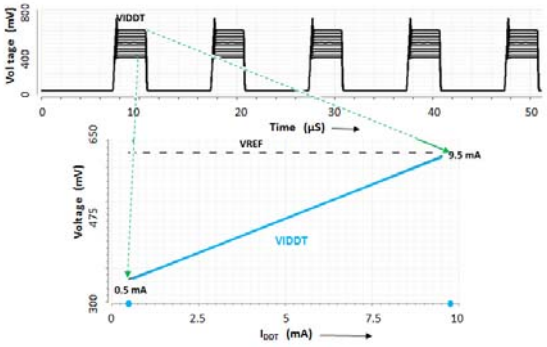

Fig.5. Post layout simulation results of I_{DDT} monitor

Fig. 5 shows the post-layout transient simulation results of the instrument (top graph). VIDDT represents the sampled voltage output from the current-to-voltage converter for a range of currents from 0.5mA to 9.5mA. The voltage VREF represents the reference voltage for digitization. As observed from the plot at the bottom, a linear response of VIDDT for the current range of interest has been accomplished.

IV. The Slack-Delay Embedded Instrument

Aging mechanisms like NBTI and PBTI are strongly dependent on the processor workload and the operating conditions, resulting in the timing degradation of the cores [15]. In the literature, a number of techniques have been proposed to monitor timing degradation by the means of using replica circuits [16] and slack-delay monitors [17].

Slack monitors are usually deployed at the end of the critical paths of the processor. These critical paths could be made of several logic paths which result in several logic transitions. Therefore it is necessary to have a slack delay monitor that can determine the timing degradation in the presence of multiple logic transitions.

Our proposed slack delay monitor can determine the remaining slack before the final transition (i.e. before the following clock edge) in the presence of multiple transitions, which is the main contribution of this newly proposed design.

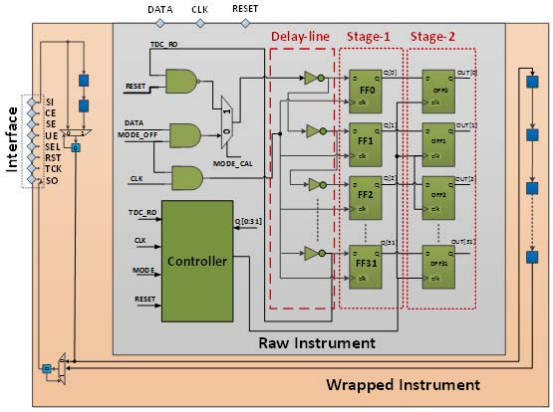

Fig. 6. Scheme of the wrapped slack-delay embedded instrument.

The scheme of the proposed IJTAG-compatible slack delay monitor is shown below in Fig. 6. The inputs from the processor core are highlighted on the top. DATA is the main input, taken from the end of the critical path (that is under monitoring) while CLK is the input clock-signal to the flip-flop that captures the data-transitions over the critical path; the RESET signal is the system reset. The main idea presented in this design is to observe the 416ps time before the clock-edge occurs and to sample the DATA signal. The slack delay EI can be configured into 3 different modes of operation of which the Monitoring-Mode is the most important one.

In the Monitoring-Mode, the monitor observes the DATA signal before the following positive edge of CLK and once the transition occurs, it captures the DATA signal and sends it via the IJTAG interface to the higher hierarchical level, where this reading can be interpreted and the remaining slack can be measured. In the Monitoring-Mode, the controller module sets a window of 256 clock-cycles (as a reference time) to capture the first transition over the DATA signal. This value is a design trade-off between the probability of occurrence of a transition and the waiting time for detection at the system level of a transition. Afterwards the MUX will select DATA as an input to the 'Delay-line' (highlighted in red, Fig. 6). The main purpose of the block 'Delay-line' is to setup the observation window of 416ps before the clock edge. To sample the DATA signal contents over 'Delay-line', a set of flip-flops 'Stage-1' is used to capture the signal DATA at every positive-edge of CLK. The 32-bit output Q[31:0] of 'Stage-1' goes to the controller module, that determines if there is any transition happening. In the case of a transition, the controller module generates a capturing signal to the second set of flip-flops 'Stage-2' that captures the contents of 'Stage-1'. In the case of no transition, the controller module will generate a capturing signal at the end of the 256 clock-cycle window. For the remaining slack calculation, the 32-bit output OUT[31:0] of 'Stage-2' is then transferred to the system level via the IJTAG interface.

Fig. 7 shows the post-layout simulation results of the monitor for five different cases. In the most important Case-

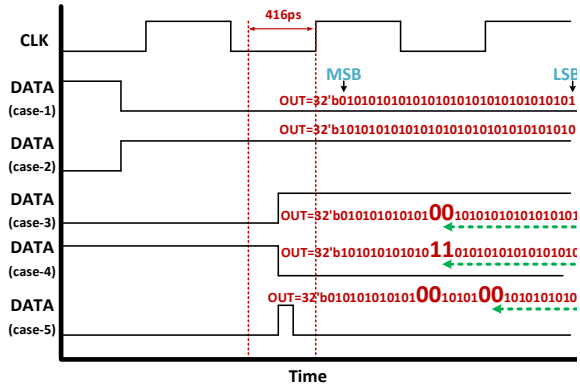

Fig. 7. The post-layout simulation results of the proposed slack-delay embedded instrument.

5, there are two transitions on the signal 'DATA', as initially it changes its logical value from '0' to '1' and then the logical value changes from '1' to '0' in the (dashed) observation window. The output shows two ripples (bold and capital) indicating two transitions. To determine the remaining time slack, we determine the number of bits before the ripple occurs (the green line) and multiply this number with the propagation delay of each invertor calculated in the Calibration-Mode. The maximum resolution of the current design is 15ps. The layout of the slack-delay embedded instrument is shown in Fig. 11 at the bottom of the figure, and its area is 5400µm^2 in 40nm TSMC technology, mainly due to the on-board controller.

V. The Intermittent Resistive Fault Embedded Instrument

Interconnection reliability is a very important factor of the total reliability of CPSoCs. One of the most challenging faults, no faults found (NFF), that threats interconnection dependability are intermittent resistive faults (IRFs) [18, 19]. They are appearing as random low-level (burst)

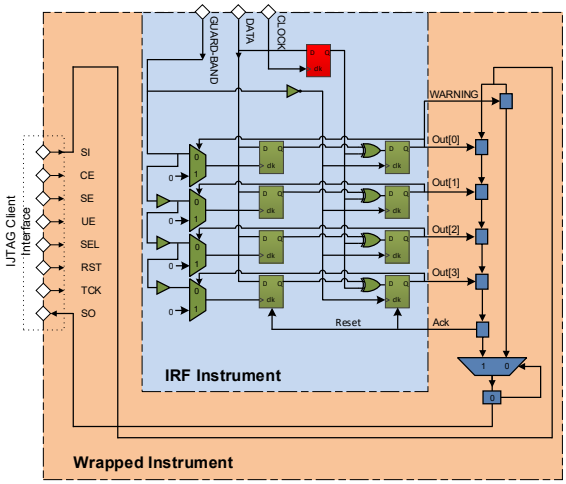

Fig. 8. The IJTAG-compatible IRF embedded instrument for detecting intermittent faults.

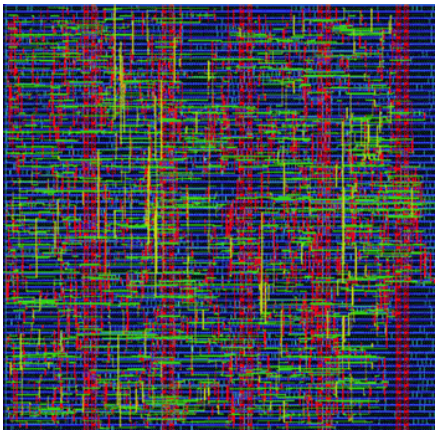

Fig. 9. Layout of the IJTAG-compatible IRF embedded

occurrences in time, being randomly fixed in locations; usually they cause in turn timing violations, and often after aging a system failure. The major causes of IRFs are loose and marginal connections, such as leaky vias and Trough Silicon Vias (TSV) [18]. In CPSoCs, there are various types of interconnections both at chip and board (sensor) level [19]. All these interconnections are susceptible to IRFs and it is very important to detect these beginning anomalies before they evolve in a system failure later on especially in safety-critical systems with zero downtime.

Because IRFs in an interconnection occur randomly in time during the operational time of a system, IRF detection is only possible by on-line in-situ monitoring [20]. In order to detect IRFs, we have introduced an on-line in-situ digital instrument, which is able to detect IRFs in a system's data paths. Fig. 8 shows the IRF instrument wrapped by the usage of the IJTAG standard. In this figure, the IRF instrument's gates are highlighted in the green color, and the IJTAG scan-chain is shown in dark blue. The flip-flop in red is not part of the instrument. It resembles the flip-flop at the end of a data path. The IRF instrument has several D-flip-flops, comparators, and a delay chain. The IRF instrument monitors the data at the end of a transmission line (data path). It captures all the late transitions (timing violation) on the DATA signal during a timing window provided by the GUARD-BAND signal. In case of a timing violation detection on the DATA, the WARNING signal will be raised and the degree of violation will be captured by the instrument's flip-flops. The captured information is transferred to the IJTAG chain. The layout of the IRF EI in 40nm TSMC CMOS standard-cell technology is depicted in Fig. 9.

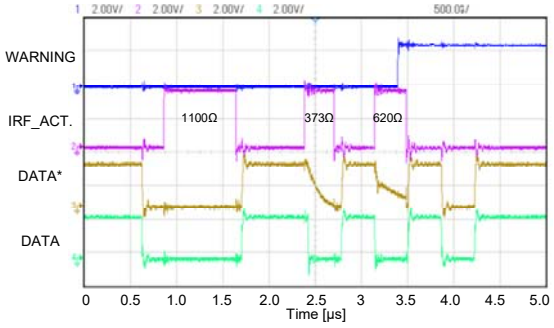

Fig. 10. Measurement results of the IJTAG-compatible IRF embedded instrument.

To characterize our IRF instrument, we have implemented an IRF generator [21] to inject IRFs in a real transmission line. In addition, we have designed and implemented a fault management framework using an IJTAG network to collect information from the implemented IRF instrument. As JTAG controller, we have employed JTAG Live [22] in combination with Matlab software. To transfer data between sensors and control units in SoCs, serial protocols can be used. Fig. 10 shows an example of the measurement results for IRF injection in a transmission line with a serial protocol. In this figure, the IRF_ACT signal indicates the injected IRF by the IRF generator in the DATA transmission line. It consists of three pulses with various values and durations. The DATA* signal shows the DATA signal after distortion by the injected IRF. The WARNING signal has become one if the IRF instrument has detected a timing violation. In this measurement example, the last pulse of the injected IRF with resistance value of 620 Ω has caused the maximum delay violation and has been detected by the IRF instrument. From our measurements of 10.000 fault injections on random data transmissions, we can conclude that in the case of serial protocol transmissions the IRF instrument can detect IRFs with resistance values larger than 470 Ω.

Besides the previously discussed embedded instruments, also voltage and temperature EIs have been designed and implemented. Fig. 11 shows the layout of the complete stand-alone collection of our EIs for characterization purposes (40 nm TSMC CMOS); the I_{DDT} monitor is at the left, the temperature monitors are at the right, the voltage EI is at the top and the slack-delay EI at the bottom. In the center are the IRF EI and the complete IJTAG network. The embedded instruments are also separately included near the target cores in Fig. 2.

VI. EI FUSION, LIFE-TIME PREDICTION AND ENHANCED DEPENDABILITY

The data of the previously discussed EIs have to be fused first into a single virtual EI. The EI data is weighed on the basis of correlation change of the real-time data [7]. The new data of this virtual EI is subsequently applied to our embedded lifetime prediction algorithm software [23]. If the data sheet lifetime is jeopardized, the non-healthy processor core is electronically isolated and replaced by another healthy core and on-chip runtime mapping of tasks is performed. As two cores are minimally required for the ICD CPSoC, two spare cores remain, boosting the lifetime and hence dependability with a factor of four [24].

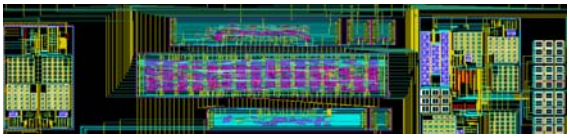

Fig. 11. Layout of all IJTAG EIs for characterization: slack-delay (bottom), I_{DDT} (left), temperature (right), voltage (top) embedded instruments; IRF EI and IJTAG network in the middle.

VII. Conclusions

In safety-critical automotive systems, designers increasingly use many-processor cores CPSoCs, combining analogue front-ends with massive digital processing. As an example, a highly dependable four-processor CPSoC for Imminent Collision Detection in cars, with no downtime, has been used as example. This paper deals with several embedded instruments interconnected by an innovative IJTAG infrastructure. Three IJTAG-compatible EI designs have been presented, an I_{DDT} monitor for reliability assessment, a slack-delay embedded instrument capable of coping with aging monitoring, and a detector if intermittent resistive faults occur in the interconnections. The EI designs and IJTAG infrastructure have been verified by post-layout simulation and some by actual measurements. In combination with on-chip counteractions, the lifetime can be increased with a factor of around four in our case. The EIs and the CPSoC designs and layouts were completed and verified and the mixed-signal 40nm CMOS implementation is currently being fabricated by TSMC.

Acknowledgments

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References

[1] P. Axer, M. Sebastian and R. Ernst, “Reliability analysis for MP-SoCs with mixed-critical, hard real-time constraints,” in Conference on Hardware/Software Codesign and System Synthesis, pp. 149-158, 2011.

[2] A. Avizienis, J.-C. Laprie and B. Randell, “Fundamental concepts of dependability,” Laboratory for Analysis and Architecture Systems (LAAS-CNRS), Report 01-145, April 2001.

[3] “The implementation of embedded PVT monitoring subsystems in todays cutting edge technologies,” white paper Moortec Semiconductor Ltd., 2017.

[4] E. Larsson and F.G. Zadegan, “Accesing on-chip instruments through life-time of systems,” in Proc. Latin-American Test Symposium (LATS), Foz do Iguacu Brasil, 2016.

[5] S. Taghvaeeyan and R. Rajamani, “Two-dimensional sensor system for automotive crash prediction,” in IEEE Trans. on intelligent transportation, vol. 15, no. 1, pp. 178-190, 2014.

[6] H.G. Kerkhoff, G. Ali, H. Ebrahimi and A. Ibrahim, “An automotive MP-SoC featuring an advanced embedded instrument infrastructure for high dependability,” in Proc. ITC-Asia, Taipei Taiwan, pp. 1-6, September 2017.

[7] M. Zabair, K. Hartmann and O. Loffeld, “A correlation based sensor fusion method for mult-channel seismic network,” Int. Jrnl. of Computer and Electrical Engineering, Vol. 4, No. 3, pp. 363-366, June 2012.

[8] A.M.Y. Ibrahim, “Structured and cost efficient dependability management for SoCs through test standards reuse,” Ph.D. thesis University of Twente, 267 pages, January 2018.

[9] H.G. Kerkhoff, G. Ali, J. Wan, A. Ibrahim and J. Pathrose, “Applying IJTAG-compatible embedded instruments for life-time enhancement of analog front-ends of cyber-physical systems,” in proc. VLSI-SoC conference, Abu Dhabi UAE, pp. 1-6, October 2017.

[10] A. Zambrano, “A dependable automotive anisotropic magnetoresistance sensor for automotive applications,” Ph.D. thesis University of Twente, April 2018.

[11] R. Jonkman, “Implementation of a reliable 2D approximator using sonar,” B.Sc. thesis University of Twente, July 2017.

[12] Y. Zhao and H. G. Kerkhoff, “Unit-based functional iddt testing for aging degradation monitoring in a vliw processor,” in proc. Euromicro Conference on Digital System Design, pp. 353–358, August 2015.

[13] V. Stopjakova, H. Manhaeve, and M. Sidiropulos, “On-chip transient current monitor for testing of low-voltage cmos ic,” in proc. of the Conference on Design, Automation and Test in Europe, (DATE), New York, USA: ACM, pp. 538-542, 1999.

[Online]. Available:http://doi.acm.org/10.1145/307418.307560.

[14] J. Wan, H.G. Kerkhoff and J. Bisschop, “Simulating nbti degradation in arbitrary stressed analogue/mixed-signal environments,” in IEEE Trans. on Nanotechnology, vol. 15, No. 2, pp. 137-148, March 2016.

[15] N. Pour Aryan, "Monitoring concepts for degradation effects in digital CMOS circuits," Dissertation Technische Universität München, München Germany, 2015.

[16] J. Tschanz, K. Bowman, S. Walstra, M. Agostinelli, T. Karnik, and V. De, "Tunable replica circuits and adaptive voltage-frequency techniques for dynamic voltage, temperature, and aging variation tolerance," in proc. VLSI Circuits Symposium, pp. 112-113, 2009.

[17] W. Shan, L. Shi, and J. Yang, "In-situ timing monitor based adaptive voltage scaling system for wide-voltage-range applications," in IEEE Access, vol. PP, pp. 1-8, 2017.

[18] S. Davidson, “Towards an understanding of no trouble found devices,” in IEEE VLSI Test Symposium (VTS), pp. 147–152, 2005.

[19] H. G. Kerkhoff and H. Ebrahimi, “Detection of intermittent resistive faults in electronic systems based on the mixed-signal boundary-scan standard,” in proc. IEEE Asia Symposium on Quality Electronic Design (ASQED), KUL Malaysia, pp. 77–82, 2015.

[20] H. Ebrahimi, A. Rohani, and H. G. Kerkhoff, “Detecting intermittent resistive faults in digital CMOS circuits,” in proc. IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), pp. 87–90, 2016.

[21] H. Ebrahimi and H. G. Kerkhoff, “Testing for intermittent resistive faults in CMOS integrated systems,” in proc. IEEE Euromicro Conference on Digital System Design (DSD), pp. 703–707, 2016.

[22] “JTAG Live Studio, available: http://www.jtaglive.com/.”

[23] Y. Zhao and H.G. Kerkhoff, “Highly dependable multi-processor SoCs employing lifetime prediction based on health monitors,” in proc. Asian Test Symposium (ATS), Hiroshima Japan, pp. 228-233, 2016.

[24] X. Zhang, “Towards a dependable homogeneous many-processor SoC,” Ph.D. thesis University of Twente, 213 pages, 2014.