Power Loss Analysis of a Multiport DC – DC Converter for DC Grid Applications

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***Abstract*— In this paper, power losses of a multiport DC – DC converter are analysed. The converter has four bidirectional ports and consists of a triple active bridge and four half bridge converters. As a result, sixteen different operating modes, defined by all combinations of power flow direction, are possible. The converter power losses and resulting efficiencies vary widely with operating conditions. This paper presents methods to accurately calculate the efficiency of the four-port converter in each operating mode using component datasheet information, taking into account losses in the transformer of the triple active bridge converter, passive components and semiconductors. A 200 W converter prototype is used to experimentally validate the loss model for one specific operating mode.**

Keywords*— *Multiport DC-DC Converter, DC grid, Converter Power Loss, Operating Mode, Converter Efficiency

I. INTRODUCTION

In recent years, DC grids using multiport DC-DC converters have attracted the attention of researchers because they offer a low cost, low component count, feasible and sustainable model of distributed generation amidst the increasing energy demand, penetration of renewable energy sources, and concerns of global warming [1]. Fig. 1 shows a multiport DC-DC converter-based DC grid with integration of solar PV, energy storage system (ESS), DC load and utility grid. In all cases, it is desired to operate DC grids at maximum efficiency. Power electronics converters, which provide the interface between sources and loads [2], introduce losses into the grid and can have relatively low efficiency, especially at light loads [3]. Therefore, accurate predictions of their power losses under any operating mode are useful since they can help optimize the operation of the grid.

In power electronics converters, steady state voltage and current waveforms can be mathematically modelled to obtain the duration of current flow in each converter device and consequently to calculate the power losses at any time point in a switching cycle. However, this process is not straightforward in multiport DC-DC converters due to the multiple operating modes, defined by all combinations of power flow direction, and design choices [4]. In [5], the efficiency of a Triple Active Bridge (TAB) converter was found to be dependent on transformer's turns ratio and leakage inductances. Proper selection of these parameters is

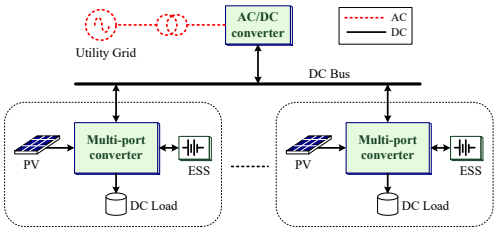

Fig. 1. Multiport DC-DC converter-based DC grid with integration of solar (PV), energy storage system (ESS), DC loads and utility grid

key in the design of a highly efficient converter. Reference [4] reports that most of the TAB converter losses are because of iron and copper losses in the transformer's leakage inductances and windings respectively. The losses were found to be largely dependent on the phase shifts of the applied voltages to the transformer. The paper further proposes a design approach that limits the phase shifts of the TAB converter to lower the losses. Other methods such as rectangular, trapezoidal, and triangular modulation schemes aimed at suppressing the losses of the TAB converter have been proposed in [6].

In previous papers, the power losses of the TAB converter are analyzed from the design point of view so that an efficient converter design could be obtained. However, in DC grid applications, it is useful to analyse the losses of an existing converter design from the operation point of view so that higher-level control schemes can be designed to take losses into account. This way, the operation of the grid could be optimized (i.e. operated with maximum efficiency).

This paper analyses the power loses of a four port DC-DC converter topology (which consists of the TAB converter and four half bridge converters) from the operation point of view. The analysis establishes the most efficient operating mode of the converter.

The rest of the paper is organized as follows: section II describes the four port DC-DC converter topology and its voltage and current characteristics for any operating mode. In section III, expressions used to calculate the power losses are obtained. Section IV discusses the results and conclusions are drawn in section V.

II. FOUR PORT DC-DC CONVERTER TOPOLOGY

Fig. 2 shows the four-port DC-DC converter used in this paper. The converter consists of a TAB converter and four half-bridge (HB) converters; HB-A, HB-B, HB-C and HB-

D. The four half-bridge converters are operated in constant voltage mode using duty cycle control [7] whereas the TAB converter is operated using phase shift control [8]. All the four ports are bidirectional and the powers; P_A, P_B, P_C and P_C can be either positive or negative depending on the operating mode. The voltage and current waveforms of each part of the converter (i.e. the half bridge and TAB converter) for any specific operating mode are modelled separately in the following subsections. This allows the calculation of component power losses over a single switching cycle.

A. Triple Active Bridge Converter Modelling

Fig. 3 shows an equivalent circuit of the TAB converter and the concept of phase shift control for current flow. It consists of three DC/AC full-bridge converters connected to a network of linkage inductors, L_{12}, L_{13}, L_{23} using a three-winding transformer with turns ratio, $1{:}N_2{:}N_3$. Each DC/AC converter produces a square voltage waveform across the transformer terminals with a fixed 50% duty cycle and a magnitude equal to the respective DC link capacitor voltage (i.e. V_1, V_2, V_3). The power flow between the converters is achieved by controlling the phase shift angle of each waveform with respect to the reference waveform at the primary. The power exchange between two converters (k and j) depends on the relative phase shift angle, ($\phi_{kj} = \phi_j - \phi_k$) between them. As the result, an alternating square voltage waveform with magnitudes V'_k, and V'_j (referred to the primary) is established across the linkage inductance L_{kj} as shown in Fig. 3. This results to a symmetrical piece-wise linear current i_{kj} (1):

$$i_{kj}(t) = \begin{cases} I_{kj(0)} + \dfrac{V'_k + V'_j}{L_{kj}} t & 0 < t < t_{sw} \\ I_{kj(p)} + \dfrac{V'_k - V'_j}{L_{kj}} (t - t_{sw}) & t_{sw} < t < \dfrac{T_s}{2} \end{cases} \quad (1)$$

where j,k = 1,2,3, $I_{kj(0)}$ and $I_{kj(p)}$ are instantaneous currents (given by (2) and (3) respectively) when the voltages V'_k, and V'_j change polarity from negative to positive as shown on the waveform in Fig. 3 for a switching period, T_s and t_{sw} is the switch-on time given by (4).

$$I_{kj(0)} = \frac{-T_s}{4L_{kj}} \left(2V'_j d_{kj} + V'_k - V'_j\right) \quad (2)$$

$$I_{kj(p)} = \frac{T_s}{4L_{kj}} \left(2V'_k d_{kj} + V'_j - V'_k\right) \quad (3)$$

$$t_{sw} = \frac{\phi_{kj} T_s}{2\pi} \text{ ; and } d_{kj} = \phi_{kj}/\pi \quad (4)$$

The linkage inductance L_{kj} can be calculated by (5):

$$L_{kj} = \frac{L'_k L'_{i,i\neq k\neq j} + \sum_{k=1,k\neq j}^{3} L'_k L'_j}{L'_{i,i\neq k\neq j}} \quad (5)$$

where L'_i, L'_j, L'_k (i,j,k = 1,2,3) are the transformer leakage inductances referred to the primary side. The total piecewise linear current $i_k(t)$ that flows into each winding with N_k turns and the associated DC/AC converter is obtained by (6):

$$i_k(t) = \frac{N_1}{N_k} \sum_{k\neq j}^{3} i_{kj}(t) \quad j,k = 1,2,3 \quad (6)$$

Equations (1)-(6) suggest that for a given operating mode, current flow results from adjusting the relative phase shift angle ϕ_{kj}. With the three DC/AC converters, this implies that the converter can operate under six operating modes as shown in Fig. 4. To calculate the power losses for any operating mode, all the six modes have been examined and the corresponding steady state voltage and current waveforms are shown in Fig. 5. Consequently, the duration of current flow and power loss in each DC/AC converter MOSFET and transformer winding can now be determined at any time point in a switching cycle.

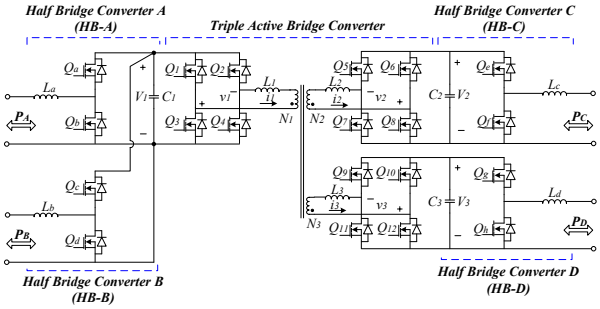

Fig. 2. Schematic of a four port DC-DC converter topology

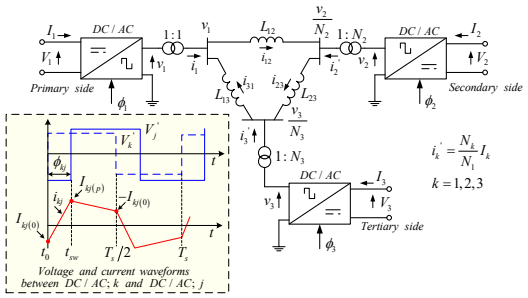

Fig. 3. Equivalent circuit of a TAB converter and the concept of phase shift control for current flow.

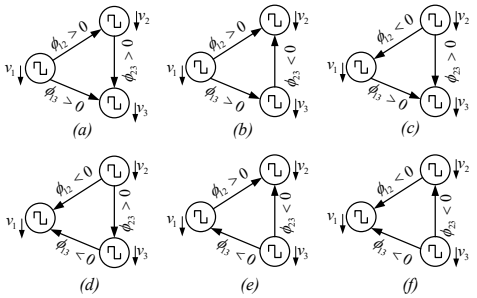

Fig. 4. Six possible operating modes of the three DC/AC converters of the TAB converter: (a) mode 1 (b) mode 2 (c) mode 3 (d) mode 4 (e) mode 5 and (f) mode 6

B. Half-Bridge DC/DC Converter Modelling

Fig. 6 shows a half bridge converter which operates in either buck or boost mode depending on the operating mode. The voltage and current waveforms at steady state are shown in Fig. 7. The piece-wise linear current through the filter inductor L_γ (where $\gamma = a,b,c,d$ in Fig. 2) is given by:

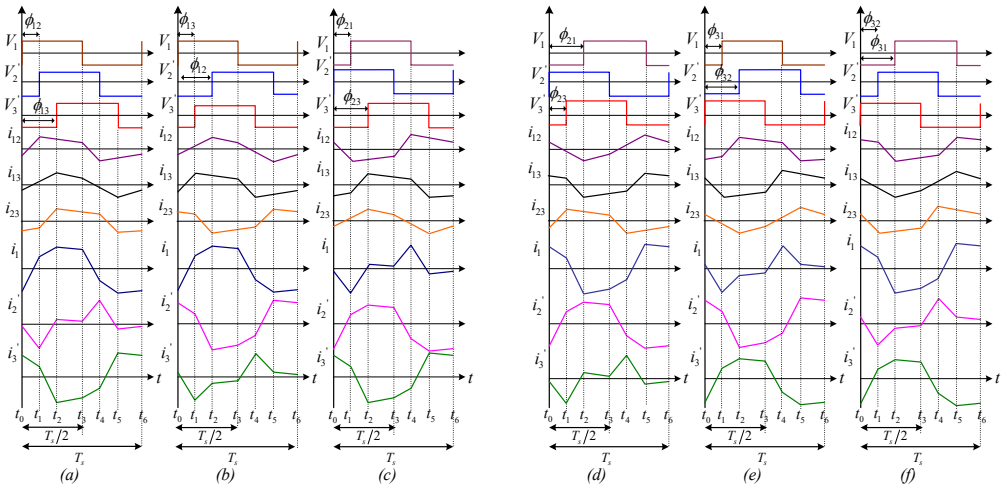

Fig. 5. Idealized (six) voltage and current waveforms of a TAB converter with MOSFETs operating in synchronous rectification: (a) mode 1 (b) mode 2 (c) mode 3 (d) mode 4 (e) mode 5 and (f) mode 6

$$i_L(t)=\begin{cases} i_{L(0)}+\dfrac{\Delta i_L}{DT_s}t & 0\le t\le DT_s \\ i_{L(0)}+\Delta i_L\left(\dfrac{T_s-t}{(1-D)T_s}\right) & DT_s\le t\le T_s \end{cases} \tag{7}$$

where the initial inductor current $i_{L(0)}$ is given by

$$i_{L(0)}=\begin{cases} I_0-\dfrac{\Delta i_L}{2} & (buck) \\ I_{in}-\dfrac{\Delta i_L}{2} & (boost) \end{cases} \tag{8}$$

and duty cycle, $D = V_T/V_h$ in buck and $D = (V_h - V_T)/V_h$ in boost mode. The ripple current Δi_L and currents through the MOSFETs Q_x, and Q_y ($x = a,c,e,g$ and $y = b,d,f,h$ in Fig. 2) are given by (9)-(11) in Table I for both buck and boost modes. The voltages, V_T and V_h are presented in Fig. 6.

TABLE I
Summary of Instantaneous Currents
of the Half Bridge in Fig. 6 and Fig. 7.

Current	Buck $[0 < t \le DT_s]$	Boost $[DT_s < t \le T_s]$	
Δi_L	$\dfrac{V_h-V_T}{L_\gamma}DT_s$	$\dfrac{V_h}{L_\gamma}DT_s$	(9)
$i_{Qx}(t)$	$I_0+\dfrac{\Delta i_L}{2}(2t-DT_s)$	$I_{in}+\dfrac{\Delta i_L}{2}\dfrac{T_s-(2t-DT_s)}{(1-D)}$	(10)
$i_{Qy}(t)$	$I_0+\dfrac{\Delta i_L}{2}D\dfrac{T_s-(2t-DT_s)}{(1-D)}$	$I_{in}+\dfrac{\Delta i_L}{2}(2t-DT_s)$	(11)

The capacitor current, i_{Ch} is given by (12):

$$i_{C_h}(t)=\begin{cases} \dfrac{V_L}{2L_\gamma}(2t-DT_s) & 0\le t\le DT_s \\ \dfrac{V_L}{2L_\gamma}D\dfrac{T_s-(2t-DT_s)}{(1-D)} & DT_s\le t\le T_s \end{cases} \tag{12}$$

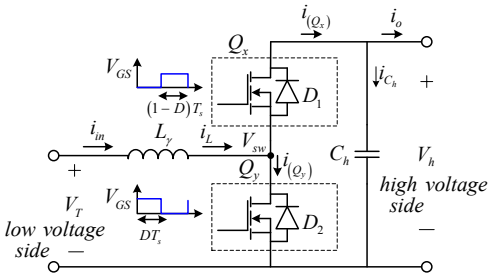

Fig. 6. Schematic diagram of a half bridge DC-DC converter.

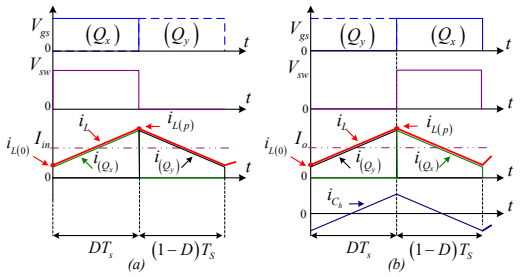

Fig. 7. Voltage and current waveforms of the half bridge converter when it operates in (a) buck and (b) boost mode.

III. Loss Calculation

This section describes the power loss expressions used to calculate the losses of the converter in Fig. 2. The Power losses have been divided into semiconductor device losses, passive component losses and transformer losses. Because of synchronous rectification by the MOSFETs, the power loss contribution by the body diodes are ignored [9].

A. Power Losses in Semiconductor Devices

Power losses in semiconductor devices are divided into conduction and switching losses.

1. Conduction Losses

For each MOSFET, the conduction losses are evaluated for the interval in which it is conducting [5].The conduction interval [t_x, t_y] (where t_x, is the start time and t_y is the end time of conduction) is obtained from the steady state voltage and current waveforms presented in Fig. 5 and Fig. 7. Therefore, the conduction losses are estimated by:

$$P_{sw(C)} = \frac{1}{n_{sw,p}} \left(\sqrt{\frac{1}{T_s} \int_{t_x}^{t_y} i_x^{\,2}(t)\, dt} \right)^2 R_{DS(on)} \qquad (13)$$

where $n_{sw,p}$ is the number of MOSFETs in parallel [10], $R_{DS(on)}$ is the MOSFET on resistance and $i_x(t)$ is the piece wise linear current given by (10)-(11) for the MOSFETs in the half-bridge and by (6) for the MOSFETs in the DC/AC converters.

2. Switching Losses

Switching losses of the converter are a result of the power lost to turn on and turn off the MOSFET switches. Each MOSFET turns on while its body diode is initially conducting. Therefore, the voltage drop across the MOSFET is given by the voltage drop of the conducting forward-biased body diode which in most cases is negligible. Thus, turn on losses are negligible and can be ignored. Power losses during turn off are the majority because each MOSFET turns off at a non-negligible voltage condition and they are given by [11]:

$$P_{sw(off)} = \frac{1}{2} \left| i_x(t) \right| V_{sw} t_{off} f_s \qquad (14)$$

Where $i_x(t)$ is given by (6), (10) and (11), V_{sw} is the voltage drop across the MOSFET, f_s is the switching frequency of the converter and t_{off} is the turn off time of the MOSFET.
The power lost to charge/discharge the input gate capacitance of the MOSFET when turning on/off is estimated by [11]:

$$P_{sw(GD)} = n_{sw,p}\, Q_G V_{gs} f_s \qquad (15)$$

where Q_G is total gate charge and V_{gs} is the gate-source voltage.

B. Power Losses in the Passive Components

Passive components such as capacitors and inductors also introduce losses into the system due to their equivalent series resistance (ESR). These losses are given by:

$$P_{pass(C)} = \left(\sqrt{\frac{1}{T_s} \int_{t_x}^{t_y} i_p^{\,2}(t)\, dt} \right)^2 R_{ESR} \qquad (16)$$

where R_{ESR} is the ESR of either the DC link capacitor C_h or filter inductor L_γ, and i_p is the current flowing through each passive component, given by (7) and (12) respectively.

C. Power Losses in the Transformer

Power losses in the transformer are equal to the sum of copper losses in the windings and magnetic core losses. The copper losses (17) depend on the current, i_x (6) flowing in each winding.

$$P_{Trx(cu)} = \left(\sqrt{\frac{1}{T_s} \int_{t_x}^{t_y} i_x^{\,2}(t)\, dt} \right)^2 R_k \qquad (17)$$

where R_k is the DC resistance of the printed circuited winding and is given by [12]:

$$R_k = \chi N_k R_{(trace)} \qquad (18)$$

and χ is the mean length turn, $R_{(trace)}$ is the DC resistance of the copper trace and N_k is the number of turns of the winding. The transformer magnetic core losses consist of the hysteresis and eddy current losses [13]. The total magnetic core losses under square wave voltage with duty cycle, D can be approximated by the Natural Steinmetz Extension [14]:

$$P_{Trx(core)} = k_N f_s^{\,\alpha} \hat{B}^{\beta} \left[\left(\frac{2}{D} \right)^{\alpha} + \left(\frac{2}{1-D} \right)^{\alpha} (1-D) \right] V_{core} \qquad (19)$$

where k_N is:

$$k_N = \frac{k}{\left(2^{\beta+1}\right) \pi^{\alpha-1} \left(0.2761 + \frac{1.7061}{\alpha + 1.354} \right)} \qquad (20)$$

and k, α, β, are empirical parameters specific to a ferrite material [15]. B is the peak flux density and V_{core} is the volume of the core.

System loss, ΣP_{loss} can be obtained by summing all the losses in each device of the converter in Fig. 2. The system efficiency is obtained from the total power output ΣP_{out}:

$$Efficiency, \eta = \frac{\sum P_{out}}{\sum P_{out} + \sum P_{loss}} \qquad (21)$$

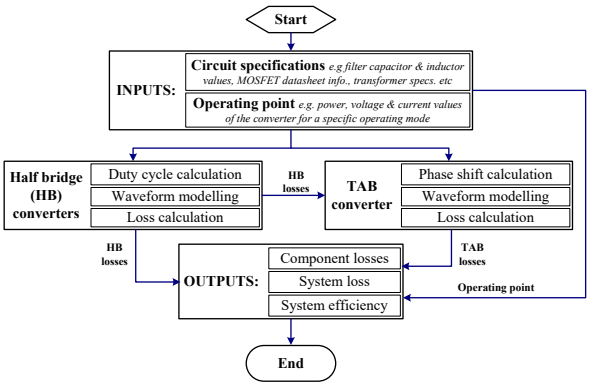

Fig. 8. Flowchart for calculating the power losses and efficiency of the four port DC-DC converter in Fig.1 for each operating mode.

IV. Simulation and Experimental Results

A. Simulation Results

Fig. 8 shows a flowchart used to estimate the converter loss and efficiency using the loss model presented in section II and section III. All four ports of the converter in Fig. 2 are bidirectional. Therefore, sixteen operating modes are possible. To help visualise the modes for power loss estimation and simulation purposes, three cases were analysed as shown in Fig. 9, Fig. 10 and Fig.11. In each case, the power, P_B of HB-B was set to; -160 W, 0 W and 160 W respectively. The choice to set P_B constant is arbitrary; other ports could be chosen instead. In each case, the converter was operated to maintain the power balance, $P_A = \Sigma P_{loss} - (P_B + P_C + P_D)$. This means that HB-A was not directly controlled and it either absorbed power when $P_A < 0$ or supplied power when $P_A > 0$. The first case is defined in Fig. 9 and investigates the power losses when P_B is -160 W

(flows out of the converter). P_B and P_C were varied from -160 W to 160 W so that all the operating modes which are possible for this case are visualised. It can be observed that efficiency is high for the operating modes when P_D values are in the range $P_D \approx$ [-50 W, 50W]. A crease on the efficiency map can also be observed. This is as the result of P_A changing direction as it either absorbs or supplies the balance of power. The efficiency drastically reduces for the operating modes when $P_D >$ 50 W and $P_D <$ -50 W. The second case is shown in Fig.10 and is defined by the operating modes where P_B is set to 0 W and P_C, and P_D are varied as shown in the figure. Efficiency rapidly falls as P_A, P_B, P_C and P_D approach zero as there is a constant component of power loss. Efficiency reaches a maximum for the operating modes where $P_D \approx$ [-50 W, 50W] and $P_C \neq$ 0 W. The third case is shown in Fig. 11 where P_B is set to 160 W and flows into the converter. Similar results to the first and second cases are obtained. Three distinct maximum efficiency regions can be observed. These are defined by the supplying and absorbing action of P_A. Fig. 12 shows the power loss distribution in the converter for a specific operating point given by P_B = -160 W, P_C = 100 W and P_D = -100 W. In this case, passive component and MOSFET turn off switching losses are dominant. Passive component losses are high in the HB-A converter because of the large P_A to supply the power balance and system losses whereas the core losses are low for the given operating mode.

B. Experimental Verification

Fig. 13 shows a 200 W, 100 kHz four port DC-DC converter prototype developed in the laboratory. The circuit parameters are shown in Table II and the MOSFET switches are obtained from Fairchild and are chosen as follows: MOSFET FDD8896/FDU8896 (30V, 94A @ 25°C, 5.7mΩ) chosen for the switches on primary DC/AC, HB-A and HB-B converters, MOSFET FDD10AN06A0_F085 (60V, 50A @ 25°C, 10.5mΩ) for the secondary DC/AC and HB-C converter, and MOSFET FQD18N20V2 (200V, 15A @ 25°C, 140mΩ) for the switches on the tertiary DC/AC and HB-D converter. Fig. 14 presents both the system power losses and efficiencies calculated using the loss model presented in section II and section III, and those obtained by the experiment tests. During the experiment, P_B was varied in the range [0W, 160W] while keeping P_C and P_D constant at 50 W and 45 W respectively. The choice to vary P_B is arbitrary and is intended to contrast with the cases considered in the simulation section above where P_B was set (i.e. supplying power, $P_A = \Sigma P_{loss} + |P_B| - (P_C + P_D)$) and constant. It can be observed that between P_B = -160 W and $P_B \approx$ -70 W, system power loss and efficiency curves are decreasing. This is because during this period, P_A is positive, (i.e. supplying power, $P_A = \Sigma P_{loss} + |P_B| - (P_C + P_D)$) and system efficiency is given by, $\eta = |P_B| / (P_A + P_C + P_D)$ where P_C, P_D are constant. Therefore, by reducing $|P_B|$, the rate at which it will reduce will be higher than that of P_A. Hence the system efficiency reduces despite the reduction in the system power loss as shown in Fig. 14. The efficiency is low when P_A = 0 at $P_B \approx$ -70 W and increases afterwards when P_A (negative) starts to absorb the excess power.

TABLE II
Circuit Parameters of the Experimental Circuit Shown in Fig. 2.

Power rating		200 W
Voltage	$V_1/V_2/V_3$	19 V/38 V/152 V
Leakage inductance	$L_1/L_2/L_3$	720nH/3μH/44μH
Filter inductance	$L_a/L_b/L_c/L_d$	3.3μH/3.3μH/22μH/47μH
Filter capacitance	$C_1/C_2/C_3$	300μH/48μH/4.8μH
Transformer core material		3F3
Maximum flux density	B	100mT
Transformer turn ratio	N_1:N_2:N_3	1:2:8

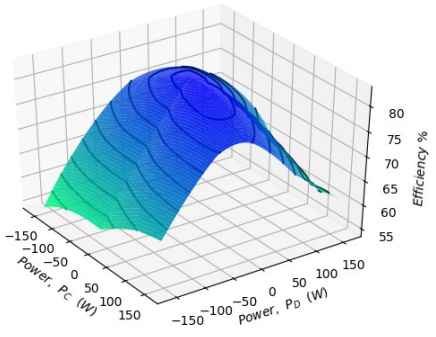

Fig. 9. System efficiencies of the four port DC-DC converter for the operating modes where P_B = -160 W and $P_A = \Sigma P_{loss} - (P_B + P_C + P_D)$.

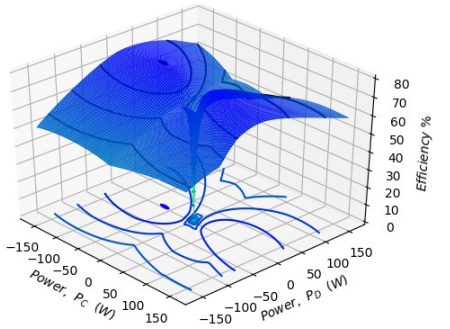

Fig. 10. System efficiencies of the four port DC-DC converter for the operating modes where P_B = 0 W and $P_A = \Sigma P_{loss} - (P_B + P_C + P_D)$.

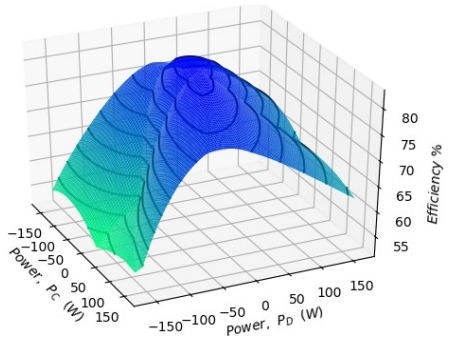

Fig. 11. System efficiencies of the four port DC-DC converter for the operating modes where P_B = 160 W and $P_A = \Sigma P_{loss} - (P_B + P_C + P_D)$.

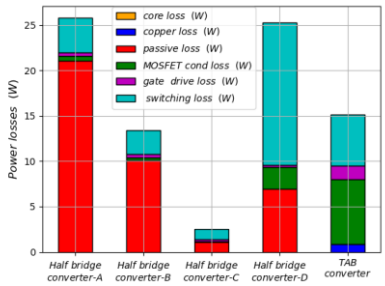

Fig. 12. Four port DC-DC converter power losses distribution for a specific operating point given by P_B = -160 W, P_C = 100 W and P_D = -100 W. $P_A = \Sigma P_{loss} - (P_B + P_C + P_D)$.

Fig. 13. A 200 W, 100kHz four port DC-DC converter laboratory prototype

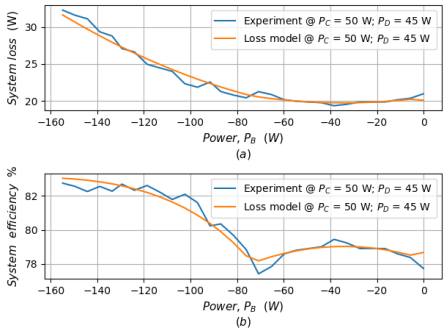

Fig. 14. Predicted and measured (a) system power losses and (b) system efficiencies for different operating modes.

From Fig. 14, the loss model results are consistent with the experiment tests. The small discrepancies could be because of extra experimental losses such as heat and the assumptions made in the loss model. However, thermal effects on the accuracy of the results were minimised by remotely operating the experiment using a Python script to limit the run time of the converter to less than 30 s to avoid heating of the components. From the results, it was found that system losses and efficiencies of the converter (Fig. 2) depends on the operating mode. The highest efficiencies were generally obtained when $P_D \approx$ [-50 W, 50W], i.e. the converter as a whole operates with maximum efficiencies when HB-D is used less; this is a design quirk associated with the particular implementation of the experimental circuit. Most of the losses in the converter result from the passive component and MOSFET turn off switching losses. Conduction losses in the MOSFET switches are relatively low. The results obtained in this paper will be used to improve the converter design so that efficiencies greater than 90% will be obtained. Furthermore, the results will be used to develop high level control strategies that are aimed at reducing the losses.

V. CONCLUSION

A power loss model for a four port DC-DC converter was developed. Converter losses and efficiencies were calculated using this model. It was found that the power losses and efficiencies depend on the operating mode of the converter. For the given four port converter topology, it was found that the converter operated with high efficiency for the operating modes when power, P_D absorbed(supplied) from(to) the terminal of the half bridge converter, HB-D was in the range, $P_D \approx$ [-50 W, 50W]. Most of the power losses in the converter were the passive component and the turn off switching losses in the MOSFETs. The calculated results were compared to the results obtained from a 200 W laboratory prototype and were found to be consistent. The loss model and experimental method developed here can be readily adapted to estimate power losses in other multiport DC-DC converter topologies.

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