Finite Control Set Model Predictive Control of Isolated DC/DC Modular Multilevel Converter

Seema Mir Akbar*†, Ammar Hasan* Alan Watson†, Pat Wheeler† and Shafiq Odhano‡
*School of Electrical Engineering and Computer Science,
National University of Sciences and Technology, Pakistan
†Department of Electrical and Electronic Engineering, University of Nottingham, Nottingham, United Kingdom
‡School of Engineering, Newcastle University, Newcastle upon Tyne, U.K.
Email: seema.akbar@nottingham.ac.uk

Abstract: Isolated DC/DC modular multilevel converters (MMC) consisting of two MMCs isolated by a transformer are one of the converter topologies being considered used for DC/DC conversion in HVDC transmission. Two level modulation can be used to obtain different voltage levels by inserting/bypassing a specific number of sub-modules (SM) in the converter circuit. However, it does not take into account the SM's voltage when elevation factors need to be readjusted, which results in either higher or lower output voltage than the reference. This paper proposes a finite control set model predictive control (FCS-MPC) for output voltage regulation to the reference value. A cost function comprising the output voltages is defined and a mathematical equation is formed to calculate the one step ahead value of output voltage. The number of SMs which minimize the cost function is applied to the converter circuit. Voltage balancing amongst the sub-module cells has been achieved by using a sorting algorithm. The performance of the proposed control strategy is evaluated and verified.

***Index Terms*—Modular multilevel converter (MMC), Finite control set model predictive control (FCS-MPC), elevation factor.**

I. Introduction

High voltage DC (HVDC) transmission technology has become an attractive solution for transmitting electrical power over long distances due to lower line losses [1]–[4]. It can be used for efficient transmission of electrical power generated by renewable energy resources [5], [6]. Power from offshore wind farms can be efficiently transmitted to the utilization point by using HVDC technology [7]. In undersea transmission losses occurring due to distributed capacitance can be reduced by HVDC transmission [7]. Output voltage of solar energy system is DC [8], which lends it more suitable for HVDC transmission. Another application of HVDC system is to interconnect Asynchronous AC grids [1].

Power converters are essential components of HVDC transmission technology. AC/DC converters are required on the power plant side to convert the generated AC into DC for transmission, while a DC/AC converter is needed to supply the DC transmitted power to AC on load side. DC/DC converters are required to interconnect DC microgrids having different voltage levels. Similarly DC/DC converters are also required for tap changing purposes [13]. Tap changing is required to regulate output voltage when it is needed to supply a desired voltage to the load, to encounter voltage drops due to load and to encounter input voltage changes on load.

The modular multilevel converter (MMC) proposed in [9] has a modular structure consisting of multiple submodules (SM) and each SM can be inserted or bypassed in the converter circuit to adjust output voltage, currents and frequency. It can provide high step up/down voltage ratio, thus bulky transformers can be avoided as voltage step up can be achieved by adjusting number of SMs in MMCs. Voltage stress on each switching component is decreased due to modular structure. Multiple capacitors are used each with an SM which results in small currents through capacitors and hence low losses. A number of redundant SMs can be installed in the converter circuit which makes its structure scalable and reliable. Faulty SMs can be easily bypassed. Hence, MMC has several desirable properties which makes it suitable to be used in HVDC transmission [10]. Significant research has been carried out on the MMC and many converter topologies has been presented for AC/DC, DC/AC and DC/DC conversion, which can be used in HVDC transmission [12], [13]. This paper focuses on high voltage DC/DC MMCs as this is relatively new area of research compared to AC/DC and DC/AC MMC applications and many control related issues are open to be resolved [11], [12].

Many topologies of DC/DC MMCs have been proposed in [12]–[17]. A DC/DC converter topology based on voltage divider type structure has been proposed in [17]. This converter has low losses but it can not provide high step up/down ratios. Another converter topology based on MMC with a resonant circuit and rectifier at the output is presented in [17]. Soft switching, high switching frequency and inherent balancing of SMs are the main features of this converter but high current flow limits its applications in HVDC. This converter is unidirectional and cannot be used for step down purposes. The isolated DC/DC MMC presented in [13] is a converter topology that can be used in HVDC transmission for wide range of applications.

An isolated DC/DC MMC consisting of two MMCs: one known as the primary MMC, which converts DC into AC, and the secondary MMC, which converts AC into DC, isolated by a transformer. This is mostly used as a tap changer in HVDC transmission. Two level modulation has been presented in [13]

to obtain high voltage conversion ratios between output and input voltages without utilizing the transformer in a DC/DC MMC. This technique defines two modulation levels by specifying number of active SMs in upper and lower arm of MMC resulting in a certain output to input voltage ratio on each MMC known as elevation factor. Thus two elevation factors, the primary elevation factor k_p and the secondary elevation factors k_s on primary and secondary MMCs respectively are obtained whereas total elevation attained is the product of k_p and k_s.

Elevation factors are required to be readjusted to cope with faulty SMs or to adjust the output voltage with a change in reference. Two level modulation does not take SM voltage into consideration while setting elevation factors, either a greater or lesser voltage appears at the output as time is needed for SMs capacitors to adjust its voltage according to the new setting condition, which is the main drawback of this technique. A control algorithm is needed to select the best possible number of active SMs such that output voltage and current follow the given reference as the two quantities are dependant on number of active SMs.

This paper suggests a finite control set model predictive control (FCS-MPC) [18]–[21] to find optimal number of active SMs instead of using fixed levels as in case of two level modulation when the elevation factor is changed. This control scheme defines a cost function based on the output voltage, and minimize it for finite set of insertion indices(number of SMs to be inserted in an arm). It considers present values of SM voltages and a single step prediction for the value of the voltage. The optimal number of SMs is selected to be inserted in the converter circuit based on cost function. With the application of this control technique the output voltage obtained is always nearer to the reference voltage. The output voltage follows the reference, hence output current is also within the specified limits. The voltages of the SMs is also required to be balanced such that all SMs should have approximately the same voltage, which is equal to the average of all SM voltages in a specific arm. This paper has proposed two sorting algorithm for SM voltage balancing for primary and secondary MMC.

The rest of the paper is organized as follows. Section II describes the isolated DC/DC MMC, its mathematical model and two level modulation to set different elevation factors. It also discusses the shortcomings of this technique when changing elevation factors. The proposed solution is presented in Section III. Simulation results showing the comparison of two level modulation and the proposed solution are given in Section IV. Section V provides conclusion of the paper.

II. Isolated DC/DC Modular Multilevel Converter

The isolated DC/DC MMC, presented in [13], consists of two MMCs, known as the primary MMC and the secondary MMC, and a transformer which interconnects the two converters. The primary MMC converts DC into AC and the secondary MMC converts AC into DC with specific elevation factors. The transformer is used for isolation and can also provide voltage elevation if needed but generally voltage elevation is provided by the operation of the MMCs and a 1:1 ratio transformer is used. High frequency can be used with this type of converter. Since component size is inversely proportional to frequency small size capacitors, inductors and transformers can be used with the isolated MMC. Frequency is only limited by switching losses and transformer insulation requirement.

The isolated DC/DC MMC can be three phase or single phase. In this paper we will focus on single phase isolated DC/DC MMCs shown in Fig.1. Each MMC of a single Phase isolated DC/DC MMC consists of two legs where each leg has two arms, the upper arm and lower arm. Each arm is composed of N number of identical SMs and an inductor.

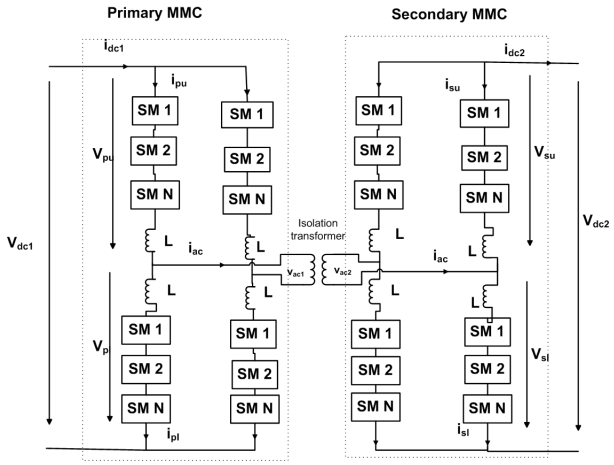
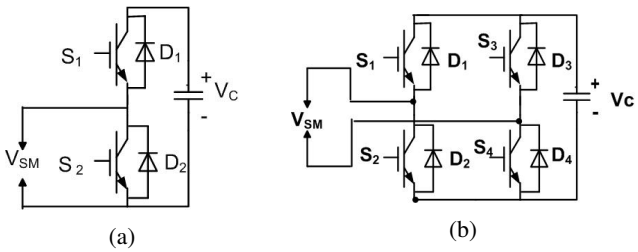


Fig. 1: Isolated Single Phase DC/DC Modular Multilevel Converter

A simple and commonly used realization of SM is shown in Figure 2(a). It comprises of two switches connected in half bridge configuration and a capacitor having voltage V_c [11]. Two voltage levels '0' also known as off state and 'V_c' known as on or active state can be obtained using this configuration. Another type of SM consisting of a capacitor and four switches connected in full bridge configuration is shown in Figure 2(b) [11], [12]. Three different voltage levels '0' , V_c and -V_c can be obtained using this configuration.

The number and the structure of SMs can be different for primary and secondary MMCs but all arms of each MMC have the same number of SMs with similar structure. SMs with half bridge circuit configuration are used in the secondary MMC while full bridge SMs are used in primary MMC for



(a) (b)

Fig. 2: Submodule Structure: (a) Half Bridge. (b) Full Bridge.

providing elevation factor if required, otherwise half bridge SMs are sufficient for DC to AC conversion.

A. Mathematical Modelling of the converter

Different voltages and currents of the converter are given as:

V_{dc1}: input voltage of primary MMC
V_{ac1}: output voltage of Primary MMC
V_{ac2}: input voltage of secondary MMC
V_{dc2}: output voltage of Secondary MMC
i_{dc1},i_{dc2}: input current and output current of the converter
V_{pu}, V_{pl}: upper and lower arm voltages on primary MMC respectively
i_{pu}, i_{pl}: upper and lower arm currents on primary MMC respectively
V_{su}, V_{sl}: upper and lower arm voltages on secondary MMC respectively
i_{su}, i_{sl}: upper and lower arm currents on secondary MMC respectively
i_{ac}: current in transformer
V_{cp},V_{cs}: voltage of an SM on primary and secondary MMC respectively

The input voltage V_{dc1} and output voltage V_{dc2} are constant, the capacitor voltages of all SMs are equally fixed, and the currents and voltages of opposite arms are same as assumed in [13] while deriving the model of isolated DC/DC MMC.

If $n_{inserted}$ is the number of inserted SMs in an arm, each having a voltage of V_c, and assuming that each SM has almost the same voltage, which is equal to the average of SMs voltage, then the voltage of the arm is given by:

$$V_{arm} = n_{inserted} * V_c$$

$$i = C_{eq}\frac{dV^{\Sigma}}{dt} \tag{1}$$

If V is the total voltage of an arm and C_{eq} is the equivalent capacitance of all capacitors in an arm then current, i, through the arm is given by:

$$i = C_{eq}\frac{dV}{dt} \tag{2}$$

By rearranging equation (2)

$$\frac{dV^{\Sigma}}{dt} = \frac{i}{C_{eq}} \tag{3}$$

where

$$C_{eq} = \frac{C}{n_{inserted}} \tag{4}$$

C is the capacitance of each SM's capacitor and $n_{inserted}$ is the number of inserted SMs in an arm.

From equations (3) and (4)

$$\frac{dV^{\Sigma}}{dt} = \frac{n_{inserted}}{C} * i \tag{5}$$

Using Euler methods and assuming a sampling period of T_s, equation (5) can be presented in discrete-time to obtain the predicted value of voltage for next state V_{k+1}:

$$V_{k+1} = V_k + \frac{n_{inserted}}{C} * i * T_s \tag{6}$$

$V^{ave}{}_{s\_upper}$: Average voltage of an SM in upper arm which is calculated as:

$$V_{s\_upper}^{ave} = \frac{V_{s\_upper}^{\Sigma}}{N} \tag{7}$$

and $V^{ave}{}_{s\_lower}$: Average voltage of an SM in lower arm, which is calculated as:

$$V_{s\_lower}^{ave} = \frac{V_{s\_lower}^{\Sigma}}{N} \tag{8}$$

Voltages in upper and lower arms of secondary MMC using Equation(6) are given by:

$$V_{su}(k+1) = V_{s\_upper}^{ave} * n_{s\_upper} + \frac{n_{s\_upper}}{C_s} * i_{su} * T_s \tag{9}$$

$$V_{sl}(k+1) = V_{s\_lower}^{ave} * n_{s\_lower} + \frac{n_{s\_lower}}{C_s} * i_{sl} * T_s \tag{10}$$

where

n_{s_upper}, n_{s_lower}: number of SMs to be inserted in upper arm and lower arm of secondary MMC

The arm currents can be calculated by applying KCL to the converter circuit:

$$i_{su} = -\frac{i_{ac}}{2} - \frac{i_{dc2}}{2} \tag{11}$$

$$i_{sl} = \frac{i_{ac}}{2} - \frac{i_{dc2}}{2} \tag{12}$$

By applying KVL to the converter circuit input and output voltage can be expressed as:

$$V_{dc2} = V_{su} + V_{sl} \tag{13}$$

which can be can be written as in equation (14)

$$V_{dc2}(k+1) = V_{su}(k+1) + V_{sl}(k+1)) \tag{14}$$

From equation (9), (10) and (14) the next state value of output voltage is given by:

$$V_{dc2}(k+1) = V_{s\_upper}^{ave} * n_{s\_upper} + \frac{n_{s\_upper}}{C_s} * i_{su} * T_s + V_{s\_lower}^{ave} * n_{s\_lower} + \frac{n_{s\_lower}}{C_s} * i_{sl} * T_s \tag{15}$$

From the above equations it is clear that n_{s_upper} and n_{s_lower} are the insertion indices to be determined by the controller to maintain the output voltage at the reference value.

B. Two level modulation

A modulation technique inspired by dual active bridge named as two level modulation has been presented in [13] for the isolated DC/DC MMC. The magnitude of square waves at the output of primary MMC and DC output of the secondary MMC can be changed in discrete steps. This technique is named as two level modulation as two levels for voltage are selected by activating N_1/N_2 where N_1 is number of active SMs in upper arm in positive half cycle and N_2 is number of active SMs in lower arm in positive half cycle. After the half cycle the number of active SMs for upper and lower arm interchanges. Two elevation factors have been defined

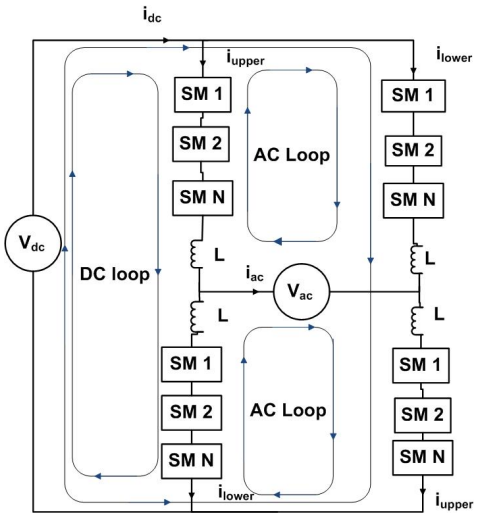


Fig. 3: voltage elevation

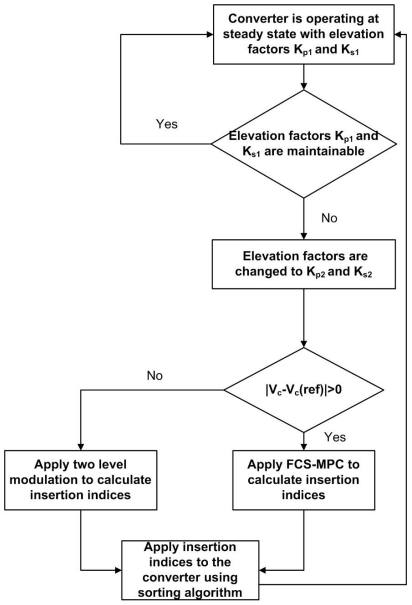


Fig. 4: Proposed Control Technique

for primary and secondary MMC. K_p is the primary elevation factor and K_s is the secondary elevation factor. The output voltage is given by:

$$V_{dc2} = K_p * K_s * V_{dc1} \tag{16}$$

The secondary MMC voltage is phase shifted from primary MMC voltage by a phase angle which can be changed to control the power flow. Bipolar/full bridge SMs are necessary to provide voltage elevation in primary MMC, unipolar/half bridge SMs are sufficient to provide voltage elevation on secondary side. The circuit shown in Fig. 3 is used to explain the elevation factors both on primary and secondary sides. Two types of loops are present in this circuit. A loop containing the DC voltage and two branches upper and lower is known as DC loop while sum of SMs in a DC loop is called as N_{dc}. A loop containing the AC voltage and two branches is known as the AC loop and sum of SMs in AC loop is known as N_{ac}. There are two identical DC loops and two identical AC loops. The primary and secondary elevation factors are given by:

$$K_p = \frac{N_{ac}}{N_{dc}} \tag{17}$$

$$K_s = \frac{N_{dc}}{N_{ac}} \tag{18}$$

SMs voltage balancing is achieved by implementing a sorting algorithm or a swapping balance scheme presented in [13].

Two level modulation is capable of obtaining voltage elevation in each MMC and capacitors gets charged according to the available input voltage and number of active SMs in a leg. Capacitors maintain a constant voltage level under steady state conditions and converter provides a constant output voltage according to the selected elevation factors. Different elevation factors can be obtained by changing the number of active SMs. As discussed earlier, this converter can be used as a tap changer where output voltage regulation is required and elevation factors needs to be changed with changing reference voltage. Similarly if a number of faulty SMs increases beyond the available number of redundant SMs then required elevation factor can not be maintained with available number of SMs on that specific primary or secondary MMC. Elevation factors on both primary and secondary MMC are needed to be changed to get the same total elevation factor as before the occurrence of the fault for constant output voltage.

The elevation factors are adjusted according to the reference voltage and input voltage relation given by equation (16) but the resultant output voltage will not be equal to the reference voltage. The capacitor voltage does not change instantly as soon as its charging voltage changes hence, the SMs will retain the previous voltage, resulting in higher/lower output voltage than the reference. Control techniques are required to be designed to select appropriate number of SMs to get output voltage same as reference voltage in the case of a tap changing process or fault. This paper proposes a FCS-MPC based algorithm to cope with the discussed situation.

III. Proposed Control Technique

The proposed control scheme is shown in Fig. 4. It considers the scenario when elevation factors at steady state K_{p1} and K_{s1} are not maintainable due to a fault or tap changing with new elevation factors K_{p2} and K_{s2}. It suggests that the two level modulation should be implemented on the primary side with the new elevation factor. However, FCS-MPC is used on secondary side to adjust the output voltage. The voltage of each SM is measured on secondary MMC and compared with a reference as given by equation (19).

$$V_{SM}^{ref} = \frac{V_{dc2}^{ref}}{K_s} \tag{19}$$

If the norm of the difference of SM voltages and its reference is greater than zero, FCS-MPC is used to calculate insertion indices for both upper and lower arms at discrete steps instead of using constant modulation levels on secondary MMC. If

norm of the difference of SM voltages and its reference is equal to zero, two level modulation is applied by deriving insertion indices from the new secondary elevation factor. A sorting algorithm is used in both cases for SM voltage balancing.

FCS-MPC and sorting algorithms are discussed in the following sub sections.

A. FCS-MPC

FCS-MPC is emerging as an efficient technique for controlling power converters [18]–[21]. This technique calculates a one step ahead value of a predefined cost function for every possible control action, and the control action which minimizes the cost function is selected. This control technique differs from other predictive techniques in that it uses a cost function to find the optimal control set from available finite set of control actions [21]. The converter model is used to predict the output voltage at each sample time for every valid control set. Cost functions can have single term or many terms depending on the control requirements of system. The general form of cost function is:

$$J = \sum_{i} Q_i |x_i(k+1) - x_i^{Ref}(k+1)| \tag{20}$$

A cost function, represented by J, is the summation of the difference between the reference value and predicted value of the controlled variables x. Constraints can also be included in the cost function. A discrete model of the system is used to predict the values of controlled variables. Q represents weighting factor, specific values of Q are used with each term that allow the level of compromise to be adjusted between different terms of cost function. The cost function is evaluated for finite set of control actions in FCS-MPC and the control action which minimizes the cost function is applied to the system. A flow diagram of FCS-MPC is shown in Fig. 5. One step ahead prediction values of output voltage is calculated by equation (15) for all possible values of insertion indices n_{upper} and n_{lower} (1 to N(total number of SMs in an arm)) based on measured values of quantities i_{su}, i_{sl}, $V^{ave}{}_{upper}$ and $V^{ave}{}_{lower}$ from the converter circuit as shown in the block diagram in Fig.6. The cost function, given by equation (21), derived from equation (20), is evaluated for all possible values of insertion indices.

$$J = |V_{dc2}(k+1) - V_{dc2}^{Ref}(k+1)| \tag{21}$$

Insertion indices minimizing the cost function are selected and applied to the converter for that specific sampling period. The capacitor voltage balancing task is achieved by sorting algorithm discussed in next subsection.

B. Capacitor Voltage Balancing

As discussed earlier, capacitor voltage balancing is an important task in MMC operation. Sorting algorithms and fixed swapping schemes are used for this purpose. In this work a sorting algorithm, based on the sorting algorithm presented in [22], [23], is used for capacitor voltage balancing

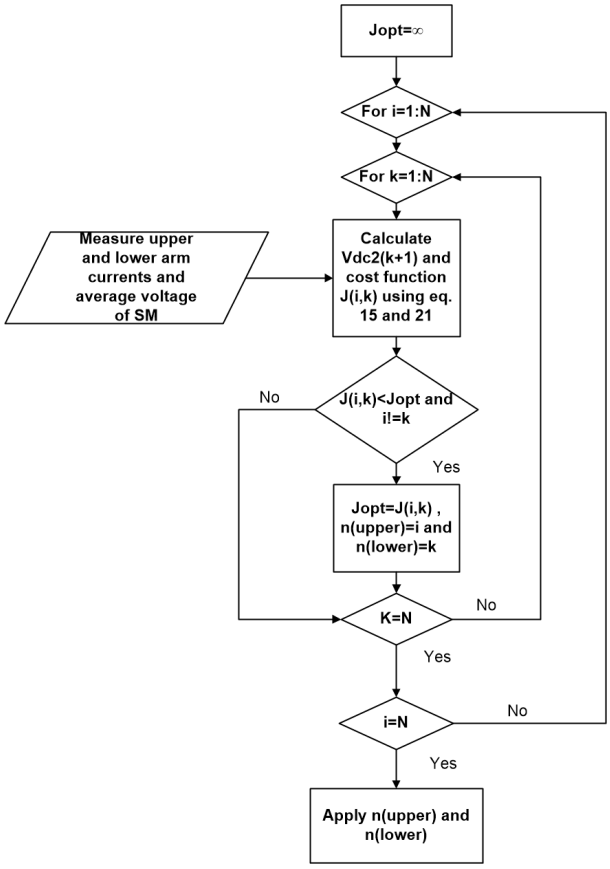


Fig. 5: Flow chart of FCS-MPC

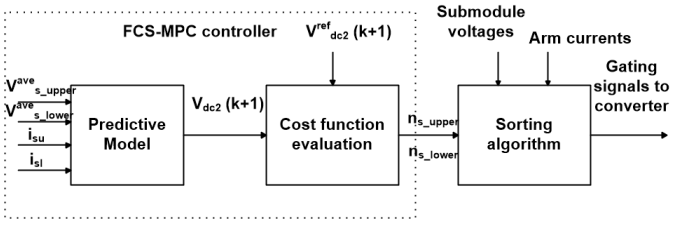


Fig. 6: Block Diagram of FCS-MPC

for both primary and secondary MMC. Since the primary and secondary side SM topologies are different, the sorting algorithms used for primary and secondary MMC msut also be different. The sorting algorithm bypasses SMs having minimum voltage and insert a SM having maximum voltage if there is a discharging current flowing through the arm. If charging current is flowing then SMs having maximum voltage are bypassed while SMs having minimum voltage are inserted in the circuit in order to charge the capacitors. Thus all SMs maintains a balance voltage, which is equal to the average voltage of SMs of an arm.

The number of SMs to be inserted in upper or lower arm of a leg in primary is presented by $n_{inserted}$, if it is negative then SMs are inserted, providing negative voltage, and if it is positive then SMs with providing positive voltage are inserted in a specific arm. All SMs are arranged in descending order with respect to its output voltages. At every sample time

TABLE I: Simulation Parameters

Parameters	Values
Input voltage V_{dc1}	1kV
Reference output voltage V^{ref}_{dc2}	5kV
SM Capacitance of primary MMC C_p	69mF
SM Capacitance of Secondary MMC C_s	50mF
Primary inductance value L_p	0.8 μ H
Secondary inductance value L_s	0.7 μ H
Number of SMs per arm in Primary MMC	3
Number of SMs per arm in secondary MMC	3
Transformer ratio	1:1
Sampling time T_s	0.05 ms

$n_{inserted}$ and arm current are checked. If both $n_{inserted}$ and current are positive, then SMs equal to $n_{inserted}$ and having minimum voltages are inserted in the arm with each SM providing positive voltage. If $n_{inserted}$ is positive but current is negative, then SMs equal to $n_{inserted}$ and having maximum voltages are inserted in the arm with each SM providing positive voltage. If $n_{inserted}$ and current are negative, then SMs equal to $n_{inserted}$ and having minimum voltages are inserted with each SM injectng negative voltage in the circuit. If $n_{inserted}$ is negative but current through arm is positive, then SMs $n_{inserted}$ and having maximum voltages are inserted in the circuit with each SM providing negative voltage.

As unipolar SMs are utilized in secondary MMC hence these can be inserted in an arm of converter only providing positive voltage and $n_{inserted}$ is always positive. All SMs are grouped into off state and on state/active, and arranged in descending order with respect to its output voltages. The difference of $n_{inserted}$ and active SMs is checked and if the difference of the SM voltages is positive and current through arm is also positive, then SMs equal to the difference and having minimum voltages among the off state are inserted in the arm. If the difference of $n_{inserted}$ and active SM voltages is positive and current through arm is negative, then SMs equal to the difference and having maximum voltages among the off state SMs are inserted in the arm. If the difference is negative and current through arm is positive, then SMs equal to the difference and having maximum voltages among the on state SMs are bypassed in the arm. If both the votlage difference and current through arm are negative, then SMs equal to the difference and having minimum voltages among the on state SMs are bypassed in the arm.

IV. Simulation Results

To evaluate the performance of the proposed control strategy an isolated DC/DC MMC is simulated in Matlab Simulink. The simulation parameters are given in the Table. 1. A circuit similar to Fig. 1 is constructed in simulink. There are two legs in each converter which consists of two arms each having three SMs. Full bridge/bipolar SMs have been used in primary MMC to provide an elevation factor on primary side. Half bridge/unipolar SMs have been used on secondary MMC. Initially the converter is operating at a total elevation factor equal to five. The input voltage is 1kV dc and output voltage is 5kV dc with an elevation factor of five. Two level modulation is used on both primary and secondary MMC. The primary elevation factor K_p= 5 which can be obtained with "3/-2"-modulation. The primary MMC converts 1kV dc into a square wave having magnitude of 5kV. Each SM capacitor has obtained an average voltage of 1kV. A sorting algorithm has been implemented for capacitor voltage balancing. It sorts SMs based on capacitor voltage and gives gating signals to the converter by taking the arm current into account. To get 5kV DC at output a secondary elevation factor K_s=1 is used which is achievable with "3/0"-modulation. Each SM has an average voltage of 1.64kV. Capacitor voltage balancing is achieved by using sorting algorithm.

At time t>0.05 seconds the primary and secondary elevation factors are changed whilst keeping the total elevation factor equal to five as before. According to existing literature, two level modulation can be used to obtain K_p= 1 and K_s=5 resulting in a total elevation factor of five. Another option is to use FSC-MPC as suggested in this paper. The converter is operated with and without FCS-MPC. The performance of both cases is discussed in the following subsections.

A. Simulation of Isolated DC/DC MMC without FCS-MPC

According to existing literature a possible solution is to set the primary elevation factor K_p= 1 and secondary elevation factor K_s=5 to obtain a total elevation factor of five. Two level modulation is used on both primary and secondary MMC to obtain the voltage elevation at the output. A two level modulation scheme with "3/0"-modulation is used on primary MMC to get an elevation factor of 1. We can also use "1/0" or "2/0"-modulation but "3/0"-modulation is a better option as in this case each SM will heve a voltage of 0.33kV compared to the "1/0" and "2/0" case where SM voltage will be 1kV and 0.5kV respectively. Thus using "3/0"-modulation decreases the voltage stress on switches. The input voltage is converted from 1kV DC to a square wave of magnitude 1kV at this stage. A two level modulation of "3/2" is used on secondary side to obtain an elevation factor of five.

B. Simulation of Isolated DC/DC modular multilevel converter with FCS-MPC

In the proposed control technique two level modulation has been used only on the primary MMC. An elevation factor of one is achieved by using "3/0"-modulation on primary side. It converts the 1kV DC input voltage to a square wave of magnitude 1kV. On the secondary side a controller based on FCS-MPC has been used. A block diagram of the controller is shown in Fig. 6. A flow chart of FCS-MPC controller has been presented in Fig.4 . Since the aim is to only control the output voltage the cost function is only optimized for this voltage. The proposed controller predicts one step ahead value of the output voltage using equation (15). In second stage, the controller calculates the optimal value of insertion indices using a cost function based on the reference voltage. The optimal number of lower and upper SMs is applied to the secondary MMC through a sorting algorithm which balances voltages of SMs in an arm.

C. Analysis of results for proposed FCS-MPC and existing two level modulation

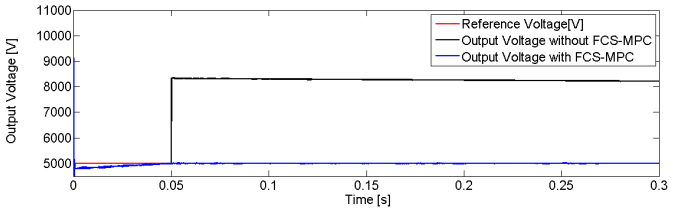
The output DC voltage for both cases is shown in Fig. 7a. At t=0.05seconds the converter has attained steady state operation and each SM of secondary MMC has obtained a voltage of approximately 1.64 kV. With a k_s=5, which can be achieved by a "3/2"- modulation, five SMs are connected in series during each cycle at the output terminals. Ideally the SM voltage should be 1kV but due to capacitor characteristics it will take some time to change from 1.64KV to 1kV. Thus the output DC voltage is approximately 8.2 kV which is much higher than the reference voltage. This SM voltage will gradually decrease and reduces to 1kV and then "3/2"- modulation will result in 5kV which is the reference voltage. However, it takes a long time and in this duration the other systems connected at the output of converter may become damaged. With a load at a rated voltage of 5kV and power of 20 kW the output current should be 4 A. At t<0.05 the output current is 4A under steady state conditions as shown in Fig. 7b. However, at t>0.05 with "3/2"-modulation the output current increases to 6.5A resulting in high current stress on switches and also an increase in losses.

According to proposed control scheme an elevation factor of five is not used until each SM voltage is greater than 1kV. SM voltages are measured for each half cycle and compared with the reference voltage. This controller calculates optimal number of SMs to be inserted in secondary MMC and as shown in Fig.7a the output voltage is always near to the reference voltage. Similarly, the output current for FCS-MPC control strategy is equal to 4A (Fig. 7b) as expected. This will decrease conduction losses occurring on the secondary MMC and will also reduce the current stress on each switch. As the capacitor voltage drops to 1kV then the controller will shift the secondary elevation factor to five. A "3/2"- modulation can then be used then to obtain an output voltage of 5kV.

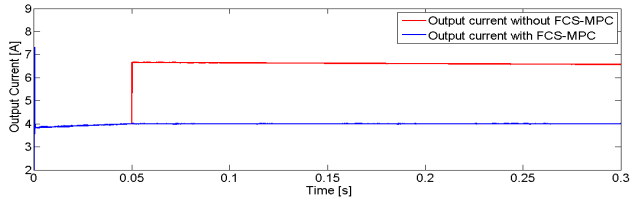
The number of SMs in upper and lower arms of the secondary MMC during the positive and negative half cycles are shown in Fig. 7c - Fig. 7f. These figures show that FCS-MPC selects optimal insertion indices to minimize the error between the reference and the predicted voltage in each cycle. This controller results in elevation factor of three on secondary MMC as the number of SMs is fluctuating between one and two.

V. Conclusion

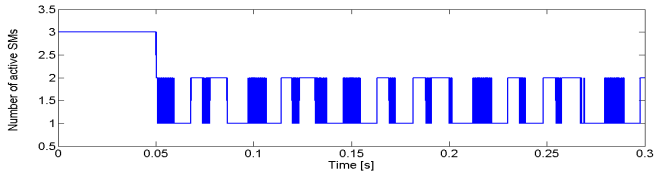
This paper has presented a control technique based on FCS-MPC to improve the performance of an isolated DC/DC MMC during tap changing or to cope with faulty SMs. Two level modulation has been studied in this paper and it is shown that SMs are not able to adjust their output voltage quickly when elevation factors are changed to cope with faulty SMs or tap changing resulting in a different value than the required output voltage. This paper suggests that FCS-MPC should be used to specify insertion indices instead of using fixed elevation factors as specified by two level modulation until the SM voltage is equal to the reference voltage. The



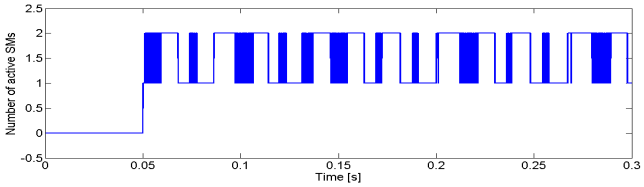
(a) Output Voltage



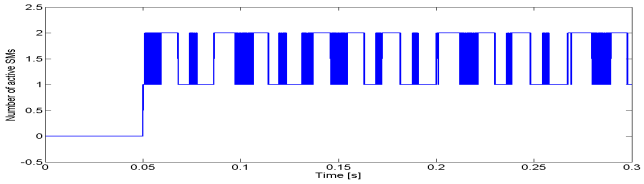
(b) Output current



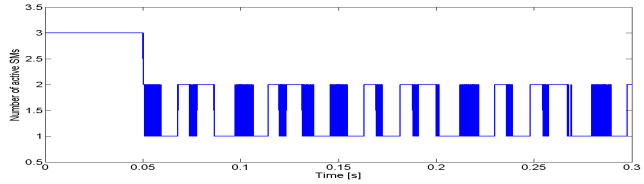
(c) Number of active SMs in upper arm of Secondary MMC during positive half cycle



(d) Number of active SMs in upper arm of Secondary MMC during negative half cycle.



(e) Number of active SMs in lower arm of Secondary MMC during positive half cycle



(f) Number of active SMs in lower arm of Secondary MMC during negative half cycle

Fig. 7: Simulation Results

mathematical model of the converter has been used to define a cost function based on output voltage to calculate the optimal insertion indices. A sorting algorithm has been used for SM voltage balancing on both the primary and secondary side of the MMC. Simulations have been performed which show the effectiveness of the proposed algorithm.

REFERENCES

[1] R. Rudervall, J. Charpentier, and R. Sharma, "High voltage direct current transmission systems technology, " ABB Power Syst. Sweden, Review Paper, 2000.

[2] B. R. Andersen, "HVDC transmission-Opportunities and challenges," in Proc. 8th IEE Int. ACDC, Mar. 2006, pp. 24–29.

[3] Heyman, Olof, Lars Weimers, and Mie-Lotte Bohl. "HVDC-A key solution in future transmission systems." World Energy Congress-WEC. 2010.

[4] www.siemens.com/press/HVDC-Inelfe

[5] Teske, Sven, et al. Energy [r] evolution-a sustainable world energy outlook. Greenpeace International, EREC and GWEC, 2012.

[6] J. M. Carrasco et al., "Power-Electronic Systems for the Grid Integration of Renewable Energy Sources: A Survey," in IEEE Transactions on Industrial Electronics, vol. 53, no. 4, pp. 1002-1016, June 2006.

[7] N. Kirby, L. Xu, M. Luckett, and W. Siepmann, "HVDC transmission for large offshore wind farms," Power Eng. J., vol. 16, no. 3, pp. 135–141, Jun. 2002

[8] Blaabjerg, F.; Zhe Chen; Kjaer, S.B., "Power electronics as efficient interface in dispersed power generation systems," in Power Electronics, IEEE Transactions on , vol.19, no.5, pp.1184-1194, Sept. 2004

[9] Lesnicar, A.; Marquardt, R., "An innovative modular multilevel converter topology suitable for a wide power range," in Power Tech Conference Proceedings, 2003 IEEE Bologna , vol.3, no., pp.6 pp. Vol.3-, 23-26 June 2003

[10] Marquardt, R., "Modular Multilevel Converter: An universal concept for HVDC-Networks and extended DC-Bus-applications," in Power Electronics Conference (IPEC), 2010 International , vol., no., pp.502-507, 21-24 June 2010

[11] Debnath, S.; Jiangchao Qin; Bahrani, B.; Saeedifard, M.; Barbosa, P., "Operation, Control, and Applications of the Modular Multilevel Converter: A Review," in Power Electronics, IEEE Transactions on , vol.30, no.1, pp.37-53, Jan. 2015

[12] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro and R. Lizana, "Circuit Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters," in IEEE Transactions on Power Electronics, vol. 30, no. 1, pp. 4-17, Jan. 2015. doi: 10.1109/TPEL.2014.2310127

[13] Kenzelmann, S.; Rufer, A.; Dujic, D.; Canales, F.; De Novaes, Y.R., "Isolated DC/DC Structure Based on Modular Multilevel Converter," in Power Electronics, IEEE Transactions on , vol.30, no.1, pp.89-98, Jan. 2015

[14] M. Saeedifard and R. Iravani, "Dynamic Performance of a Modular Multilevel Back-to-Back HVDC System," in IEEE Transactions on Power Delivery, vol. 25, no. 4, pp. 2903-2912, Oct. 2010. doi: 10.1109/TPWRD.2010.2050787

[15] D. Shen, A. Kraemer and D. Dohnal, "Vacuum Switching Technology Improves the Switching Capacity of On-Load Tap-Changers in HVDC Applications," 2006 International Conference on Power System Technology, Chongqing, 2006, pp. 1-6.

[16] J. A. Ferreira, "The Multilevel Modular DC Converter," in IEEE Transactions on Power Electronics, vol. 28, no. 10, pp. 4460-4465, Oct. 2013.

[17] X. Zhang, T. C. Green and A. Junyent-Ferré, "A New Resonant Modular Multilevel Step-Down DC–DC Converter with Inherent-Balancing," in IEEE Transactions on Power Electronics, vol. 30, no. 1, pp. 78-88, Jan. 2015.

[18] R. Vargas U. Ammann S. Kouro, P. Cortes and J. Rodriguez. Model predictive control- a simple and powerful method to control power converters. IEEE Transactions on Industrial Electronics, 56(6), Jun 2009.

[19] J. I. Yuz J. Rodriguez S. Vazquez P. Cortes, G. Ortiz and L. G. Franquelo. Model predictive control of an inverter with output lc filter for ups applications. IEEE Transaction on Industrial Electronics, 56(6):1875–1883, 2009.

[20] C. Silva P. Correa P. Lezana P. Cortes J. Rodriguez, J. Pontt and U. Ammann. Predictive current control of a voltage source inverter. IEEE Transaction on Industrial Electronics, 54(1):495–503, 2007.

[21] T. Geyer. A comparison of control and modulation schemes for medium-voltage drives: Emerging predictive control concepts versus pwm-based schemes. IEEE Transaction on Industry Applications, 47(3):1380–1389, 2011.

[22] Vatani, M.; Bahrani, B.; Saeedifard, M.; Hovd, M., "Indirect Finite Control Set Model Predictive Control of Modular Multilevel Converters," in Smart Grid, IEEE Transactions on , vol.6, no.3, pp.1520-1529, May 2015

[23] H. Nademi, A. Das, and L. Norum, Modular multilevel converter with adaptive observer of capacitor voltages, IEEE Trans. Power Electron., vol. 30, no. 1, pp. 235248, Jan. 2014.