Design and Implementation of GaN-based Dual-Active-Bridge DC/DC Converters

Quanxue Guan*, Luigi Rubino†, Zhenyu Wang*, Serhiy Bozhko*
*Department of Electrical and Electronics Engineering, University of Nottingham, U.K.
†Department of Industrial and Information Engineering, Seconda Universita Degli Studi Di Napoli, Italy
Email: quanxue.guan@nottingham.ac.uk, luigi.rubino@unicampania.it, (ezzzw1, eezsb1)@nottingham.ac.uk

***Abstract*—This paper presents the design and implementation of multicellular isolated bidirectional dual-active-bridge (DAB) DC/DC converters which are the core equipment of the European CleanSkyII Project ASPIRE. Both the primary and the secondary H-bridge circuits use gallium nitride (GaN) devices which enable high frequency operation. Between two H-bridge circuits is a planner transformer which is customized for the frequency range from 100kHz to 300kHz, saving the volume and weight. Three proportional integral controllers in parallel are also proposed to control the power transfer and compensate the DC offset values to the transformer, providing efficient operation in both buck and boost modes, allowing on-fly turn-on, turn-off and fast power reversal. Experiment results validate that the converters satisfy the requirements of the Project ASPIRE for the use in more electric aircrafts.**

***Index Terms*—Dual-Active-Bridge converter, gallium nitride device, isolated bidirectional DC/DC converter, more electric aircraft**

I. Introduction

In the recent decades, both the direct current (DC) supplies, energy storage systems and loads have been widely applied in power distribution network [1], [2]. Due to such trend, isolated bidirectional DC/DC converters are significantly demanded. This is specially true for more electric aircrafts (MEA) where the aeronautical electrical network has two DC buses, 270V and 28V respectively, and energy is required to flow bidirectionally between two electric buses [3]–[6].

The project ADVANCED SMART-GRID POWER DISTRIBUTION SYSTEM (ASPIRE) [7] aims at developing a set of isolated bidirectional DC/DC converters to control the energy flow between two DC buses with decentralized supervisors and intelligent energy manage strategies for Regional Aircrafts. The cellular DC/DC converters are the fundamental of the system which enables the Smart Grid concept. In case any of the converter is faulty or overloaded other converters can still share the power and supply the energy robustly.

According to requirements of the energy management, the key design parameters for the ASPIRE DC/DC converter cells are numerated below.

- *Power rating:* 3 kW
- *Primary side voltage:* 270VDC
- *Secondary side voltage:* 28VDC
- *Transformer turns ratio:* 10:1
- *Fast power reversal:* ms range
- *Switching frequency:* above 100kHz

CLLC Resonant Converter (CLLC-RC) and Dual-Active-Bridge (DAB) Converter topologies match well the requirements of DC/DC converters in MEA power systems. The CLLC-RC generally provides full soft switching for secondary side bridge and zero current turn-on for the primary bridge and thus boasts low switching losses [8], [9]. Besides, the core saturation problem is avoided since no DC offset current flows in the transformer due to the existence of DC-blocking capacitors [10]. This also makes the converter insensitive to the DC voltage disturbances. However, the additional resonant capacitor bank decreases the system reliability and slows down the power reversal rate. Because the switching frequency has to be controlled with respect to the resonant frequency, complex variable frequency control methods are required but these are sensitive to parameters variations.

On the contrary, DAB converters generally have low total components count, fast power reversal capability, high reliability and robust to circuit parameter variations because of the absence of capacitors in the high-frequency alternating current link loop. Furthermore, they can achieve wide-range zero voltage switching (ZVS) turn-on operation by using simple modulation technique [11]. However, any imbalance in the H-bridge circuitries will accumulate offset currents and then cause severe saturation to the transformer core [12]. Besides, DAB has higher switching loss than CLLC-RC when the input and output voltage significantly vary from the nominal values. After a thorough consideration, ASPIRE project chooses DAB topology as the preferential solution majorly owing to the fast power reversal capability and high reliability which is critical for MEA applications [13].

The harsh environment of the on-board power systems often calls for the utilization of the wide band-gap (WBG) power devices that have the potential for high-temperature high-frequency scenarios [14]–[16]. WBG devices also contribute to the improvement in terms of efficiency and power density thanks to low conduction and switching losses. A simulation model of 270V/28V DAB converter for MEA applications was developed to compare the performance of silicon carbide (SiC) devices and silicon devices [17]. However, the switching frequency is limited below 60kHz according to the characteristics of SiC devices [18], [19]. To further reduce the size

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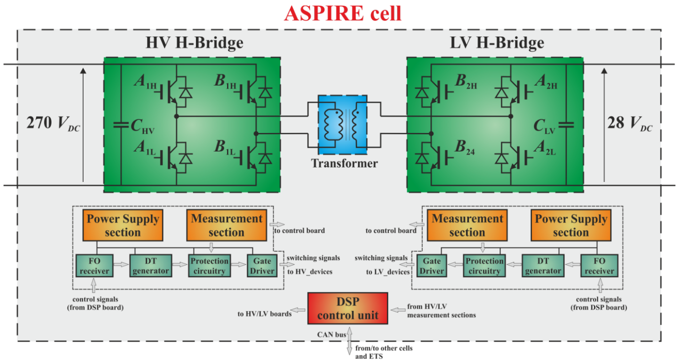

Fig. 1. Isolated bidirectional Dual-Active-Bridge DC/DC converter.

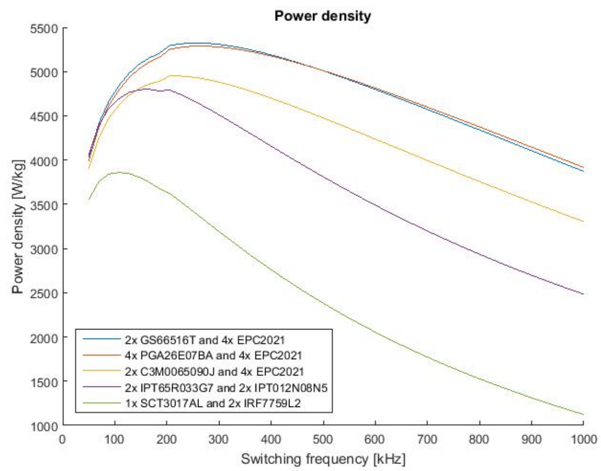

Fig. 2. Power density as a function of switching frequency for different semiconductor devices combinations.

of passive components, for example the transformer, gallium nitride (GaN) devices are highly preferred. A high step-down 150-to-12V, 150W converter with 1MHz switching frequency and peak efficiency around 93% was designed in [17]. Xue et al. obtained a peak efficiency of 96.4% with a 300V input, 300V output DAB converter working at 2.4 kW power output and 500 kHz switching frequency [20], [21]. Other high-efficient GaN-based DC/DC converters have been reported with revised topologies [22], [23].

This paper presents the design and implementation of high-frequency DAB converters with high step ratio using GaN devices at both the primary and secondary H-bridge circuitries.

II. Hardware Design

The single phase DAB converter is shown in Fig. 1. A simulation model is built with PLECS to explore the power density potential of different device combination. The results in Fig. 2 show that the combination to use two GS66516T GaN FETs working in parallel for the high voltage (HV) side while six EPC2021 GaN FETs in parallel for the low voltage (LV) side gives the highest power density among the others. This combination facilitates the minimization of conduction losses at the secondary low voltage side and provides sufficient safety margin in case the open-circuit of any GaN FETs.

A. Low-voltage H-bridge Board

The overall structure and signal flow of the LV boards are shown in Fig. 3. The LV H-bridge comprises of the fibre optic receivers and transmitters circuit, dead-time adjustment circuit, protection circuit, main power circuit with gate driving circuit, the measurement circuit and auxiliary power supply circuits.

The most critical part of the design is the gate drive circuitry for the paralleled GaN devices, due to the high carrying current and high di/dt. To improve the consistency among the six devices paralleled as one switch, two gate drivers are used, each of them driving three devices. The track length from the gate driver output to the gate of the devices and the returning ground is maintained exactly equal and as short as possible. A pair of ultrafast Zener diodes with ultra-low input capacitance and ultra-small 0201 footprint are used to suppress the spike across the gate and source of the devices.

Since the EPC GaN devices have a narrow allowable gate voltage ranging from -4V to 6V, two isolated power supplies are chosen to drive the GaN FETs, converting the auxiliary supply to 5V and 3.3V respectively. To further decrease the reverse conduction losses and increase the safety margin for the gates, post-regulated low voltage drop (LDO) ICs are utilized to step down 3.3V to 1.5V. These two power supplies, +5V and +1.5V, are connected in series to provide positive and negative bias voltages for the GaN FETs with the common point being the ground for the gate drive circuit as shown in Fig. 4.

There is no kelvin source pin in the package of EPC2021 GaN FETs. However, it is highly recommended to create a kelvin source from the layout, and to use wide area copper for the ground of the gate drive circuitry. Also, the common ground of the gate drive circuitry is placed one-layer right above the bottom layer where the gate driver IC is placed. Minimizing the common source inductance is crucial for a successful gate drive design for GaN devices.

Since the EPC2021 GaN FETs have very thin Line Grid Array package, multiple PCB layers are used to provide sufficient current carrying. But the GaN FETs are supplied with die size 6.05mm*2.3mm. Special attention has been taken during the design. The width of the solder bumps and the clearance between two bumps are both 0.2mm which pose a restraint to the minimum track width and the minimum copper-to-copper clearance. This will lead to a manufacturing limitation on the maximum layer number which is needed for high current carrying capability. In this design, vias of 0.3mm diameter are added to both side of the FETs, connected to drain and source respectively. By doing this, it is possible to fabricate 10-layer PCB with 3oz copper thickness on each layer. On the bottom five layers, two horizontal long polygons are used to emulate the laminated busbars, connecting to DC+ and DC- respectively, as shown in Fig. 5. Similarly, two vertical wide polygons on the top five layers are used to connect both the

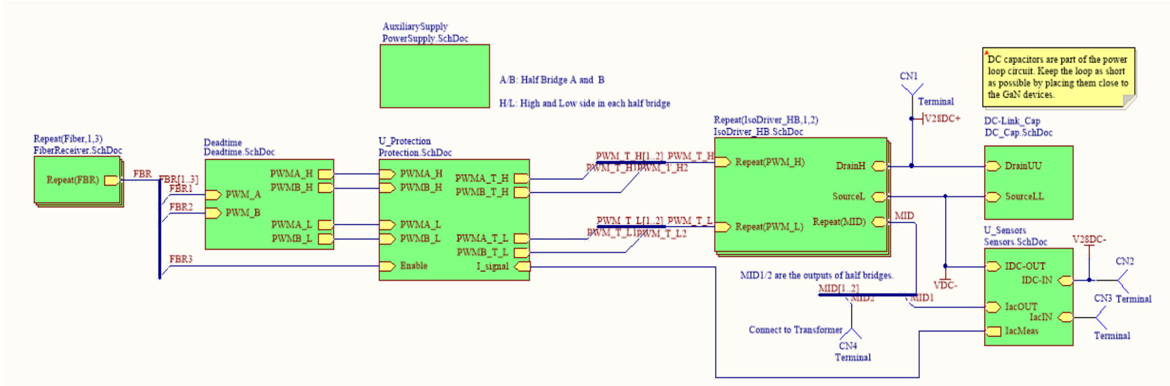

Fig. 3. Top schematic hierarchy of the low voltage board design.

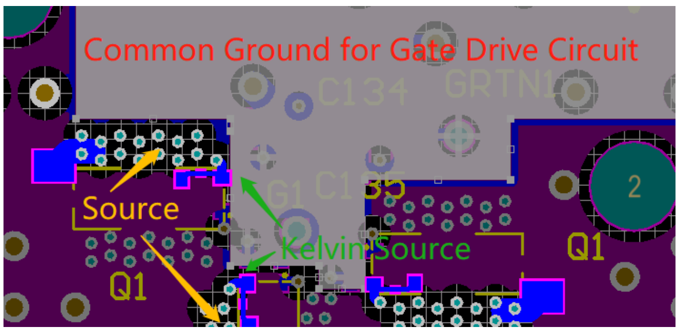

Fig. 4. Creation of Kelvin Source in the gate drive circuit.

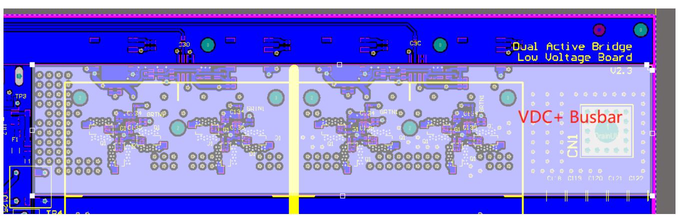

Fig. 5. VDC+ Busbar on the bottom layer.

middle points of the half bridges to the AC output connectors. By using this configuration, DC-link capacitors can be placed in the middle between VDC+ and VDC- Busbars with very small power loop inductance. According to the standard IPC-2221, the boards are aimed to carry at least 150Amps current by 50°C temperature rise.

The EPC2021 GaN FETs are placed evenly in the centre of the PCB board to distribute the heat dissipation. According to the thermal simulation and the preliminary experimental testing results, two extruded heatsinks with fan assembly, TDEX6015/TH12G whose thermal resistor is 0.50 °C/W, are used, each half-bridge using one heat-sink. The three-dimension view of the Low Voltage Board is shown in Fig. 6.

B. High-voltage H-bridge Board

The HV H-bridge circuit uses the similar schematic structure as the LV side. Only the differences from the LV board

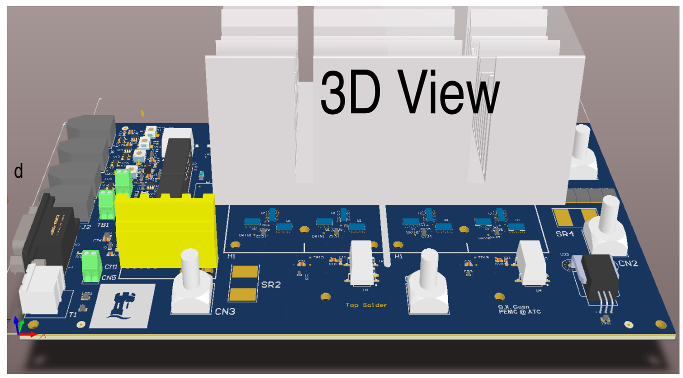

Fig. 6. Three-Dimension View of the LV Board.

design are elucidated in this subsection.

HV GaN FETs have wider gate voltage range which significantly relaxes the design for the gate driving supplies. A simple diode clamped circuit is used to split an isolated 9V supply output into +6V for turn-on and -3V for turn-off.

The most difficulty of the HV side design is to deal with the high dv/dt, which is different from the LV H-bridge boards. In the design, two GaN devices working in parallel to form one switch share one gate driver with high isolation capacity and high transient immunity.

One heatsink from Fisher, LA ICK 17*17, is selected for the H-bridge. The embedded fan can be replaced with higher speed if necessary. Overall, the three-dimension view of the How Voltage Board is shown in Fig. 7.

C. Transformer

A planar transformer for galvanic isolation is customized to have turns ratio 10:1. The transformer flux density is decided to be half of the saturation flux density of the ferrite core magnetic material 3C96. This is to provide sufficient margin for core saturation due to the unexpected DC current offset caused by fast power transition, imperfect current sensing and asymmetrical H-bridge output voltage.

The magnetizing inductance is customized around 55 uH. No additional inductor but the leakage inductance is utilized.

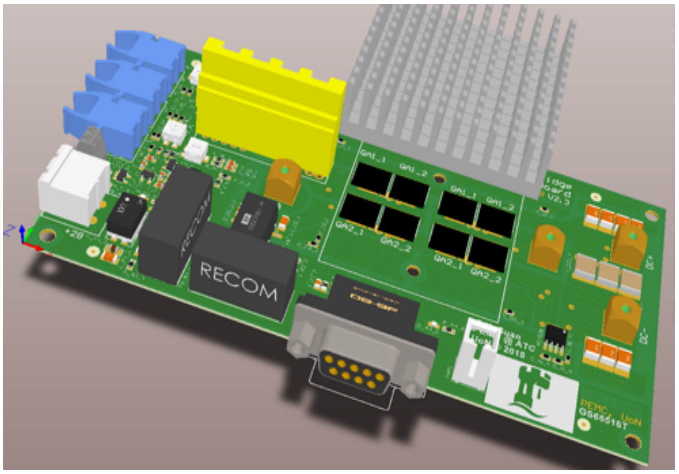

Fig. 7. Three-Dimension View of the HV Board.

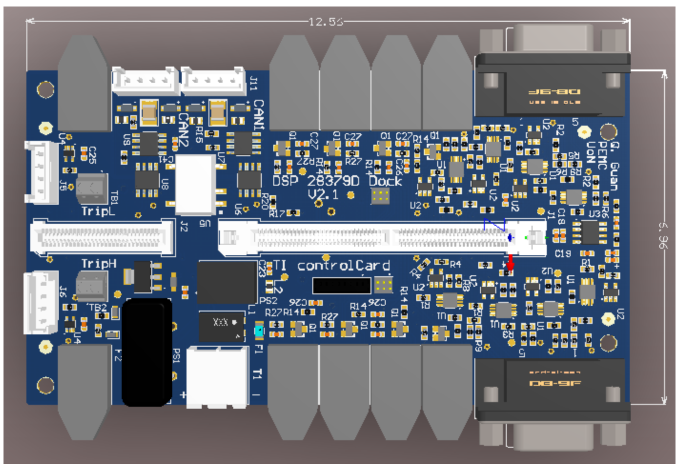

Fig. 8. Three-Dimension View of the DSP Interface Board.

D. Control Board

A dock station board is designed as the interface between the controller TI 28379D controlCard and the remaining power circuitries. This interface board consists of ADC conditioning circuits, fibre transmitters/receivers, CAN bus receivers and other connectors for digital and analogous signals. The three-dimension view of the DSP Interface Board is shown in Fig. 8.

The DSP 28379D has two cores inside, exchanging data via Interprocessor Communication (IPC) protocol. Project ASPIRE use the core-1 as the converter controller while core-2 as a local supervisor who receives commands through CAN Bus from upper level supervisors running the protection algorithm and then generating the power reference to the local converter.

III. Soft-Starting and Control

DAB converters can be controlled by the single phase shift (SPS) modulation [24]. After the control board receives the voltage and current measurements at the HV DC outputs, a proportional integral (PI) controller is assigned to tracking the output power with respect to the power reference. In SPS the

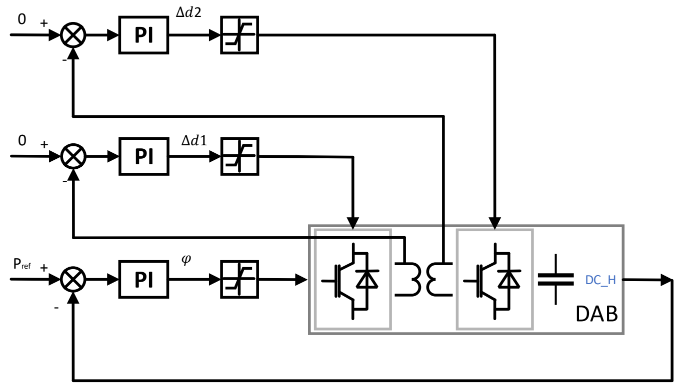

Fig. 9. Three PI controllers working in parallel to regulate the power flow and compensate the DC-offset voltages for ASPIRE converters.

TABLE I
Instruments Used in the Experiments.

Item	Part Number	Quantity
Scope 1	LeCroy MDA8000HD	1
Scope 2	LeCroy HDO6104	1
Voltage Probe	LeCroy HVD3106A	4
Current Probe 1	LeCroy CP500	1
Current Probe 2	LeCroy CP150	2
Current Probe 3	LeCroy CP031A	1
Power Supply	Delta SM500-CP90	3
Auxiliary Supply	TENMA 0-30V	1

duty cycles for the primary and secondary H-bridges are set as 50%. However, to improve the dynamic performance and remove the DC-blocking capacitors, two more PI controllers are designed to regulate the duty cycles slightly around 0.5. The three-PI-controller structure is shown in Fig. 9. The power controller compares the reference and the measured output power to determine the phase-shift, while the DC offset compensators adjust the duty-cycle to suppress the DC value of the transformer currents.

To start the converter safely from zero output, a simplified soft-starting procedure similar to [25], [26] is proposed. A rate limiter of change is employed to tune the time for soft-starting. Similar mechanism is used for the power transition and power reversal.

IV. Experiment Results

In order to validate the performance of the designed prototype, experimental tests were carried out with the instruments given in Table I. To emulate the two DC buses, three bidirectional power supplies were used with two in parallel to provide the high current at the low voltage side while the remaining to supply the high voltage.

Fig. 10 shows the waveforms at the DC terminals during starting from idle status. The delivered power is increased gradually in a stable manner to full power 3kW at around $24ms$. No significant voltage spike or inrush current can be observed from the AC-link of the transformer, as shown in Fig. 11. This demonstrates the converter has on-fly switch on capability.

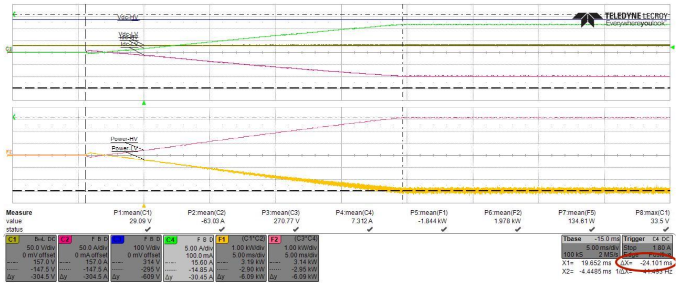

Fig. 10. DC side waveforms when the converter is soft switched on to $3kW$ nominal power reference. Channel 1: LV side voltage, Channel 2: LV side current, Channel 3: HV side voltage, Channel 4: HV side current, P5: LV side mean power, P6: HV side mean power.

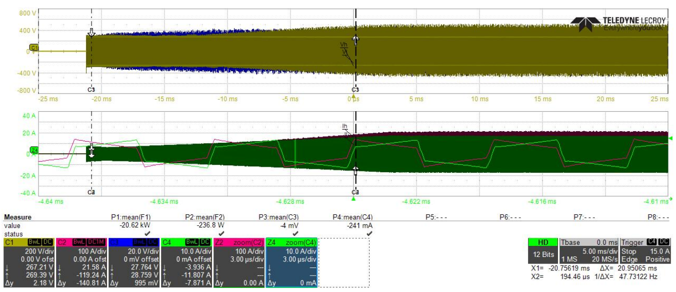

Fig. 11. AC side waveforms when the converter works at buck mode with power transferred from the HV side to the LV side. Channel 1: HV side voltage across the transformer, Channel 2: LV side current flow into the transformer, Channel 3: LV side voltage across the transformer, Channel 4: HV side current flow out of the transformer.

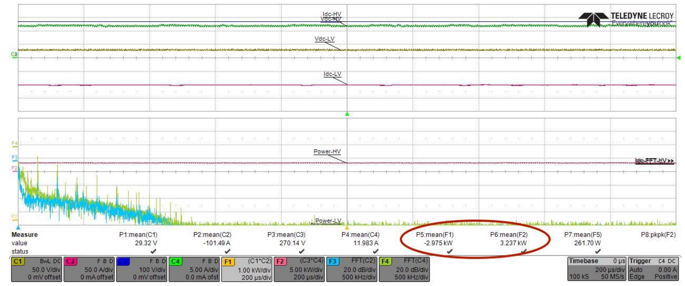

Fig. 12. DC side waveforms when the converter works at buck mode with power transferred from the HV side to the LV side. Channel 1: LV side voltage, Channel 2: LV side current, Channel 3: HV side voltage, Channel 4: HV side current, P5: LV side mean power, P6: HV side mean power, P7: Overall power loss, F3: FFT analysis to the LV side current, F4: FFT analysis to the HV side current.

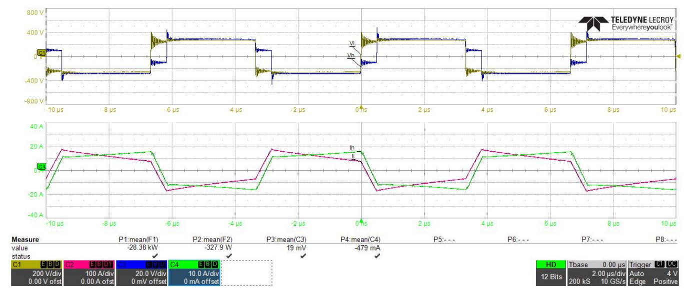

Fig. 13. AC side waveforms when the converter works at buck mode with power transferred from the HV side to the LV side. Channel 1: HV side voltage across the transformer, Channel 2: LV side current flow into the transformer, Channel 3: LV side voltage across the transformer, Channel 4: HV side current flow out of the transformer.

Fig. 12 and Fig. 13 show the waveforms when the converter transfers $3kW$ to the LV side. Fig. 14 and Fig. 15 show the waveforms when the converter transfers full power to the HV side. They validate that the converter can work at both Buck and Boost modes.

To check the duration for power reversal, references are given to the converter from positive full power to negative full power and vice the versa. The outcome is given in Fig. IV that shows the converter can operate for sudden reversal of power. The transition is less than $50ms$. This duration can be reduced easily by decreasing the rate of reference changing.

The system efficiency is preliminarily calculated according to the oscilloscope measurements and shown in Fig. 17. The converter has a peak efficiency around 95.5% for a power range of $1400W$ to $1800W$.

V. Conclusions

This paper has presented the design and implementation of a fully-GaN-based DAB converter for Project ASPIRE to facilitate the intelligent energy management in aircrafts. A soft-starting procedure and a three-PI in parallel structure controller is proposed to guarantee that the converter can work at high frequency above $100kHz$ to provide full power transfer in buck and boost modes. Besides, the converter allows on-fly turn-on, turn-off and fast power reversal with the duration tunable. A peak efficiency around 95.5% is achieved at the power range of $1400W$ to $1800W$ when the converter transfer power from the HV side to the LV side.

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Fig. 14. DC side waveforms when the converter works at boost mode with power transferred from the LV side to the HV side. Channel 1: LV side voltage, Channel 2: LV side current, Channel 3: HV side voltage, Channel 4: HV side current, P5: LV side mean power, P6: HV side mean power, P7: Overall power loss, F3: FFT analysis to the LV side current, F4: FFT analysis to the HV side current.

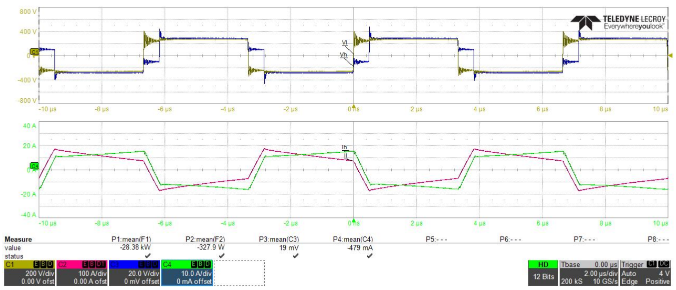

Fig. 15. AC side waveforms when the converter works at boost mode with power transferred from the LV side to the HV side. Channel 1: HV side voltage across the transformer, Channel 2: LV side current flow into the transformer, Channel 3: LV side voltage across the transformer, Channel 4: HV side current flow out of the transformer.

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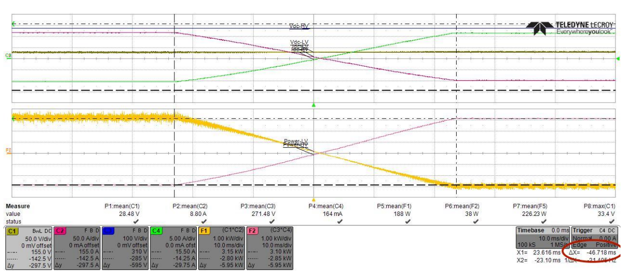

Fig. 16. DC side waveforms when the power reference is set from positive 3kW to negative 3kW. Channel 1: LV side voltage, Channel 2: LV side current, Channel 3: HV side voltage, Channel 4: HV side current, P5: LV side mean power, P6: HV side mean power.

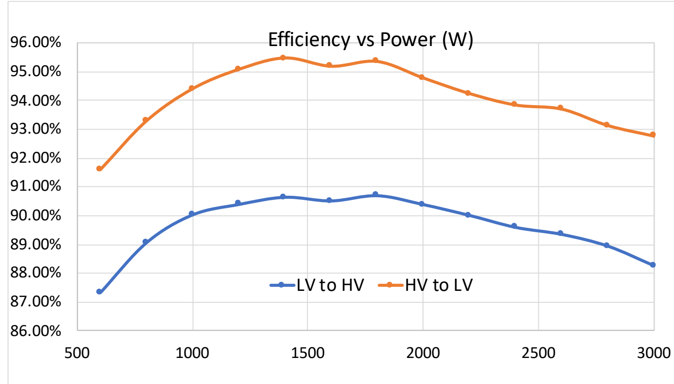

Fig. 17. Power efficiency calculation for both the cases of transferring power from LV side to HV side and the reverse direction.

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